RAMTRON ADVANCE

FM1808S FRAM® Memory

262,144-Bit Nonvolatile Ferroelectric RAM
Product Preview

Features

- 256K Nonvolatile Ferroelectric RAM
  Organized as 32,768 words x 8 bits
- CMOS Technology with Integrated Ferroelectric Storage Cells
- Fully Synchronous Operation
  - 150ns Read Access
  - 235ns Read/Write Cycle Time
  - 10^{12} Read/Write Cycle Endurance
- 10 Year Data Retention
- JEDEC Standard 21-C Write Protection (Entire Memory) and Selectable 4K Byte Write Protection
- Single 3 Volt Supply (2.7V to 3.6V)
- Low Power Consumption
  - Active Current: 20mA Typical
  - Standby Current: 15µA Typical
- CMOS Compatible I/O Pins
- SOP and TSOP Packages
- 0° to +70°C Ambient Operating Temperature Range

Description

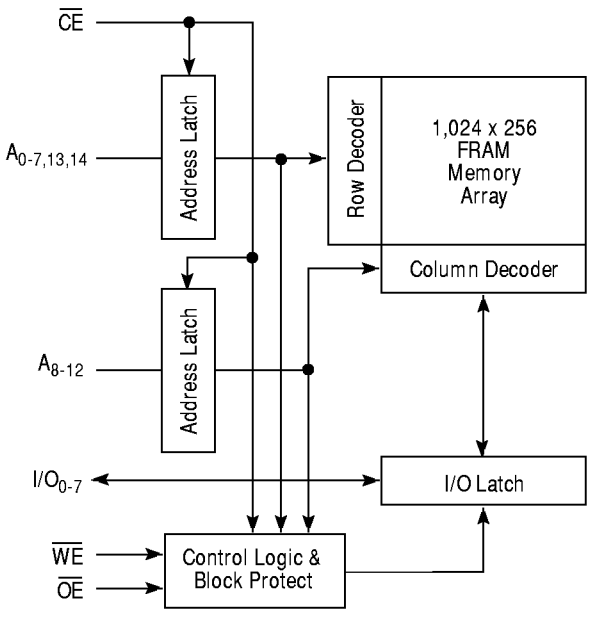
The FM1808S is a ferroelectric RAM, or FRAM® memory, organized as 32k words x 8 bits. FRAM memory products from Ramtron combine the read/write characteristics of semiconductor RAM with nonvolatile storage.

This product is manufactured in a 0.8 micron silicon gate CMOS technology with the addition of integrated thin film ferroelectric storage cells developed and patented by Ramtron.

The ferroelectric cells are polarized on each read or write cycle, therefore no special store or recall sequence is required. The memory is always static and nonvolatile.

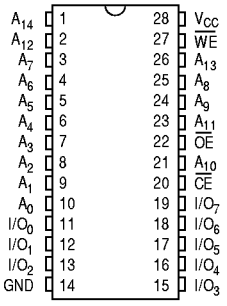
Ramtron's FRAM products operate from a single 3 volt power supply and are CMOS compatible on all inputs and outputs. The FM1808S utilizes the JEDEC standard bytewide SRAM pinout.

Functional Diagram



Pin Configuration

SOP



TSOP

This product was jointly developed by Ramtron International Corporation and Hitachi Limited.

This document describes a product under development. Ramtron reserves the right to change or discontinue this product without notice.

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Device Operation

Read Operation

When $\overline{CE}$ is low and $\overline{WE}$ is high, a read operation is performed by the FRAM memory. On the falling edge of $\overline{CE}$, all address bits (A_0 - A_{14}) are latched into the part and the cycle is started. Data will appear on the output pins a maximum access time (t_{OE}) after the beginning of the cycle.

The designer should ensure that there are no address transitions from t_{AS} (setup time) before the falling edge of $\overline{CE}$ to t_{AH} (hold time) after it. After t_{AH}, the address pins are ignored for the remainder of the cycle. It is equally important that $\overline{CE}$ be generated such that unwanted glitches or pulses, of any duration, be prevented.

After the read has completed, $\overline{CE}$ should be brought high for the precharge interval (t_{PC}). During this period data is restored in the internal memory cells and the chip is prepared for the next read or write cycle. The FM1808S will not operate in systems in which $\overline{CE}$ does not toggle with every access.

The $\overline{OE}$ pin may be used to avoid bus conflicts on the system bus. Only when both $\overline{CE}$ and $\overline{OE}$ are low will the FRAM memory drive its outputs. Under all other circumstances, the output drivers are held in a high impedance (High-Z) condition. Note that the internal read operation is performed regardless of the state of the $\overline{OE}$ pin.

Write Operation

When $\overline{CE}$ falls while $\overline{WE}$ is low, or $\overline{WE}$ falls while $\overline{CE}$ is low, a write operation will be performed by the FRAM memory. On the falling edge of $\overline{CE}$, as in the read cycle, the address will be latched into the part with the same setup and hold requirements. As in the read cycle, $\overline{CE}$ must be held high for a precharge interval (t_{PC}) between each access.

Data needs to be set up t_{DS} minimum on the rising edge of $\overline{WE}$ or $\overline{CE}$, whichever occurs first. Write operations take place regardless of the state of $\overline{OE}$, however, it may need to be driven high by the system at the beginning of the cycle in order to avoid bus conflicts.

Data is immediately nonvolatile and power may be removed from the part upon completion of the precharge interval following the write. For better noise immunity, a 10ns (typical) glitch protection is built into the $\overline{WE}$ signal.

Low Voltage Protection

When V_{CC} is below 2.4V (typical), all read and write operations to the part will be ignored. For systems in which unwanted signal transitions would otherwise occur on the $\overline{CE}$ pin at or above this voltage, $\overline{CE}$ should be held high with a power supply monitor circuit.

Whenever V_{CC} rises above 2.4V, either after power up or a brownout, no read or write operation will take place until $\overline{CE}$ has been high (above V_{IH}) for at least a precharge interval (t_{PC}). When $\overline{CE}$ is brought low, an access will start.

Write Protection

The FM1808S FRAM memory uses a superset of the JEDEC Standard 21-C for software data protection. The standard allows for the entire memory array to be protected or unprotected via software control. Ramtron enhanced the standard to allow each of the 4K word blocks on the FM1808S to be individually protected or unprotected. The protection data map is stored in the nonvolatile block protection register. This data can be recalled at any time via the enhanced standard to restore the previously stored block protection map. The configuration data may also be modified via the enhanced standard.

Standard JEDEC Protection

Upon power up, the entire memory array is write protected as per the JEDEC standard. If desired, the entire memory array can be unprotected by executing the JEDEC disable sequence shown in Table 1. The entire memory array can be write protected by executing the JEDEC enable sequence shown in Table 1. Any time these two sequences are executed, the respective operation will be performed i.e. one should insure that these sequence of addresses is only executed if enabling or disabling write protection.

Table 1. JEDEC Write Protect Sequence

Cycle	*Disable Sequence*	*Enable Sequence*	*Mode*
1	1823 Hex	1823 Hex	Read
2	1820 Hex	1820 Hex	Read
3	1822 Hex	1822 Hex	Read
4	0418 Hex	0418 Hex	Read
5	041B Hex	041B Hex	Read
6	0419 Hex	0419 Hex	Read
7	041A Hex	040A Hex	Read

Enhanced Block Protection

Ramtron added capability to the FM1808S to allow any of the eight 4K blocks to be individually protected or unprotected. This feature is enabled by adding one additional unique address to the standard JEDEC enable, disable sequence as shown in Table 1. To write a specific block protect map to the FM1808S, the access to this added address should be a "WRITE" access as shown in Table 2. Each bit of the data word has a one to one correlation with a specific 4K block as shown in Table 4. A data of "1" enables write protection. A data of "0" allows writing to that block. It should be noted that data written on this sequence is written to the block protect register and not to address 040F Hex. If the previously configured block protection map is to be restored, then the access to 040FH address should be a "READ" cycle as shown in Table 3. The data on the I/O pins after an access time will be the data contained in the block protect register that is being restored, not the data at address 040H. On the next rising edge of $\overline{CE}$ after executing the address sequence, in Table 2 or 3 the part will be placed into the write protected mode. The memory blocks that will be write protected will be those either written to the block protect register during this sequence or those restored from the previous

Table 2. Extended Write Protect Sequence

Cycle	Sequence	I/O	Mode
1	1823 Hex	Data	Read
2	1820 Hex	Data	Read
3	1822 Hex	Data	Read
4	0418 Hex	Data	Read
5	041B Hex	Data	Read
6	0419 Hex	Data	Read
7	041A Hex	Data	Read
8	040F Hex	New Block Protect Data	Write

Table 3. Extended Restore Protect Sequence

Cycle	Sequence	I/O	Mode
1	1823 Hex	Data	Read
2	1820 Hex	Data	Read
3	1822 Hex	Data	Read
4	0418 Hex	Data	Read
5	041B Hex	Data	Read
6	0419 Hex	Data	Read
7	041A Hex	Data	Read
8	040F Hex	Restore Block Protect Data	Read

contents of the block protect register. For example, if the block protect register contained the following data 10011000, addresses 3000H - 4FFFH and 7000H-7FFFH would be write protected, i.e., Blocks 3, 4 and 7.

On a $\overline{WE}$ Controlled write operation where $\overline{WE}$ rises prior to $\overline{CE}$, the data I/O outputs will become active a t_{WX} after $\overline{WE}$ rises. The data on the outputs mirror the data just written to the addressed location so no bus contention should arise. However, the addition of write protection required that the I/O outputs perform differently if a write to a protected location was attempted. If a write operation is attempted to a protected location, the I/O outputs remain high impedence after $\overline{WE}$ returns high. This is done to prevent any bus contention that might arise due to the data driven on the I/O lines externally and the data at the accessed memory location being different. The I/O outputs will remain high impedence until the next memory cycle.

Table 4. Block Number To I/O Correlation

4K Block Number	A_{14}	A_{13}	A_{12}	I/O #
0	0	0	0	0
1	0	0	1	1
2	0	1	0	2
3	0	1	1	3
4	1	0	0	4
5	1	0	1	5
6	1	1	0	6
7	1	1	1	7

Pin Names

Pin Names	Function
A_0 - A_{14}	Address Inputs
I/O_0 - I/O_7	Data Input/Output
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Input

Pin Names	Function
$\overline{OE}$	Output Enable Input
V_{CC}	Power
GND	Ground

Truth Table

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Function
H	X	X	Standby/Precharge
↘	X	X	Latch Address
L	H	L	Read
L	L	X	Write

Absolute Maximum Ratings(1)

(Beyond Which Permanent Damage Could Result)

Description	*Ratings*
Ambient Storage or Operating Temperature to Guarantee Nonvolatility of Stored Data	-40 to +85°C
Voltage on Any Pin with Respect to Ground	-1.0 to +7.0V
Lead Temperature (Soldering, 10 Seconds)	300°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. This is a stress rating only, and the functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Capacitance

T_A = 25°C, f = 1.0MHz, V_{CC} = 3V

Parameter	*Description*	*Max*	*Test Condition*
$C_{I/O}$(2)	Input/Output Capacitance	8pF	$V_{I/O}$ = 0V
C_{IN}(2)	Input Capacitance	6pF	$V_{I/O}$ = 0V

(2) This parameter is periodically sampled and not 100% tested.

DC Operating Conditions

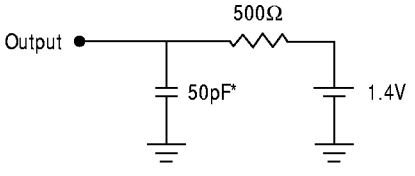
T_A = 0° to 70°C, Typical Values at 25°C

Symbol	*Parameters*	*Min*	*Typ*	*Max*	*Test Condition*
V_{CC}	Power Supply Voltage	2.7V	3.0	3.6V	
I_{CC}	Power Supply Current - Active		20mA	30mA	V_{CC} = Maximum, $\overline{CE}$ Cycling at Minimum Cycle Time $I_{I/O}$ = 0mA; $\overline{OE}$, $\overline{WE}$, A_x = CMOS Input Levels
I_{SB}	Power Supply Current - Standby (CMOS)		15µA	25µA	V_{CC} = Maximum, $\overline{CE}$ = V_{CC}, Input Levels = V_{CC} or GND, $I_{I/O}$ = 0mA
I_{IL}	Input Leakage Current			10µA	V_{IN} = GND to V_{CC}
I_{OL}	Output Leakage Current			10µA	V_{OUT} = GND to V_{CC}
V_{IL}	Input Low Voltage	-.3V		0.2* V_{CC}	
V_{IH}	Input High Voltage	0.7* V_{CC}		V_{CC}+0.3V	
V_{OL}	Output Low Voltage			0.2V	I_{OL} = 100µA
				0.4V	I_{OL} = 2.0mA
V_{OH}	Output High Voltage	V_{CC} -0.2V			I_{OH} = -100µA
		2.4V			I_{OH} = -2.0mA

AC Conditions of Test

AC Conditions	*Test*
Input Pulse Levels	0 to Vcc
Input Rise and Fall Time	<10ns
Input and Output Timing Levels	1.5V

Equivalent AC Test Load Circuit



(* including scope and jig)

Read Cycle AC Parameters

T_A = 0° to 70°C, V_{CC} = 2.7V - 3.6V

Symbol	*Parameter*	*JEDEC Symbol*	*Min*	*Max*	*Units*
t_{RC}	Read Cycle Time	t_{ELEL}	235		ns
t_{CA}	Chip Enable Active Time	t_{ELEH}	150	10,000	ns
t_{PC}	Precharge Time	t_{EHEL}	85		ns
t_{AS}	Address Setup Time	t_{AVEL}	0		ns
t_{AH}	Address Hold Time	t_{ELAX}	15		ns
t_{CE}	Chip Enable Access Time	t_{ELQV}		150	ns
t_{OE}	Output Enable Access Time	t_{OLQV}		25	ns
$t_{HZ}^{(2)}$	Chip Enable to Output High-Z	t_{EHQZ}		25	ns
$t_{OHZ}^{(2)}$	Output Enable to Output High-Z	t_{OHQZ}		25	ns

(2) This parameter is periodically sampled and not 100% tested.

Write Cycle AC Parameters

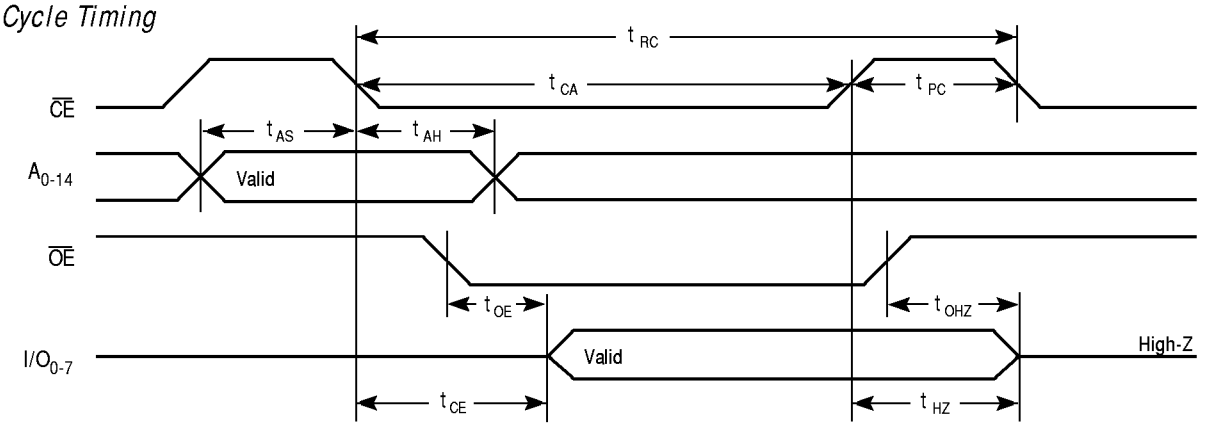
T_A = 0° to 70°C, V_{CC} = 2.7V - 3.6V

Symbol	*Parameter*	*JEDEC Symbol*	*Min*	*Max*	*Units*
t_{WC}	Write Cycle Time	t_{ELEL}	235		ns
t_{CA}	Chip Enable Active Time	t_{ELEH}	150	10,000	ns
t_{CW}	Chip Enable to Write High	t_{ELWH}	150		ns
t_{PC}	Precharge Time	t_{EHEL}	85		ns
t_{AS}	Address Setup Time	t_{AVEL}	0		ns
t_{AH}	Address Hold Time	t_{ELAX}	15		ns
t_{WP}	Write Enable Pulse Width	t_{WLWH}	50		ns
t_{DS}	Data Setup Time	t_{DVWH}	50		ns
t_{DH}	Data Hold Time	t_{WHDX}	0		ns
$t_{WZ}^{(2)}$	Write Enable Low to Output High-Z	t_{WLQZ}		25	ns
$t_{WX}^{(2)}$	Write Enable High to Output Driven	t_{WHQX}	10		ns
$t_{HZ}^{(2)}$	Chip Enable to Output High-Z	t_{EHQZ}		25	ns
$t_{WS}^{(5)}$	Write Setup	t_{CLWL}	0		ns
$t_{WH}^{(5)}$	Write Hold	t_{WHCH}	0		ns

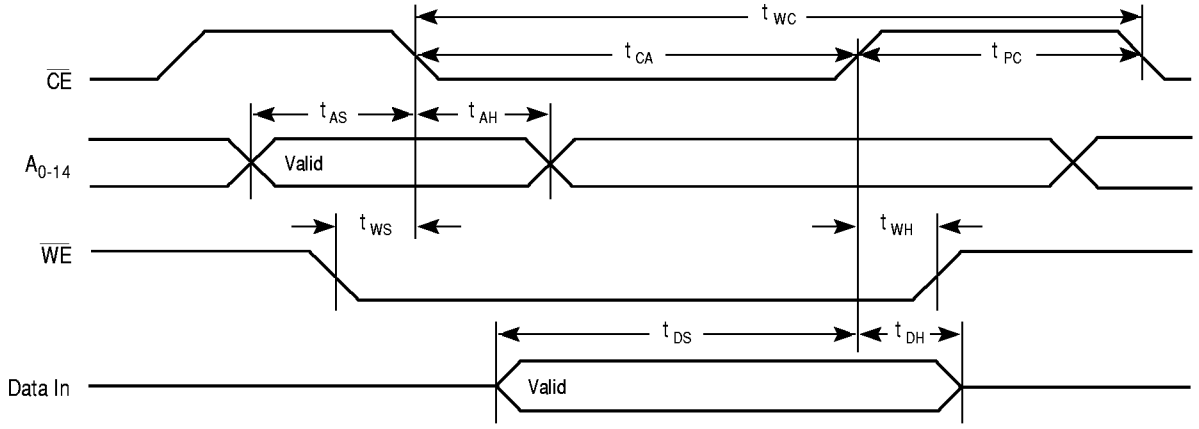
(2) This parameter is periodically sampled and not 100% tested.

(5) Not a device specification, merely distinguishes $\overline{CE}$ and $\overline{WE}$ controlled accesses.

Read Cycle Timing

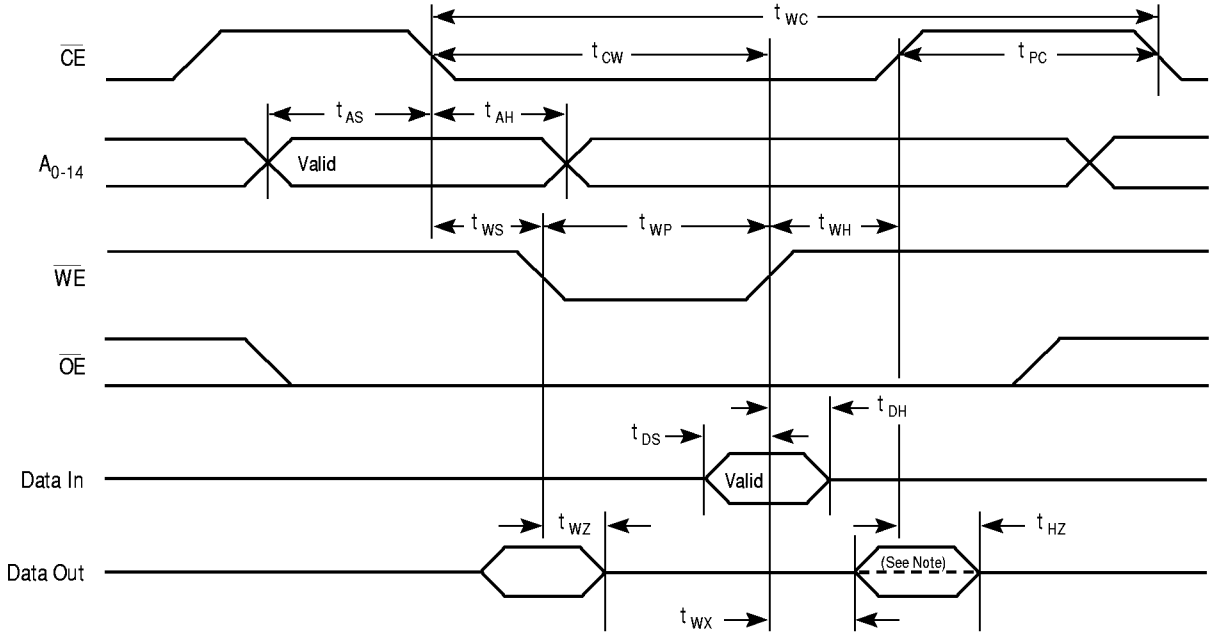


$\overline{CE}$ Controlled Write (6)



(6) State of $\overline{OE}$ does not affect operation of device for this cycle.

$\overline{WE}$ Controlled Write



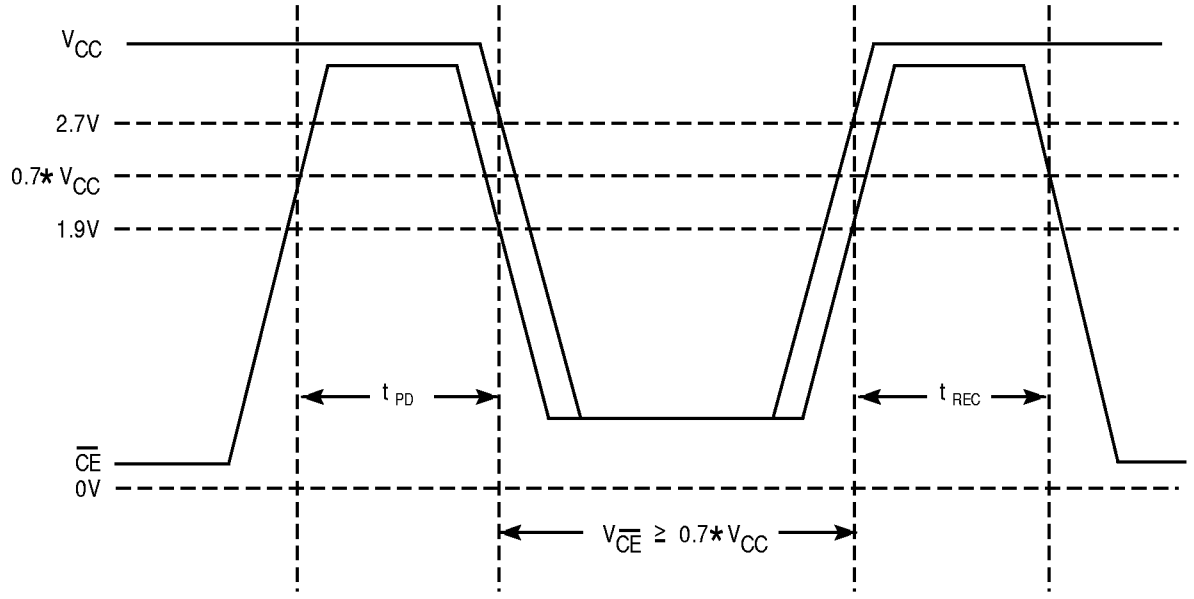
Note: Output remains high impedence after write attempt to a protected memory location.

Power-Down/Power-Up Conditions

Care must be taken during power sequencing to prevent data loss resulting from memory operations during out of spec voltage conditions. This is managed by detecting power failure with sufficient time t_{PD} to disable memory operation prior to V_{CC} dropping below its lower specification, +2.7 volts. During power up, the memory operation should be disabled until time t_{REC} after V_{CC} reaches its minimum operating voltage, +2.7 volts.

The memory has an on-chip data protection circuit which prevents memory operation when V_{CC} is less than +2.5 volts. This will protect the data in CMOS systems where the system control logic continues to function at or below +2.5 volts. However, external circuitry is required to force $\overline{CE}$ to a high level in systems with control logic that does not operate to +2.5 volts to prevent false memory operations from being initiated by the system control logic during this unspecified voltage range. There are a number of precision DC voltage detector circuits available to implement this function.

Power Up/Power Down Conditions

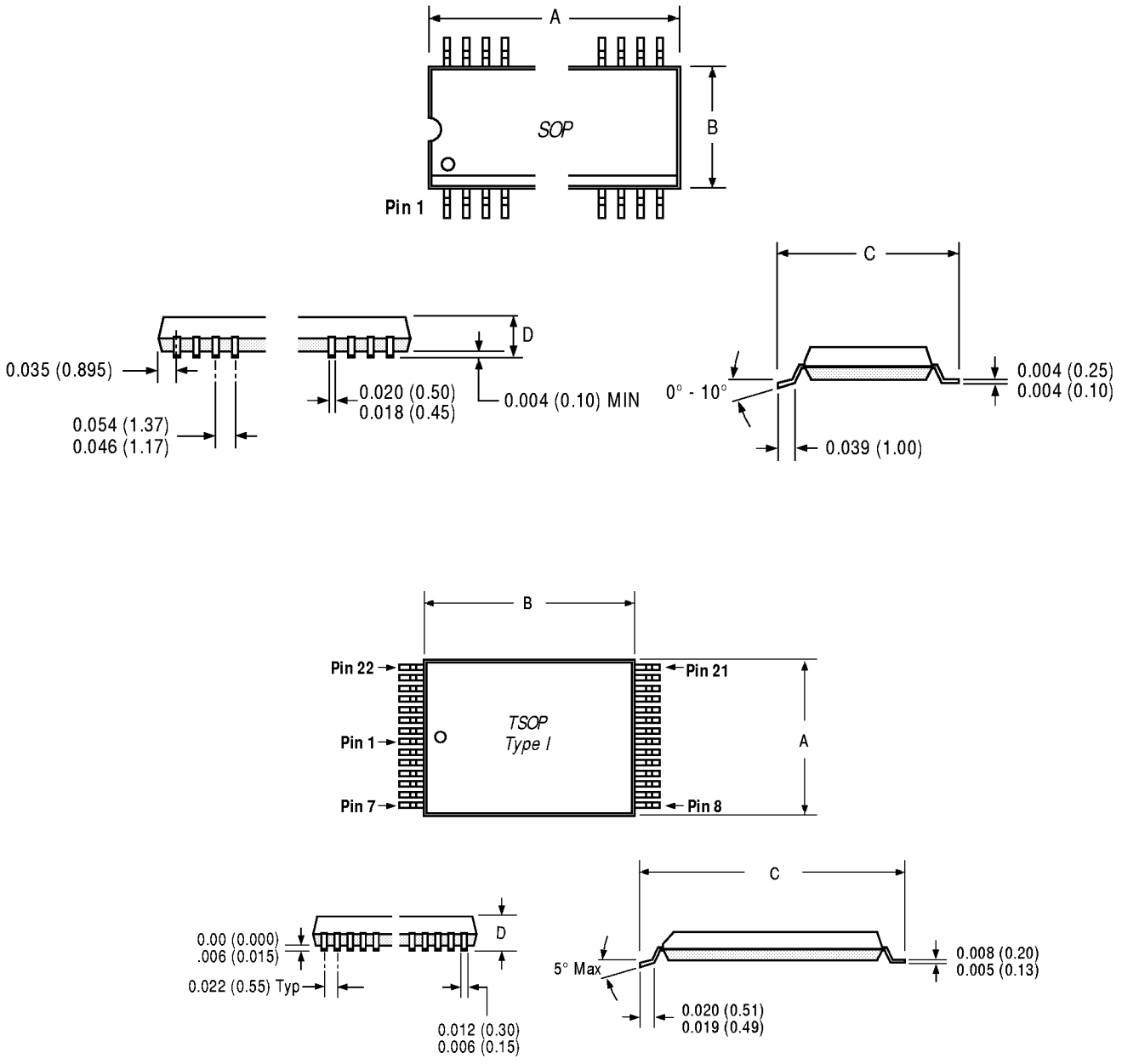


Power Up/Power Down Timing

Symbol	Parameter	Min	Typ	Max	Units
t_{PD}	$\overline{CE}$ Signal Stable to Power Down	85			ns
t_{REC}	Power-up to Operation	85			ns

Packaging Information

Package	Type	Dimensions in Inches (Millimeters)			
		FM1808S 28-Pin			
		A	B	C	D
Plastic SOP	S	0.738 (18.75) Max 0.720 (18.30) Typ	0.331 (8.40) Typ	0.476 (12.10) Max 0.453 (11.50) Min	0.118 (3.00) Max
Plastic TSOP	T	0.319 (8.10) Max 0.315 (8.00) Typ	0.465 (11.8) Typ	0.539 (13.70) Max 0.516 (13.10) Min	0.047 (1.20) Max



Ordering Information