SONY CXK5971AP/AM/AJ-25/30/35

8192-word × 9-bit High Speed CMOS Static RAM

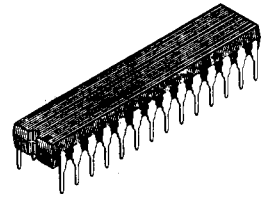
Description

CXK5971AP/AM/AJ are 73,728 bits high speed CMOS static RAMs organized as 8,192-word by 9-bit and operate from a single 5V supply. These devices are suitable for use in high speed and low power applications in which battery back up for nonvolatility is required.

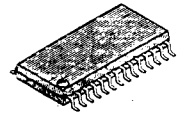
Features

- Fast access time 25ns/30ns/35ns (Max.)
- Low power standby 5 μW (Typ.)
- Low power operation 300mW (Typ., Cycle=Min.)
- Single + 5V supply: 5V ± 10%
- Fully static memory...No clock or timing strobe required.
- Equal access and cycle time.
- Common data input and output: three state output.
- Directly TTL compatible: all inputs and outputs.
- Low voltage data retention: 2.0V (Min.)
- Available in 28 pin 300mil DIP, 450mil SOP, and 300mil SOJ.

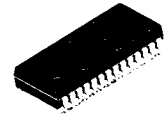
CXK5971AP
28 pin DIP (Plastic)



CXK5971AM
28 pin SOP (Plastic)



CXK5971AJ
28 pin SOJ (Plastic)



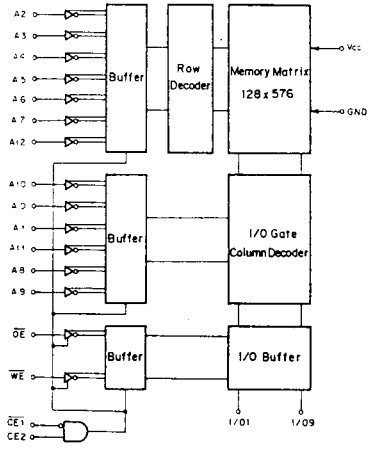
Function

8192-word × 9-bit static RAM

Structure

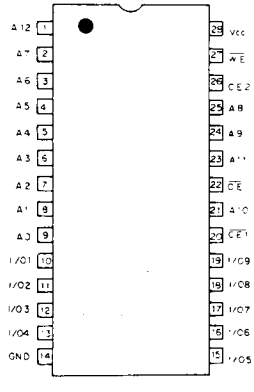
Silicon gate CMOS IC

Block Diagram



Pin Configuration

(Top View)



Pin Description

Symbol	Description
A0 to A12	Address input
I/O1 to I/O9	Data input output
$\overline{CE1}$, CE2	Chip enable 1, 2 input
$\overline{WE}$	Write enable input
$\overline{OE}$	Output enable input
Vcc	+5V Power supply
GND	Ground

PE91795 – ST

Absolute Maximum Ratings (Ta=25℃, GND=0V)

Item	Symbol		Rating	Unit
Supply voltage	V_{CC}		−0.5 * to +7.0	V
Input voltage	V_{IN}		−0.5 * to V_{CC}+0.5	V
Input and output voltage	$V_{I/O}$		−0.5 * to V_{CC}+0.5	V
Allowable power dissipation	P_D	CXK5971AP/AJ	1.0	W
		CXK5971AM	0.7	W
Operating temperature	Topr		0 to +70	℃
Storage temperature	Tstg		−55 to +150	℃
Soldering temperature• time	Tsolder		260 • 10	℃ • sec

* V_{CC}, V_{IN}, $V_{I/O}$=−3.5V Min. for pulse width less than 20ns.

Truth Table

$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1 to I/O9	Vcc Current
H	×	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
×	L	×	×	Not selected	High Z	I_{SB1}, I_{SB2}
L	H	H	H	Output disable	High Z	I_{CC1}, I_{CC2}
L	H	L	H	Read	Data out	I_{CC1}, I_{CC2}
L	H	×	L	Write	Data in	I_{CC1}, I_{CC2}

× : "H" or "L"

DC Recommended Operating Conditions (Ta=0 to +70℃, GND=0V)

Item	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V
Input low voltage	V_{IL}	−0.3 *	—	0.8	V

* V_{IL}=−3.0V Min. for pulse width less than 20ns.

5

Electrical Characteristics

DC and operating characteristics

(Vcc=5V ± 10%, GND=0V, Ta=0 to +70°C)

Item	Symbol	Test condition	– 25/30/35			Unit
			Min.	Typ. *	Max.	
Input leakage current	I_{LI}	V_{IN}=GND to Vcc	–1	—	1	µA
Output leakage current	I_{LO}	$V_{I/O}$=GND to Vcc, $\overline{CE1}$=V_{IH} or CE2=V_{IL} or $\overline{OE}$=V_{IH} or $\overline{WE}$=V_{IL}	–1	—	1	µA
Operating power supply current	I_{CC1}	$\overline{CE1}$=V_{IL}, CE2=V_{IH}, V_{IN}=V_{IH} or V_{IL} I_{OUT}=0mA	—	—	—	mA
Average operating current	I_{CC2}	Cycle=Min, Duty=100%, I_{OUT}=0mA	—	60	90	mA
Standby current	I_{SB1}	$\overline{CE1}$ ≧ Vcc–0.2V or CE2 ≦ 0.2V V_{IN} ≧ Vcc–0.2V or V_{IN} ≦ 0.2V	—	1	100	µA
	I_{SB2}	$\overline{CE1}$=V_{IH} or CE2=V_{IL}, V_{IN}=V_{IH}/V_{IL}, Cycle=Min.	—	10	25	mA
Output high voltage	V_{OH}	I_{OH}=–4.0mA	2.4	—	—	V
Output low voltage	V_{OL}	I_{OL}=8.0mA	—	—	0.4	V

* Vcc=5V, Ta=25°C

I/O Capacitance

(Ta=25°C, f=1MHz)

Item	Symbol	Test condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{IN}=0V	—	6	pF
I/O capacitance	$C_{I/O}$	$V_{I/O}$=0V	—	6	pF

Note) This parameter is sampled and is not 100% tested.

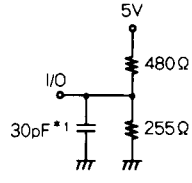
AC Characteristics

• AC test conditions

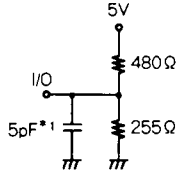
(Vcc=5V ± 10%, Ta=0 to +70°C)

Item	Conditions
Input pulse high level	V_{IH}=3.0V
Input pulse low level	V_{IL}=0V
Input rise time	tr=5ns
Input fall time	tf=5ns
Input and output reference level	1.5V
Output load conditions	Fig. 1

Output Load (1)



Output Load (2)*2



*1. including scope and jig capacitance
*2. for t_{LZ1}, t_{LZ2}, t_{OLZ}, t_{HZ1}, t_{HZ2}, t_{OHZ}, t_{OW}, t_{WH2}

Fig. 1

• Read cycle

Item	Symbol	− 25		− 30		− 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	25	—	30	—	35	—	ns
Address access time	t_{AA}	—	25	—	30	—	35	ns
Chip enable access time ($\overline{CE1}$)	t_{CO1}	—	25	—	30	—	35	ns
Chip enable access time (CE2)	t_{CO2}	—	25	—	30	—	35	ns
Output enable to output valid	t_{OE}	—	12	—	12	—	15	ns
Output hold from address change	t_{OH}	5	—	5	—	5	—	ns
Chip enable to output in low Z ($\overline{CE1}$, CE2)	t_{LZ1}* t_{LZ2}*	5	—	5	—	5	—	ns
Output enable to output in low Z ($\overline{OE}$)	t_{OLZ}*	0	—	0	—	0	—	ns
Chip disable to output in high Z ($\overline{CE1}$, CE2)	t_{HZ1}* t_{HZ2}*	0	12	0	12	0	15	ns
Chip disable to output in high Z ($\overline{OE}$)	t_{OHZ}*	0	10	0	10	0	12	ns
Chip enable to power up time ($\overline{CE1}$, CE2)	t_{PU}	0	—	0	—	0	—	ns
Chip disable to power down time ($\overline{CE1}$, CE2)	t_{PD}	—	20	—	20	—	20	ns

• Write cycle

Item	Symbol	− 25		− 30		− 35		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	25	—	30	—	35	—	ns
Address valid to end of write	t_{AW}	20	—	20	—	30	—	ns
Chip enable to end of write	t_{CW}	20	—	20	—	30	—	ns
Data to write time overlap	t_{DW}	12	—	12	—	15	—	ns
Data hold from write time	t_{DH}	0	—	0	—	0	—	ns
Write pulse width	t_{WP}	20	—	20	—	25	—	ns
Address set up time	t_{AS}	0	—	0	—	0	—	ns
Write recovery time ($\overline{WE}$)	t_{WR}	0	—	0	—	0	—	ns
Write recovery time ($\overline{CE1}$, CE2)	t_{WR1}	0	—	0	—	0	—	ns
Output active from end of write	t_{OW}*	5	—	5	—	5	—	ns
Write to output in high Z	t_{WHZ}*	0	12	0	12	0	15	ns

* Transition is measured ± 500mV from steady voltage with specified loading in Fig. 1-(2).
This parameter is sampled and is not 100% tested.

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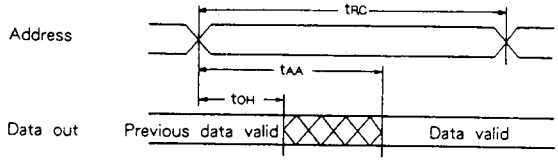
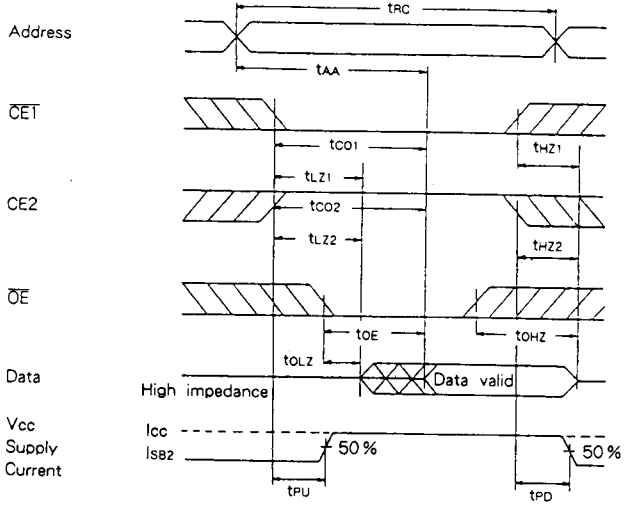
Timing Waveform

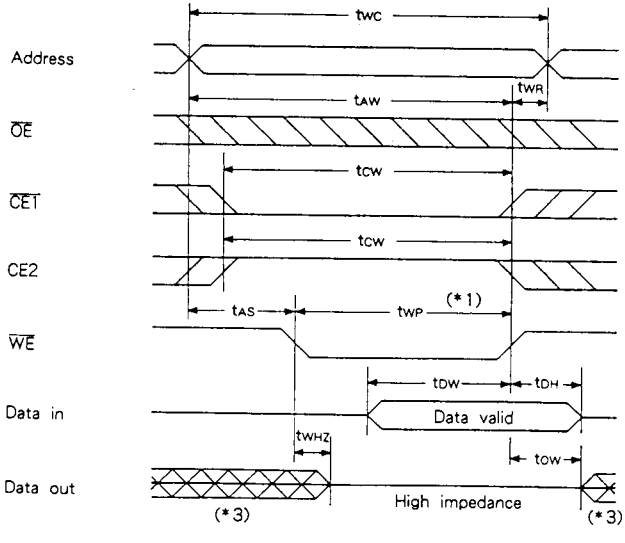
• Read cycle (1): $\overline{CE1}$=$\overline{OE}$=V_{IL}, CE2=V_{IH}, $\overline{WE}$=V_{IH}



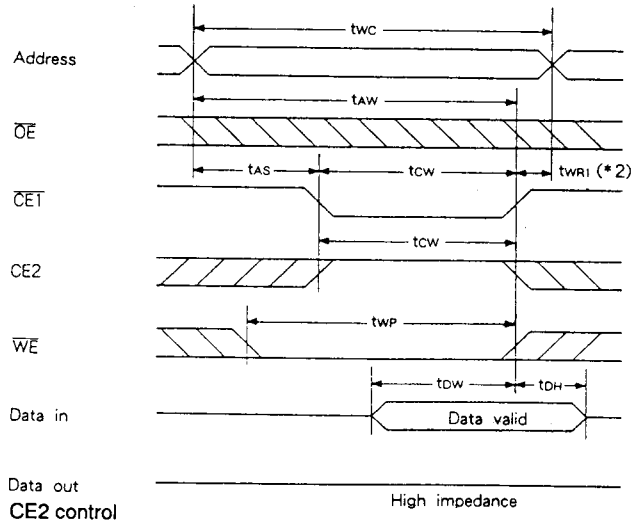
• Read cycle (2): $\overline{WE}$=V_{IH}



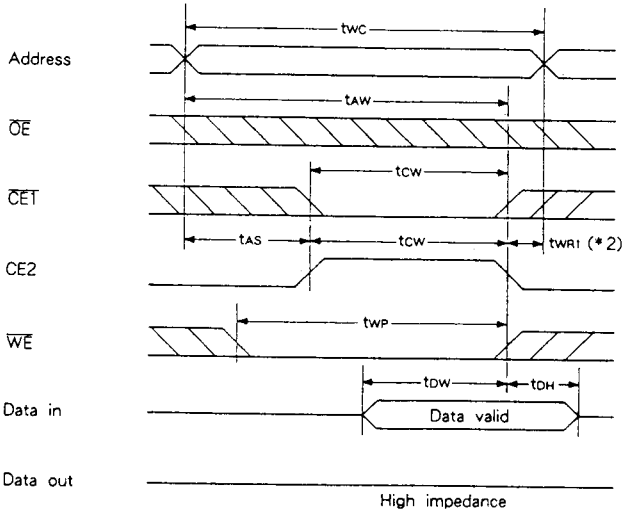
• Write cycle (1): $\overline{WE}$ control



• Write cycle (2): $\overline{CE1}$ control



• Write cycle (3): CE2 control



Note)

*1. Write is executed when both $\overline{CE1}$ and $\overline{WE}$ are at low and CE2 is at high simultaneously.

*2. t_{WR1} is tested from either the rising edge of $\overline{CE1}$ or the falling edge of CE2, whichever comes earlier, until the end of the write cycle.

*3. Do not apply the data input voltage of the opposite phase to the output while the I/O pin is in output condition.

5

Data Retention Characteristics

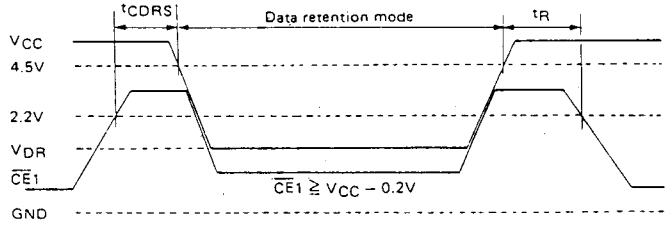
(Ta=0 to+70°C)

Item	Symbol	Test condition	−25/30/35			Unit
			Min.	Typ.	Max.	
Data retention voltage	V_{DR}	*1	2.0	5.0	5.5	V
Data retention current	I_{CCDR1}	Vcc=3.0V *1	—	0.5	50	μA
	I_{CCDR2}	Vcc=2.0 to 5.5V *1	—	1.0	100	μA
Data retention set up time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns
Recovery time	t_R		t_{RC} *2	—	—	ns

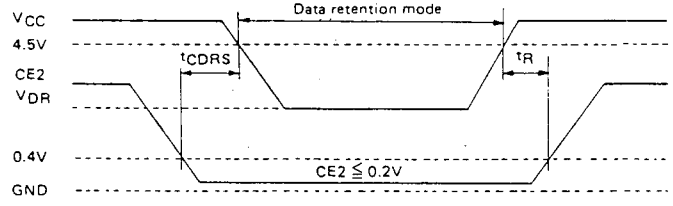
*1 $\overline{CE1} \geqq V_{CC}-0.2V$ or $CE2 \leqq 0.2V$, $V_{IN} \geqq V_{CC}-0.2V$ or $V_{IN} \leqq 0.2V$

*2 t_{RC}: Read cycle time

Data Retention Waveform (1): $\overline{CE1}$ control

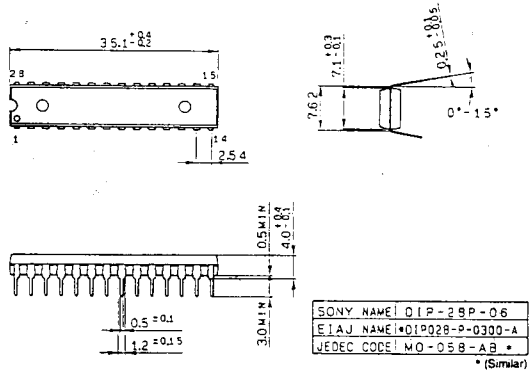


Data Retention Waveform (2): CE2 control

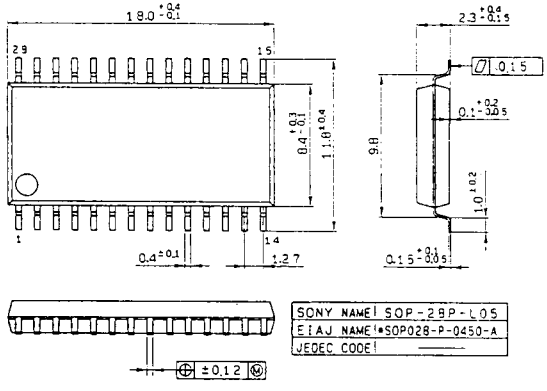


Package Outline Unit : mm

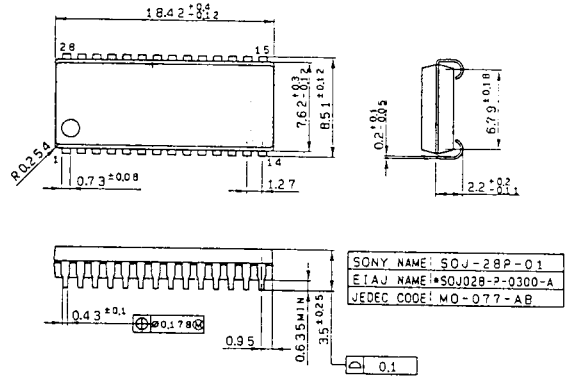
CXK5971AP 28pin DIP (Plastic) 300mil 2.0g



CXK5971AM 28pin SOP (Plastic) 450mil 0.7g



CXK5971AJ 28pin SOJ (Plastic) 300mil 0.8g



5