



# HIGH SPEED CMOS SRAM

## 256K-BIT(32K X 8)

### N341256L

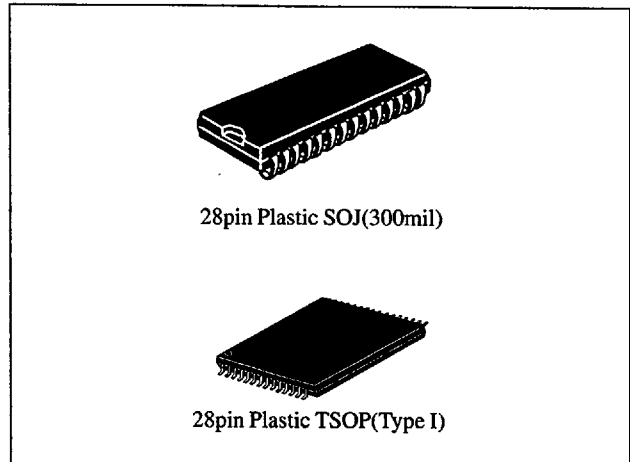
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#### ■ Features

- CMOS SRAM organized as 32,768 x 8bits
- Single+3.3V ( ± 0.3V) Power Supply
- High Speed Access time : 15ns
- Low power operation
  - Active : 90mA (Max.)
  - Standby : 1mA (Max.)

#### ● Packages

- 28pin Plastic SOJ(300mil)
- 28pin Plastic TSOP(Type I)



#### ■ Description

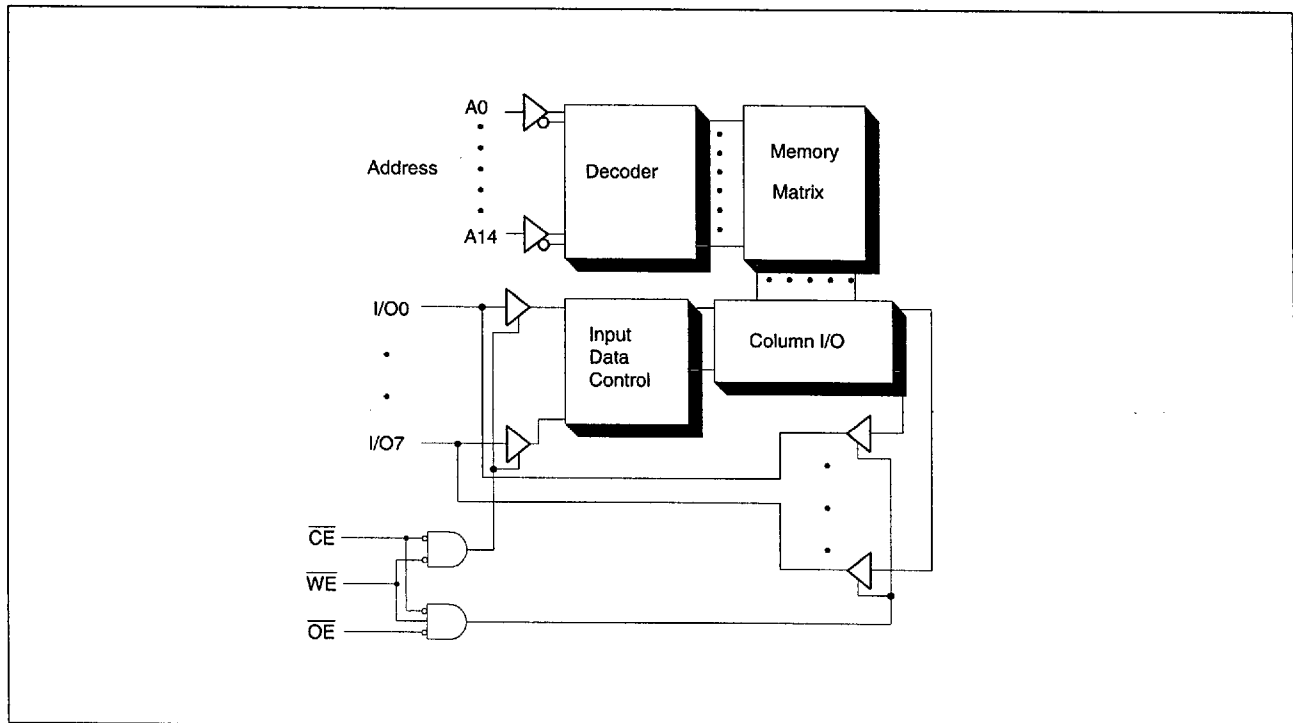
The N341256L is a high performance CMOS static RAM organized as 32,768 x 8bits.

Writing is accomplished when the  $\overline{WE}$  and  $\overline{CE}$  inputs are both Low.

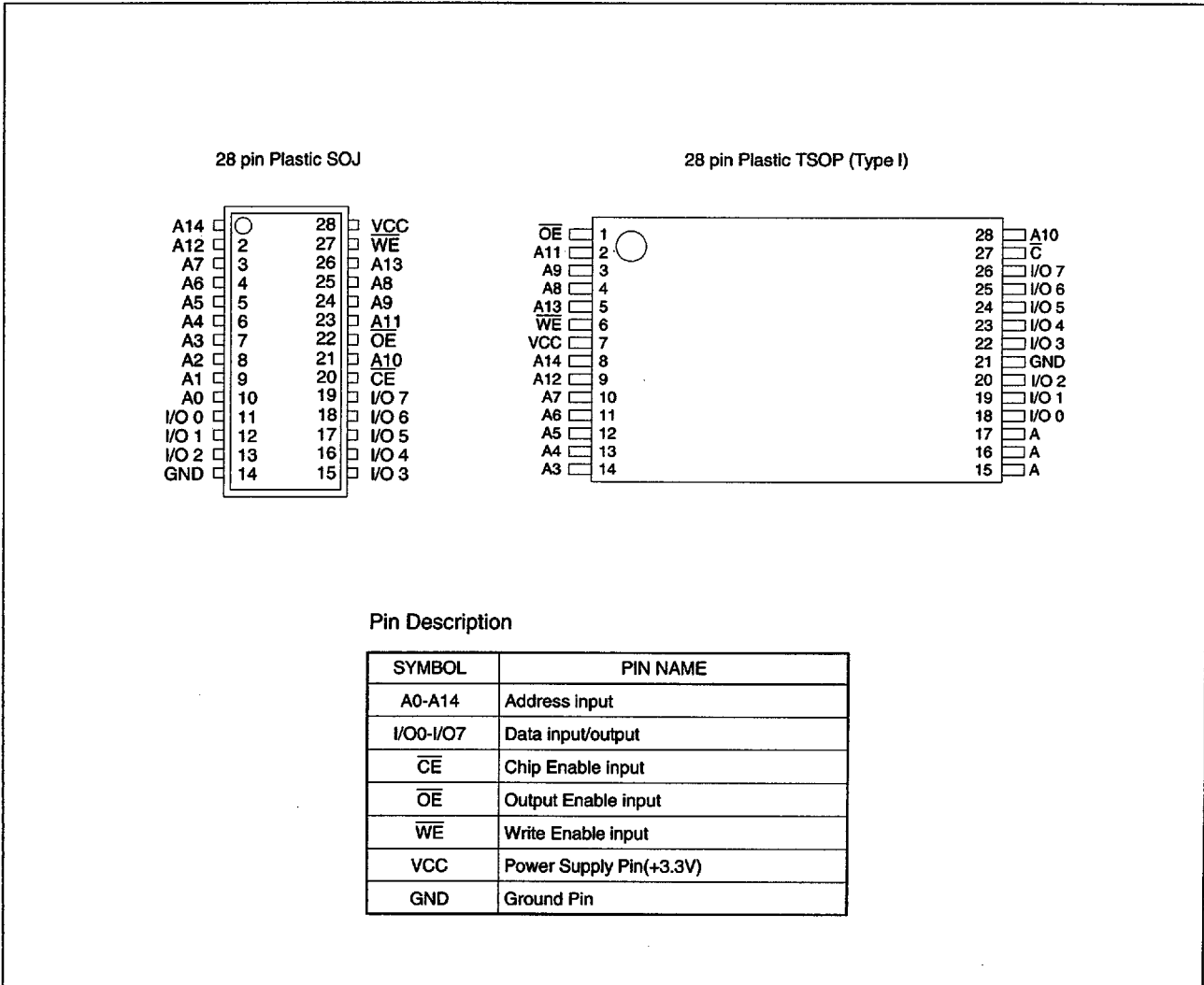
Reading is accomplished when the  $\overline{WE}$  input is High and the  $\overline{CE}$  and  $\overline{OE}$  inputs are both Low.

The N341256L operates from a single +3.3V power supply and all inputs and outputs are fully TTL compatible.

#### ■ Functional Block Diagram



■ Pin Configuration



■ Mode Selection Table

OE	WE	CE	I/O	MODE
X	X	High	High-Z	Standby
Low	High	Low	Data out	Read Cycle
X	Low	Low	Data in	Write Cycle
High	High	Low	High-Z	Output disable

Note : X = don't care.

■ **Absolute Maximum Ratings**

Symbol	Parameter	Value	Unit
VCC	Supply Voltage	-0.5 to 4.6	V
VTERM	Terminal Voltage with Respect to GND	-0.5 to VCC+0.5 (Max. 4.6)	V
TOPR	Operating Temperature	0 to 70	°C
TSTG	Storage Temperature	-55 to 150	°C
PD	Power Dissipation	1.0	W

**NOTICE**

Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

■ **Recommended Operating Conditions**

Recommended Operating Temperature and Supply Voltage

Ambient Temperature	GND	Vcc
0 to 70°C	0V	3.3V ± 0.3V

Recommended DC Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
VIH	Input High Voltage	2.0	-	VCC+0.3	V
VIL	Input Low Voltage	-0.3	-	0.8	V

Note : VIL(min) = -2.0V for pulse width less than 10ns.

■ **Capacitance**

(TOPR=25°C, f=1.0MHz)

Symbol	Parameter	Condition	Max.	Unit
CIN	Input Capacitance	VIN=0V	8	pF
COU	Output Capacitance	VOUT=0V	8	pF

Note : These parameters are sampled and not 100% tested.

■ DC Electrical Characteristics

Power Supply Currents (VCC=3.3V ± 0.3V, TOPR=0 to 70°C)

Symbol	Parameter	N341256L -15	Unit
I <sub>CC</sub>	Dynamic Operating Current $\overline{CE} \leq V_{IL}, V_{CC} = \max, f = f_{max}, I_{OUT} = 0mA, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}$	90	mA
I <sub>SB</sub>	Standby Power Supply Current (TTL level) $\overline{CE} \geq V_{IH}, V_{CC} = \max, f = f_{max}, V_{IN} \geq V_{IH} \text{ or } \leq V_{IL}$	25	mA
I <sub>SB1</sub>	Full Standby Power Supply Current (CMOS level) $\overline{CE} \geq V_{CC}-0.2V, V_{CC} = \max, f = 0, V_{IN} \leq 0.2V \text{ or } \geq V_{CC}-0.2V$	1	mA

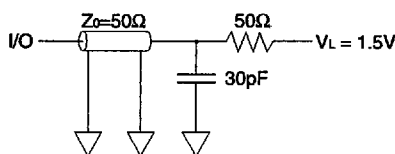
Note : All values are the maximum guaranteed values.

DC Characteristics (VCC=3.3V ± 0.3V, TOPR=0 to 70°C)

Symbol	Parameter	Condition	N341256L		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = max, V <sub>IN</sub> = GND to V <sub>CC</sub>	-2	2	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = max, $\overline{CE} \geq V_{IH}, V_{OUT} = \text{GND to } V_{CC}$	-2	2	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 4mA, V <sub>CC</sub> = min	-	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4mA, V <sub>CC</sub> = min	2.4	-	V

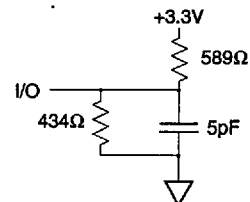
■ AC Test Conditions

Input pulse levels	GND to 3.0V
Input rise and fall times	1.5ns
Input timing reference levels	1.5V
Output timing reference levels	1.5V
Output load	See Figure 1 and 2



(Including scope and jig)

Figure 1. Output Load Equivalent



(Including scope and jig)

Figure 2. Output Load Equivalent  
(for tLZCE, tHZCE, tLZWE, tHZWE, tLZOE, tHZOE)

■ AC Electrical Characteristics

Read Cycle (VCC=3.3V ± 0.3V, TOPR=0 to 70°C)

Description	Symbol	N341256L-15		Unit
		Min.	Max.	
Read Cycle time	tRC	15		ns
Address access time	tAA		15	ns
Chip enable access time	tACE		15	ns
Output hold from address change	tOH	3		ns
Chip enable to output in Low-Z	tLZCE	5		ns
Chip disable to output in High-Z	tHZCE		5	ns
Chip enable to power up time	tPU	0		ns
Chip disable to power down time	tPD		15	ns
Output enable access time	tAOE		8	ns
Output enable to output in Low-Z	tLZOE	0		ns
Output disable to output in High-Z	tHZOE		5	ns

Note : tLZCE, tHZCE, tPU, tPD, tLZOE, and tHZOE are sampled and not 100% tested.

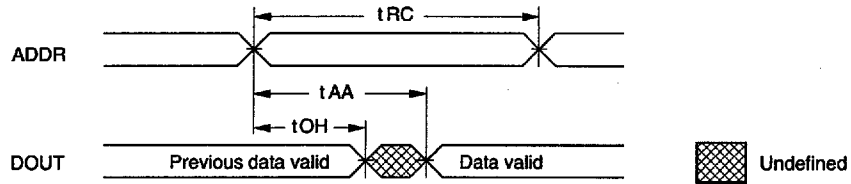
Write Cycle (VCC=3.3V ± 0.3V, TOPR=0 to 70°C)

Description	Symbol	N341256L-15		Unit
		Min.	Max.	
Write Cycle time	tWC	15		ns
Chip enable to end of write	tCW	12		ns
Address valid to end of write	tAW	12		ns
Address set-up time	tAS	0		ns
Address hold from end of write	tAH	0		ns
Write pulse width	tWP	11		ns
Data set-up time	tDS	8		ns
Data hold time	tDH	0		ns
Write disable to output in Low-Z	tLZWE	0		ns
Write enable to output in High-Z	tHZWE		3	ns

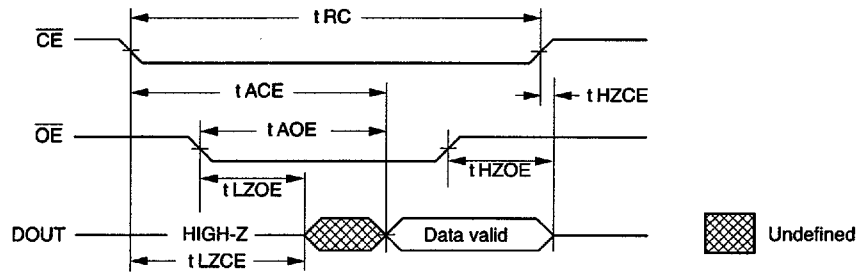
Note : tLZWE and tHZWE are sampled and not 100% tested.

■ AC Timing Waveform

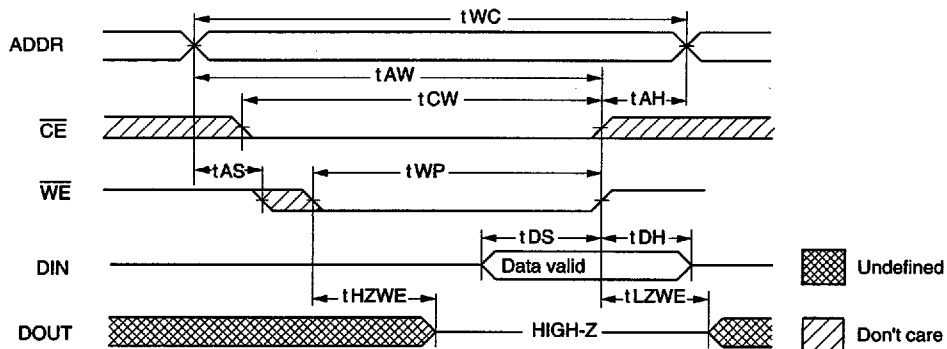
Read Cycle No.1



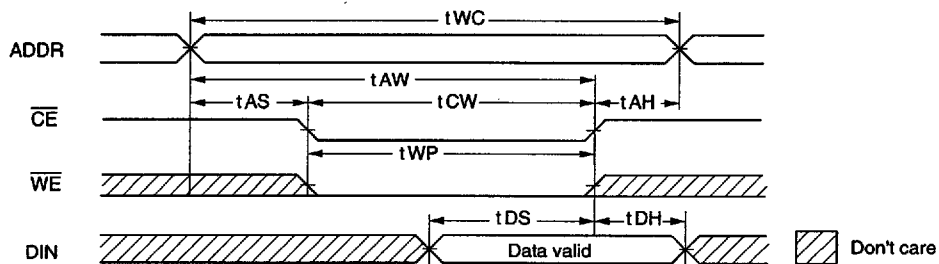
Read Cycle No.2



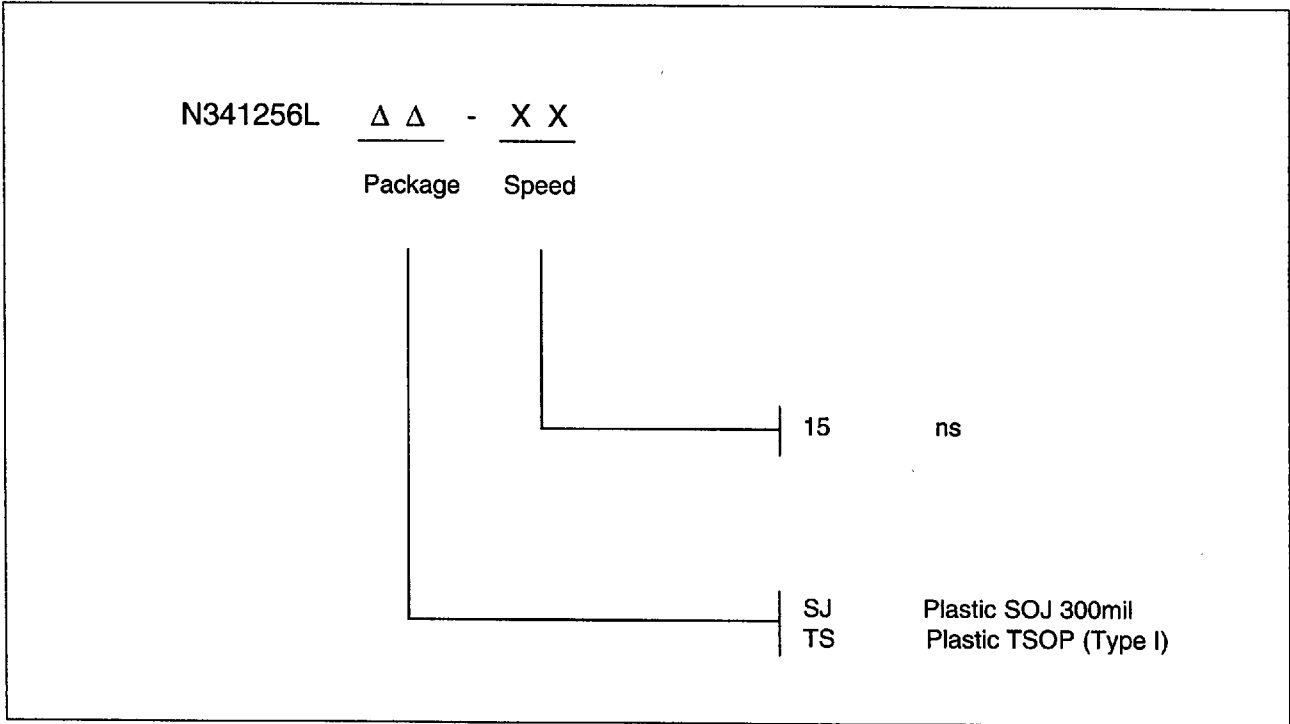
Write Cycle No.1(Write Enable Controlled)



Write Cycle No.2(Chip Enable Controlled)



■ Ordering Information



PART NO.	Access Time (ns)	Operating Current (mA)	Package
N341256LSJ-15	15	90	28Pin Plastic SOJ
N341256LTS-15	15	90	28Pin Plastic TSOP