54F/74F657

Octal Bidirectional Transceiver With 8-Bit Parity Generator/Checker and 3-State Outputs

Description

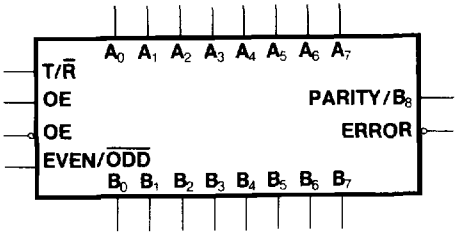
The 'F657 contains eight non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have guaranteed current sinking capability of 20 mA at the A ports and 64 mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers. Transmit (active HIGH) enables data from A ports to B ports; Receive (Active LOW) enables data from B ports to A ports. The Output Enable inputs disable both the A and B ports by placing them in a High Z condition when either the $\overline{OE}$ input is HIGH or the OE input is LOW.

The parity generator detects whether an even or odd number of bits on the A ports is HIGH, depending on the condition of the Even/$\overline{Odd}$ input. If the Even input is active HIGH and an even number of A inputs is HIGH, the Parity output is HIGH. The parity of the data received on the B ports is compared with the Even/$\overline{Odd}$ input and the Error output is LOW if not equal.

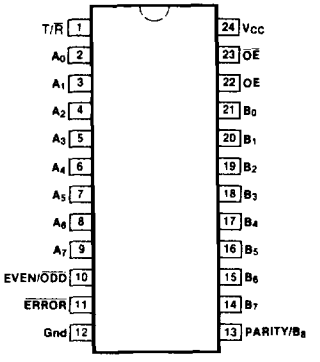
- **300 mil 24-Pin Plastic Slim Package**
- **Combines 'F245 and 'F280A Functions in One Package**
- **3-State Outputs**
- **Outputs Sink 64 mA**
- **15 mA Source Current**
- **Input Diodes for Termination Effects**

Ordering Code: See Section 5

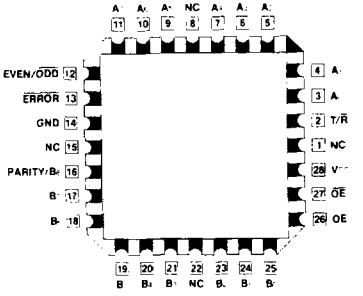
Logic Symbol



Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
A_0-A_7	Data Inputs	0.5/0.375
	Data Outputs	25/12.5
B_0-B_7	Data Inputs	0.5/0.375
	Data Outputs	25/12.5
T/$\overline{R}$	Transmit/Receive Input	0.5/0.375
$\overline{OE}$, OE	Enable Outputs	0.5/0.375
PARITY/B_8	Parity	25/12.5
E/O	Even/Odd	0.5/0.375
ERROR	Error	0.5/0.375

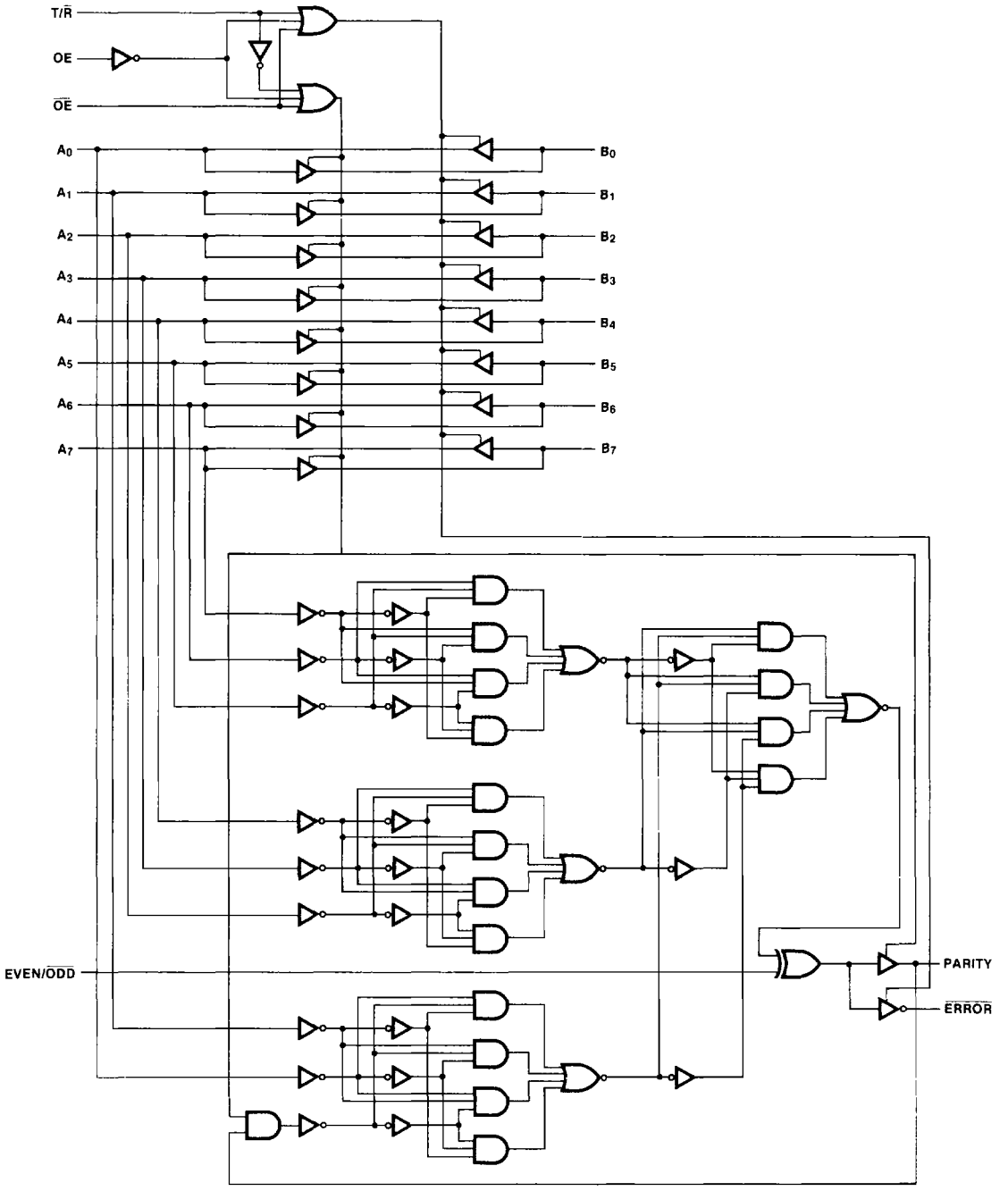
Function Table

Inputs		Output
$\overline{OE}$	T/$\overline{R}$	
L	L	Bus B Data to Bus A
L	H	Bus A Data to Bus B
H	X	High Z State

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Number of HIGH Inputs I_0-I_8	Parity	
	Even	Odd
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		120	165	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F			54F		74F		Units	Fig. No.
		T_A = +25°C V_{CC} = +5.0 V C_L = 50 pF			T_A, V_{CC} = Mil C_L = 50 pF		T_A, V_{CC} = Com C_L = 50 pF			
		Min	Typ	Max	Min	Max	Min	Max		
t_{PLH} t_{PHL}	Propagation Delay A_n to B_n or B_n to A_n		5.5 6.0						ns	3-1 3-7 3-8
t_{PLH} t_{PHL}	Propagation Delay A_n to Parity		14.0 15.5							
t_{PZH} t_{PZL}	Output Enable Time		7.0 10.0						ns	3-1 3-12 3-13
t_{PHZ} t_{PLZ}	Output Disable Time		6.5 5.0							