

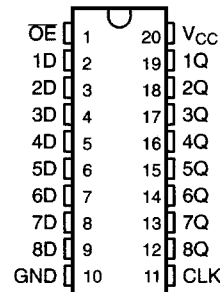
SN74LV574

OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

MARCH 1993

- **Space-Saving Package Option:
Shrink Small-Outline Package (DB)
Features EIAJ 0.65-mm Lead Pitch**
- **EPIC™ (Enhanced-Performance Implanted
CMOS) 2- μ m Process**
- **Typical V_{OLP} (Output Ground Bounce)
< 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **Typical V_{OHV} (Output V_{OH} Undershoot)
> 2 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$**
- **ESD Protection Exceeds 2000 V Per
MIL-STD-883C, Method 3015; Exceeds
200 V Using Machine Model (C = 200 pF,
R = 0)**
- **Latch-Up Performance Exceeds 250 mA
Per JEDEC Standard JESD-17**
- **Package Options Include Plastic
Small-Outline and Thin Shrink
Small-Outline Packages**

DB, DW, OR PW PACKAGE
(TOP VIEW)



description

This octal edge-triggered D-type flip-flop is designed for 2.7-V to 3.6-V V_{CC} operation.

The SN74LV574 features 3-state outputs designed specifically for driving highly capacitive or relatively low-impedance loads. It is particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

On the positive transition of the clock (CLK) input, the Q outputs are set to the logic levels that were set up at the data (D) inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without need for interface or pullup components.

The output-enable (\overline{OE}) input does not affect the internal operations of the flip-flops. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

The SN74LV574 is packaged in TI's shrink small-outline package (DB), which provides the same I/O pin count and functionality of standard small-outline packages in less than half the printed-circuit-board area.

The SN74LV574 is characterized for operation from -40°C to 85°C .

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	L	X	Q_0
H	X	X	Z

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PRODUCT PREVIEW Information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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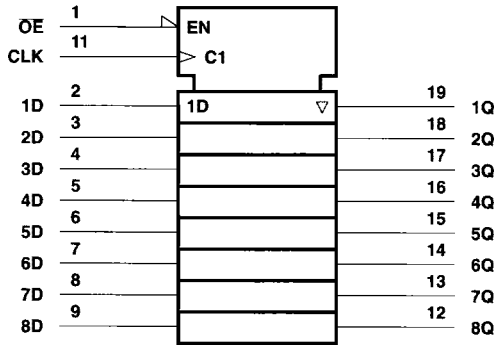
PRODUCT PREVIEW

SN74LV574

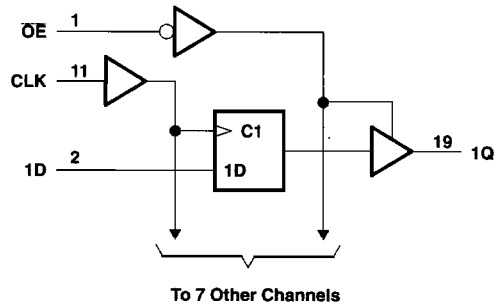
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MARCH 1993

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

PRODUCT PREVIEW

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to $V_{CC} + 0.5$ V
Output voltage range, V_O (see Notes 1 and 2)	-0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} or GND pins	± 70 mA
Maximum power dissipation at $T_A = 55^\circ\text{C}$ (in still air):	
DB package	0.5 W
DW package	0.85 W
PW package	0.5 W
Storage temperature range	-65°C to 150°C

‡ Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
2. This value is limited to 4.6 V maximum.

recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	2.7	3.3	3.6	V
V_{IH}	High-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		2	V
V_{IL}	Low-level input voltage	$V_{CC} = 2.7$ V to 3.6 V		0.8	V
V_I	Input voltage	0		V_{CC}	V
V_O	Output voltage	0		V_{CC}	V
I_{OH}	High-level output current			-8	mA
I_{OL}	Low-level output current			8	mA
$\Delta t/\Delta v$	Input transition rise or fall rate	0		100	ns/V
T_A	Operating free-air temperature	-40		85	$^\circ\text{C}$

NOTE 3: Unused or floating inputs must be held high or low.

TEXAS
INSTRUMENTS

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SN74LV574
**OCTAL EDGE-TRIGGERED D-TYPE FLIP-FLOP
 WITH 3-STATE OUTPUTS**
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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}^\dagger	MIN	TYP	MAX	UNIT
V_{IK}	$I_I = -18 \text{ mA}$	2.7 V			-1.5	V
V_{OH}	$I_{OH} = -100 \mu\text{A}$	MIN to MAX	$V_{CC} - 0.2$			V
	$I_{OH} = -6 \text{ mA}$	3 V	2.4			
V_{OL}	$I_{OL} = 100 \mu\text{A}$	MIN to MAX			0.2	V
	$I_{OL} = 6 \text{ mA}$	3 V			0.4	
I_I	$V_I = V_{CC}$ or GND	3.6 V			± 1	μA
I_{OZ}	$V_O = V_{CC}$ or GND	3.6 V			± 5	μA
I_{CC}	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6 V			20	μA
ΔI_{CC}	$V_{CC} = 3 \text{ V to } 3.6 \text{ V}$, Other inputs at V_{CC} or GND				500	μA
C_i	$V_I = V_{CC}$ or GND	3.3 V		TBD		pF
C_o	$V_O = V_{CC}$ or GND	3.3 V		TBD		pF

[†] For conditions shown as MIN or MAX, use the appropriate values under recommended operating conditions.

PRODUCT PREVIEW

