255MHz, Low Jitter, Crystal Oscillator -to- 3.3V LVPECL Frequency Synthesizer

ICS8431-11

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES APRIL 25, 2015

DATASHEET

General Description

The ICS8431-11 is a general purpose clock frequency synthesizer for IA64/32 application and a member of the HiPerClockS™ family of High Performance Clock Solutions from ICS. The VCO operates at a frequency range of 250MHz to 510MHz providing an output frequency range of 125MHz to 255MHz. The output frequency can be programmed using the parallel interface, M0 through M8, to the configuration logic. Spread spectrum clocking is programmed via the control inputs SSC_CTL0 and SSC_CTL1.

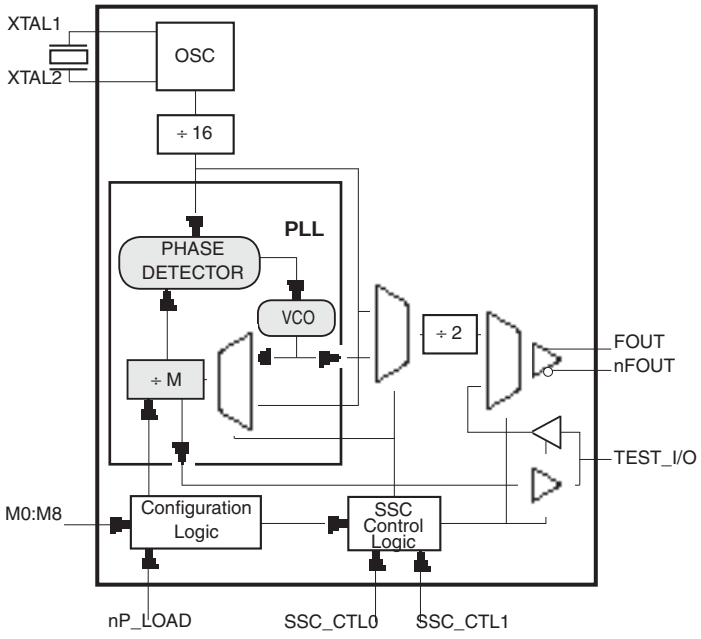
Programmable features of the ICS8431-11 support four operational modes. The four modes are spread spectrum clocking (SSC), non-spread spectrum clock and two test modes which are controlled by the SSC_CTL[1:0] pins. Unlike other synthesizers, the ICS8431-11 can immediately change spread-spectrum operation without having to reset the device.

In SSC mode, the output clock is modulated in order to achieve a reduction in EMI. In one of the PLL bypass test modes, the PLL is disconnected as the source to the differential output allowing an external source to be connected to the TEST_I/O pin. This is useful for in-circuit testing and allows the differential output to be driven at a lower frequency throughout the system clock tree. In the other PLL bypass mode, the oscillator divider is used as the source to both the M and the Fout divide by 2. This is useful for characterizing the oscillator and internal dividers.

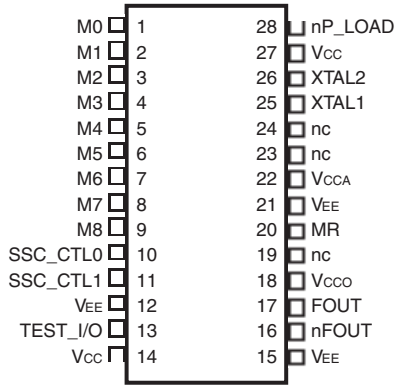
Features

- Fully integrated PLL
- Differential 3.3V LVPECL output
- Crystal oscillator interface
- Output frequency range: 125MHz to 255MHz
- Crystal input frequency range: 14MHz to 20MHz
- VCO range: 250MHz to 510MHz
- Programmable PLL loop divider for generating a variety of output frequencies
- Spread Spectrum Clocking (SSC) fixed at 1/2% modulation for environments requiring ultra low EMI
- PLL bypass modes supporting in-circuit testing and on-chip functional block characterization
- Cycle-to-cycle jitter: 30ps (maximum)
- 3.3V supply voltage
- Lead-Free package available
- 0°C to 85°C ambient operating temperature

Block Diagram



Pin Assigment



ICS8431-11
28-Lead SOIC
7.5mm x 18.05mm x 2.25mm package body
M Package
Top View

Functional Description

The ICS8431-11 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 16MHz series-resonant, fundamental crystal is used as the input to the on-chip oscillator. The output of the oscillator is divided by 16 prior to the phase detector. With a 16MHz crystal this provides a 1MHz reference frequency. The VCO of the PLL operates over a range of 250MHz to 510MHz. The output of the M divider is also applied to the phase detector.

The phase detector and the M divider force the VCO output frequency to be M times the reference frequency by adjusting the VCO control voltage. Note that for some values of M (either too high or too low), the PLL will not achieve lock. The output of the VCO is scaled by a divider prior to being sent to the LVPECL output buffer. The divider provides a 50% output duty cycle.

The programmable features of the ICS8431-11 support four output operational modes and a programmable M divider and output divider. The four output operational modes are spread spectrum clocking (SSC), non-spread spectrum clock and two test modes and are controlled by the SSC_CTL[1:0] pins.

The PLL loop divider or M divider is programmed by using inputs M0 through M8. While the nP_LOAD input is held LOW, the data present at M0:M8 is transparent to the M divider. On the LOW-to-HIGH transition of nP_LOAD, the M0:M8 data is latched into the M divider and any further changes at the M0:M8 inputs will not be seen by the M divider until the next LOW transition on nP_LOAD.

The relationship between the VCO frequency, the crystal frequency and the M divider is defined as follows:

$$fVCO = \frac{fxtal}{16} \times M$$

The M value and the required values of M0:M8 for programming the VCO are shown in *Table 3B*, Programmable VCO Frequency Function Table. The frequency out is defined as follows:

$$FOUT = \frac{fVCO}{2} = \frac{fxtal \times M}{32}$$

For the ICS8431-11, the output divider equals 2. Valid M values for which the PLL will achieve lock are defined as: $250 \leq M \leq 510$.

Table 1. Pin Descriptions

Number	Name	Type		Description
1, 2, 3, 4, 5, 6, 7	M0-M6	Input	Pulldown	M divider inputs. Data latched on LOW-to-HIGH transistion of nP_LOAD input. LVCMOS / LVTTL pins interface levels.
8, 9	M7-M8	Input	Pullup	
10, 11	SSC CTL0, SSC CTL1	Input	Pullup	SCC control pins. LVTTL / LVCMOS interface levels.
12, 15, 21	V_{EE}	Power		Negative supply pins. Connect all V_{EE} pins to board ground.
13	TEST I/O	Input / Output		Programmed as input in PLL bypass mode.
14, 27	V_{CC}	Power		Core supply pins.
16, 17	nFOUT, FOUT	Output		Differential outputs for the synthesizer. 3.3V LVPECL interface levels.
18	V_{CCO}	Power		Output supply pin.
19, 23, 24	nc	Unused		No connect.
20	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true output FOUT to go low and the inverted output nFOUT to go high. When logic LOW, the internal dividers and the outputs are enabled. Assertion of MR does not effect loaded M and T values. LVCMOS / LVTTL interface levels.
22	V_{CCA}	Power		Analog supply pin.
25, 26	XTAL1, XTAL2	Input		Crystal oscillator interface. XTAL1 is the input. XTAL2 is the output.
28	nP_LOAD	Input	Pulldown	Parallel load input. Determines when data present at M8:M0 is loaded into M divider. LVTTL / LVCMOS interface levels.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Pin Capacitance			4		pF
R_{PULLUP}	Input Pullup Resistor			51		KΩ
$R_{PULLDOWN}$	Input Pulldown Resistor			51		KΩ

Table 3A. SSC Control Input Function Table

Inputs		TEST_I/O Source	SSC	Outputs		Operational Modes
SSC_CTL1	SSC_CTL0			FOUT, nFOUT	TEST_I/O	
0	0	Internal	Disabled	fXTAL ÷ 32	fXTAL ÷ 16 ÷ M	PLL bypass; oscillator, M and N dividers test mode. NOTE 1
0	1	PLL	Enabled	$\frac{fXTAL \times M}{32}$	Hi-Z	Default SSC; Modulation Factor = ½ Percent
1	0	External	Disabled	Test Clk	Input	PLL Bypass Mode, (1MHz≤ Test Clk ≤ 200MHz); NOTE 1
1	1	PLL	Disabled	$\frac{fXTAL \times M}{32}$	Hi-Z	No SSC Modulation

NOTE 1: Used for in house debug and characterization.

Table 3B. Programmable VCO Frequency Function Table (NOTE 1)

VCO Frequency (MHz)	M Count	256	128	64	32	16	8	4	2	1
		M8	M7	M6	M5	M4	M3	M2	M1	M0
250	250	0	1	1	1	1	1	0	1	0
251	251	0	1	1	1	1	1	0	1	1
252	252	0	1	1	1	1	1	1	0	0
253	253	0	1	1	1	1	1	1	0	1
•	•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•	•
508	508	1	1	1	1	1	1	1	0	0
509	509	1	1	1	1	1	1	1	0	1
510	510	1	1	1	1	1	1	1	1	0

NOTE 1: Assumes a 16MHz crystal.

Absolute Maximum Ratings

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	46.2°C/W (0 lfpm)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 4A. Power Supply DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				140	mA

Table 4B. LVCMOS / LVTTL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 85°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage	M0:M8, SSC_CTL0, SSC_CTL1, MR, TEST_I/O, nP_LOAD	$3.135V \le V_{CC} \le 3.465V$	2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage	M0:M8, SSC_CTL0, SSC_CTL1, MR, TEST_I/O, nP_LOAD	$3.135V \le V_{CC} \le 3.465V$	-0.3		0.8	V
I_{IH}	Input High Current	M7, M8, SSC_CTL0, SSC_CTL1, TEST_IO	$V_{CC} = V_{IN} = 3.465V$			5	µA
		M0:M6, nP_LOAD, MR	$V_{CC} = V_{IN} = 3.465V$			150	µA
I_{IL}	Input Low Current	M7, M8, SSC_CTL0, SSC_CTL1, TEST_IO	$V_{CC} = 3.465V, V_{IN} = 0V$	-150			µA
		M0:M6, nP_LOAD, MR	$V_{CC} = 3.465V, V_{IN} = 0V$	-5			µA

Table 4C. LVPECL DC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 85°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 1.0	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		600	700	850	mV

NOTE 1: Output terminated with 50Ω to V_{CCO} - 2V. See Parameter Measurement Section, 3.3V Output Load Test Circuit.

Table 5. Crystal Characteristics

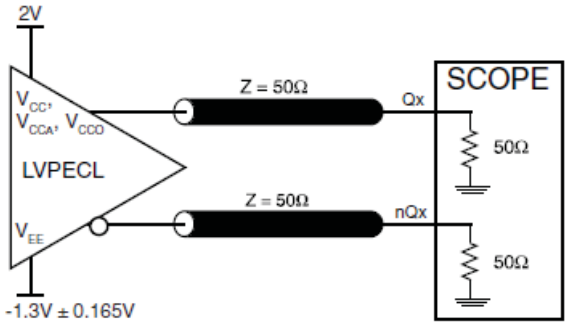
Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency			16.0		MHz
Equivalent Series Resistance (ESR)				40	Ω
Shunt Capacitance		3		7	pF

Table 6. AC Characteristics, $V_{CC} = V_{CCA} = V_{CCO} = 3.3V±5\%$, T_A = 0°C to 85°C

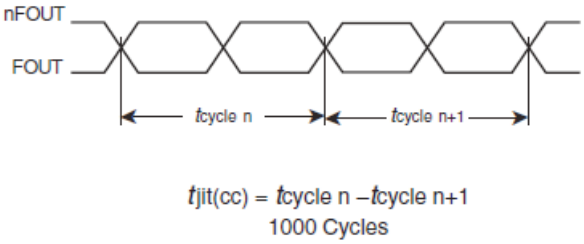
Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
F_{ave}	Average Output Frequency; NOTE 1		-750		+750	ppm
tjit(cc)	Cycle-to-Cycle Jitter; NOTE 2, 6	F_{OUT} = 200MHz		18	30	ps
					35	ps
odc	Output Duty Cycle		47		53	%
t_R / t_F	Output Rise/Fall Time	20% to 80%	300	450	600	ps
F_{xtal}	Crystal Input Range; NOTE 3, 4		14	16	20	MHz
F_M	SSC Modulation Frequency; NOTE 5		30		33.33	KHz
F_{MF}	SSC Modulation Factor; NOTE 5			0.4	0.6	%
SSC_{red}	Spectral Reduction; NOTE 5		7	10		dB
t_{STABLE}	Power-up to Stable Clock Output				10	ms

See Figures in the Parameter Measurement Information section.
NOTE 1: Without external crystal components.
NOTE 2: Jitter performance using XTAL inputs.
NOTE 3: Only valid within the VCO operating range.
NOTE 4: For XTAL input, refer to Application Note.
NOTE 5: Spread Spectrum clocking enabled.
NOTE 6: This parameter is defined in accordance with JEDEC Standard 65.

Parameter Measurement Information

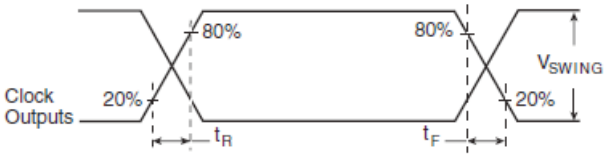


3.3V Output Load AC Test Circuit

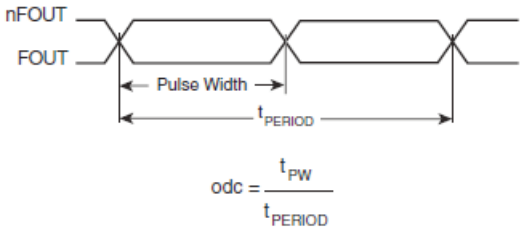


$t_{jit(cc)} = t_{cycle\ n} - t_{cycle\ n+1}$
1000 Cycles

Cycle-to-Cycle Jitter



Output Rise/Fall Time



$$odc = \frac{t_{PW}}{t_{PERIOD}}$$

Output Duty Cycle/Pulse Width/Period

Application Information

Crystal Input and Oscillator Interface

The ICS8431-11 features an internal oscillator that uses an external quartz crystal as the source of its reference frequency. A 16MHz crystal divided by 16 before being sent to the phase detector provides the reference frequency. The oscillator is a series resonant, multi-vibrator type design. This design provides better stability and eliminates the need for large on chip capacitors. Though a series resonant crystal is preferred, a parallel resonant crystal can be used. A parallel resonant mode crystal used in a series resonant circuit will exhibit a frequency of oscillation a few hundred ppm lower than specified. A few hundred ppm translates to KHz inaccuracy. In general computing applications this level of inaccuracy is irrelevant. If better ppm accuracy is required, an external capacitor can be added to a parallel resonant crystal in series to pin 25. *Figure 1A* shows how to interface with a crystal.

Figures 1A, 1B, and 1C show various crystal parameters which are recommended only as guidelines. *Figure 1A* shows how to interface a capacitor with an 18pF parallel resonant crystal. *Figure 1B* shows the capacitor value needed for the optimum ppm performance over various parallel resonant crystals. *Figure 1C* shows the recommended tuning capacitance for a various parallel resonant crystal.

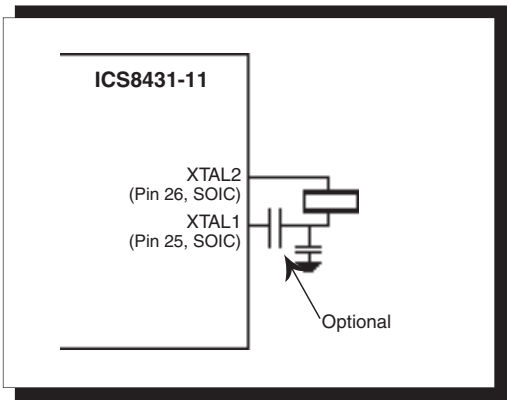


Figure 1A. Crystal Interface

Figure 1B. Recommended tuning capacitance for various 18pF parallel resonant crystals.

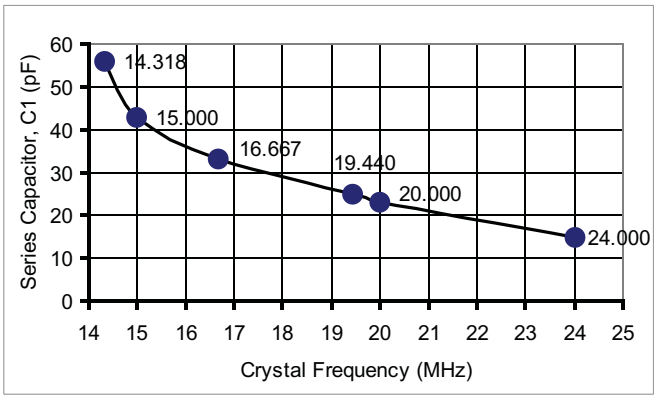
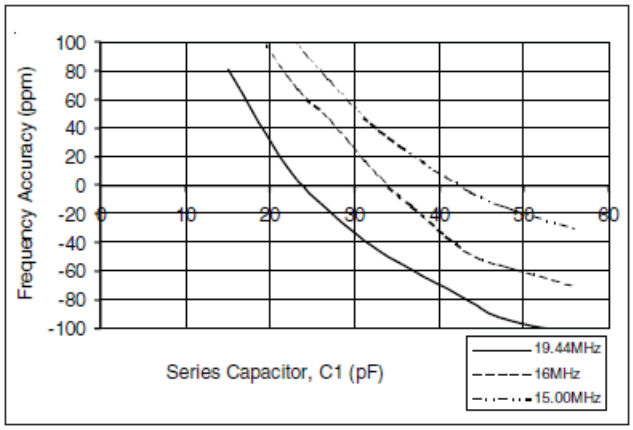


Figure 1C. Recommended tuning capacitance for various 18pF parallel resonant crystals.



Spread Spectrum

Spread-spectrum clocking is a frequency modulation technique for EMI reduction. When spread-spectrum is enabled, a 30KHz triangle waveform is used with 0.5% down-spread (+0.0% / -0.5%) from the nominal 200MHz clock frequency. An example of a triangle frequency modulation profile is shown in *Figure 2A* below. The ramp profile can be expressed as:

- Fnom = Nominal Clock Frequency in Spread OFF mode (200MHz with 16MHz IN)
- Fm = Nominal Modulation Frequency (30KHz)
- δ = Modulation Factor (0.5% down spread)

$(1 - \delta)$ fnom + 2 fm x δ x fnom x t when $0 < t < \frac{1}{2\ fm}$,

$(1 - \delta)$ fnom - 2 fm x δ x fnom x t when $\frac{1}{2\ fm} < t < \frac{1}{fm}$

The ICS8431-11 triangle modulation frequency deviation will not exceed 0.6% down-spread from the nominal clock frequency (+0.0%/-0.5%). An example of the amount of down spread relative to the nominal clock frequency can be seen in the frequency domain, as shown in *Figure 2B.* The ratio of this width to the fundamental frequency is typically 0.4%, and will not exceed 0.6%. The resulting spectral reduction will be greater than 7dB, as shown in Figure 2B. It is important to note the ICS8431-11 7dB minimum spectral reduction is the component-specific EMI reduction, and will not necessarily be the same as the system EMI reduction.

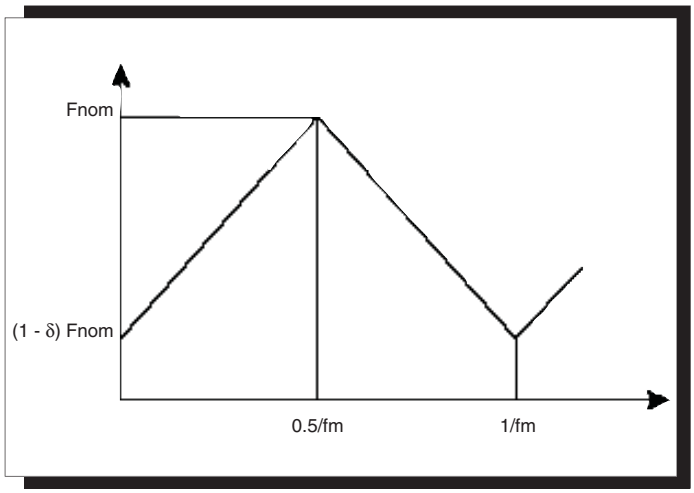


Figure 2A. Triangle Frequency Modulation

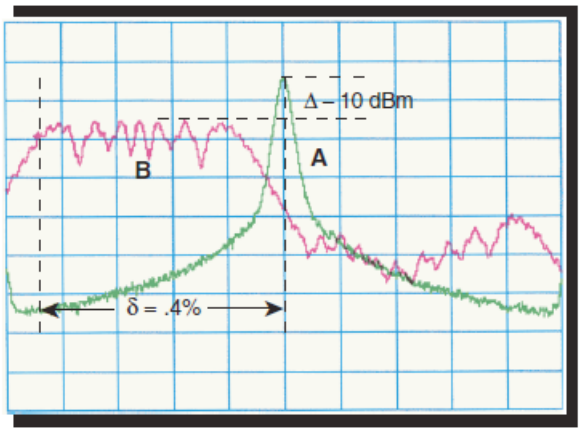


Figure 2B. 200MHz Clock Output in Frequency Domain
(A) Spread-Spectrum OFF
(B) Spread-Spectrum ON

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8431-11 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA}, and V_{CCO} should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, better power supply isolation is required. *Figure 3* illustrates how a 10Ω along with a 10µF and a .01µF bypass capacitor should be connected to each V_{CCA} pin.

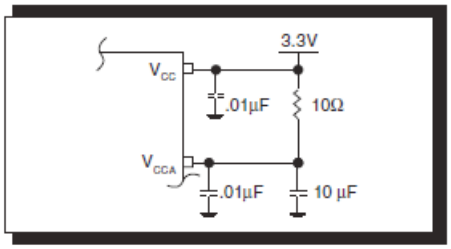


Figure 3. Power Supply Filtering

Termination for LVPECL Outputs

The clock layout topology shown below is typical for IA64/32 platforms. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

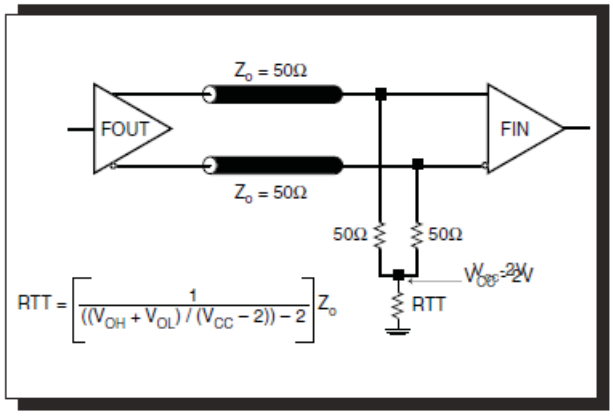


Figure 4A. LVPECL Output Termination

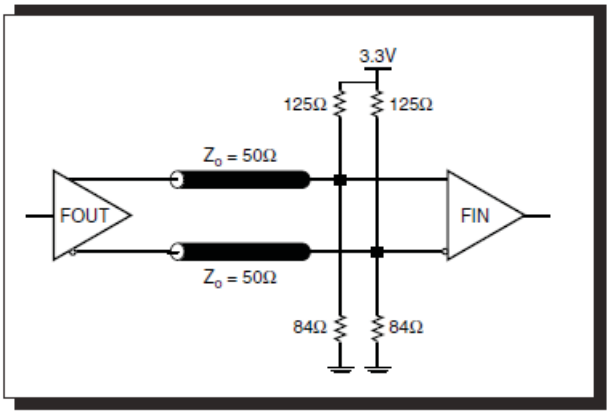


Figure 4B. LVPECL Output Termination

Layout Guideline

The schematic of the ICS8431-11 layout example used in this layout guideline is shown in *Figure 5A*. The ICS8431-11 recommended PCB board layout for this example is shown in *Figure 5B*. This layout example is used as a general guideline. The layout in the actual system will depend on the selected component types, the density of the components, the density of the traces, and the stack up of the P.C. board.

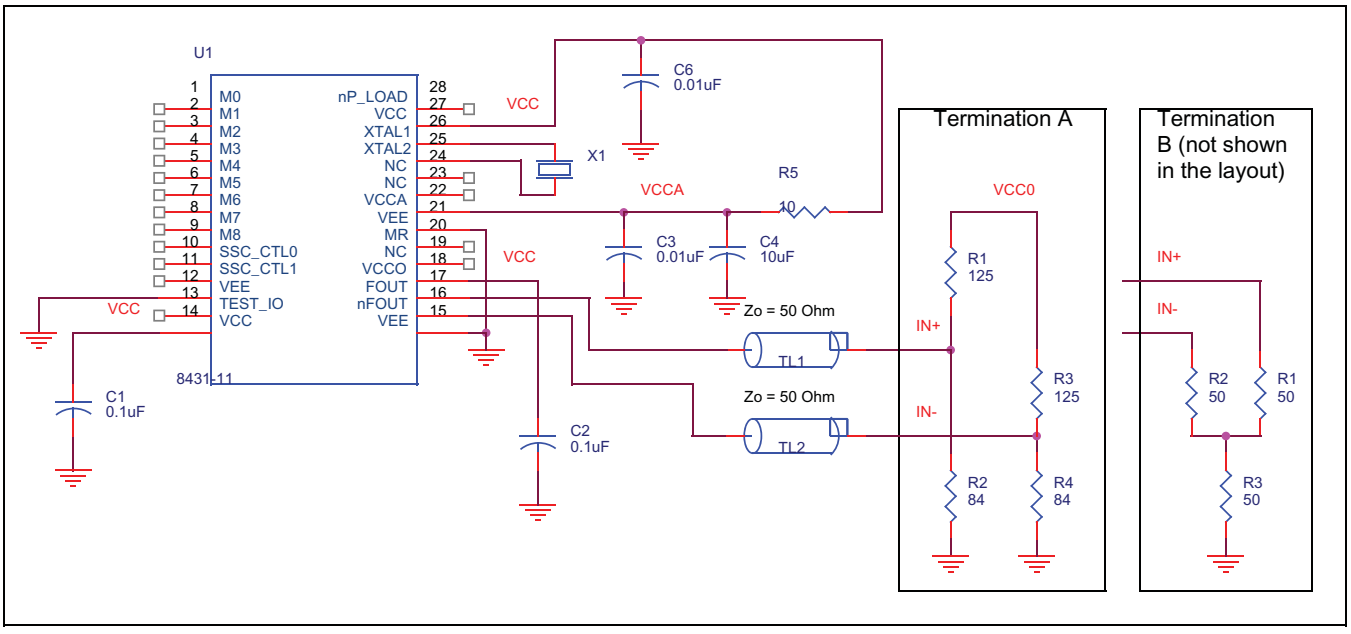


Figure 5A. Recommended Schematic Layout

The following component footprints are used in this layout example:

All the resistors and capacitors are size 0603.

Power and Grounding

Place the decoupling capacitors C1, C2, C3, C4, and C6, as close as possible to the power pins. If space allows, placment of the decoupling capacitor on the component side is preferred. This can reduce unwanted inductance between the decoupling capacitor and the power pin generated by the via.

Maximize the power and ground pad sizes and number of vias capacitors. This can reduce the inductance between the power and ground planes and the component power and ground pins.

The RC filter consisting of R5, C3, and C4 should be placed as close to the V_{CCA} pin as possible.

Clock Traces and Termination

Poor signal integrity can degrade the system performance or cause system failure. In synchronous high-speed digital systems, the clock signal is less tolerant to poor signal integrity than other signals. Any ringing on the rising or falling edge or excessive ring back can cause system failure. The shape of the trace and the trace delay might be restricted by the available space on the board and the component location. While routing the traces, the clock signal traces should be routed first and should be locked prior to routing other signal traces.

- The differential 50Ω output traces should have same length.
- Avoid sharp angles on the clock trace. Sharp angle turns cause the characteristic impedance to change on the transmission lines.
- Keep the clock traces on the same layer. Whenever possible, avoid placing vias on the clock traces. Placement of vias on the traces can affect the trace characteristic impedance and hence degrade signal integrity.
- To prevent cross talk, avoid routing other signal traces in parallel with the clock traces. If running parallel traces is unavoidable, allow a separation of at least three trace widths between the differential clock trace and the other signal trace.
- Make sure no other signal traces are routed between the clock trace pair.
- The matching termination resistors should be located as close to the receiver input pins as possible.

The matching termination resistors R1, R2, R3 and R4 should be located as close to the receiver input pins as possible. Other termination scheme can also be used but is not shown in the example.

Crystal

The crystal X1 should be located as close as possible to the pins 25 (XTAL1) and 26 (XTAL2). The trace length between the X1 and U1 should be kept to a minimum to avoid unwanted parasitic inductance and capacitance. Other signal traces should not be routed near the crystal traces.

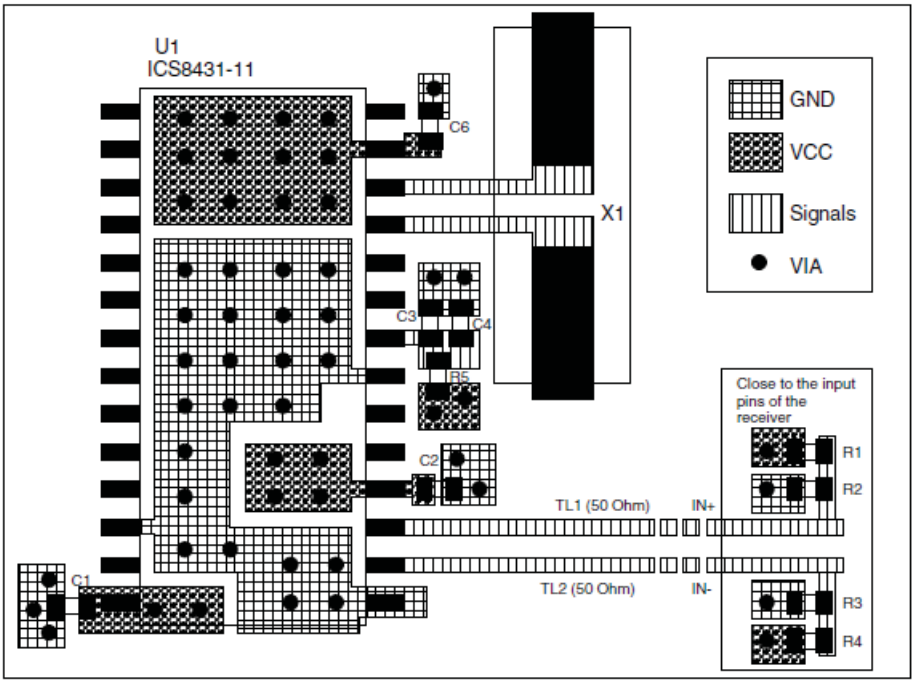


Figure 5B. PCB Board Layout For ICS8431-11

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS8431-11.
Equations and example calculations are also provided.

1. Power Dissipation.
The total power dissipation for the ICS8431-11 is the sum of the core power plus the power dissipated in the load(s).
The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.
NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)$_{MAX}$ = V_{CC_MAX} * I_{EE_MAX} = 3.465V * 140mA = **485.1mW**
- Power (outputs)$_{MAX}$ = **30.2mW/Loaded Output pair**
  If all outputs are loaded, the total power is 1 * 30.2mW = **30.2mW**

Total Power$_{_MAX}$ (3.465V, with all outputs switching) = 485.1mW + 30.2mW = **515.3mW**

2. Junction Temperature.
Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device.
The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)
T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 39.7°C/W per Table 7 below.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:
85°C + 0.515W * 39.7°C/W = 105.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 7. Thermal Resistance θ_{JA} for 28-pin SOIC, Forced Convection

θ_{JA} by Velocity (Linear Feet per Minute)	0	200	500
Single-Layer PCB, JEDEC Standard Test Boards	76.2°C/W	60.8°C/W	53.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 6.*

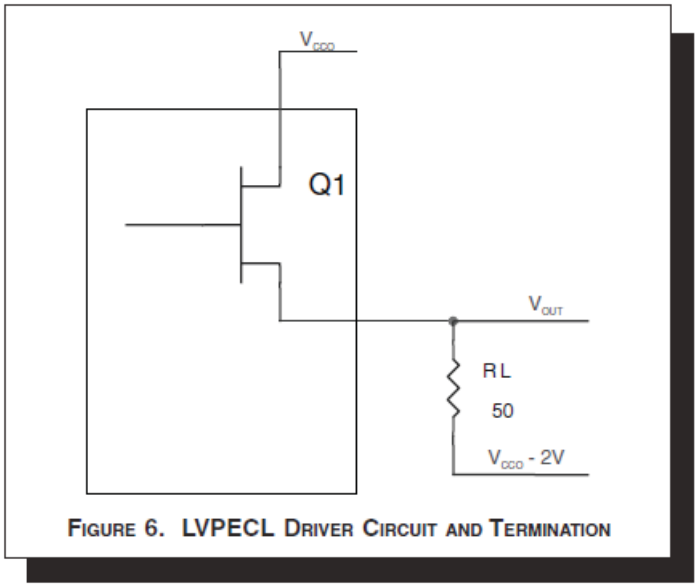


Figure 6. LVPECL Driver Circuit and Termination

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 1.0V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{1.0V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 1V)/50\Omega] * 1V =$ **20.0mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30.2mW**

Reliability Information

Table 8. θ_{JA} vs. Air Flow Table for 28 Lead SOIC

θ_{JA} by Velocity (Linear Feet per Minute)			
	0	**200**	**500**
Single-Layer PCB, JEDEC Standard Test Boards	76.2°C/W	60.8°C/W	53.2°C/W
Multi-Layer PCB, JEDEC Standard Test Boards	46.2°C/W	39.7°C/W	36.8°C/W

NOTE: Most modern PCB designs use multi-layered boards. The data in the second row pertains to most designs.

Transistor Count

The transistor count for ICS8431-11 is: 5555

Package Outline - M Suffix for 28 Lead SOIC

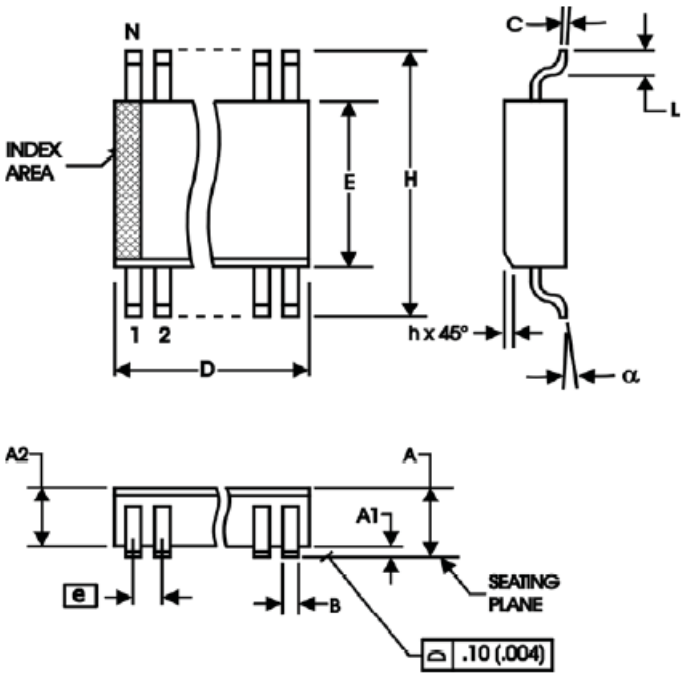


Table 9. Package Dimensions

SYMBOL	Millimeters	
	MINIMUM	MAXIMUM
N	28	
A	--	2.65
A1	0.10	--
A2	2.05	2.55
B	0.33	0.51
C	0.18	0.32
D	17.70	18.40
E	7.40	7.60
e	1.27 BASIC	
H	10.00	10.65
h	0.25	0.75
L	0.40	1.27
α	0°	8°

Reference Document: JEDEC Publication 95, MS-013, MO-119

Table 10. Ordering Information

Part/Order Number	Marking	Package	Count	Temperature
ICS8431EM-11	ICS8431EM-11	28 Lead SOIC	26 Per Tube	0°C to 85°C
ICS8431EM-11T	ICS8431EM-11	28 Lead SOIC on Tape and Reel	1000	0°C to 85°C
ICS8431EM-11LF	ICS8431EM-11LF	28 Lead “Lead-Free” SOIC	26 Per Tube	0°C to 85°C
ICS8431EM-11LFT	ICS8431EM-11LF	28 Lead “Lead-Free” SOIC on Tape and Reel	1000	0°C to 85°C

REVISION HISTORY SHEET				
Rev	**Table**	**Page**	**Description of Change**	**Date**
A	T1 T6	2 6	Revised descriptions in Pin Description table. Revised notes in AC Characteristics table. Changed V_{DDx} to V_{CCx} throughout datasheet. Updated Figures. Added Power Considerations.	12/18/01
B	T4C T5	5 6	V_{OH} parameters revised from V_{CCO}-1.28 Min., V_{CCO} - 0.98 Max. to V_{CCO} -1.4V Min., V_{CCO} - 1.0V Max. Crystal Characteristics table has been shortened. ESR row, value changed from 50Ω Max. to 70Ω Max.	1/10/02
B	T1	3 9	Updated Pin Description Table. Added 18pF description to text on Crystal input.	2/22/02
B	T1	3	Corrected pin number placement for M0:M8 pins in Pin Description Table.	3/4/02
B	T1	3	Pin Description Table, corrected description for MR pin.	6/6/02
B	T1	3	Pin Description Table, corrected description for V_{EE} pin.	6/18/02
B		1	In Features section, replaced “Average output frequency range: -750ppm to +750ppm” with “Output frequency range: 95MHz to 255MHz”.	8/7/02
B	T10	17	Ordering Information Table - updated Revision of Part/Order Number and Marking from ICS8431CM-11 to ICS8431EM-11.	9/11/02
B	T1 T4A	3 5 9	Pin Description Table - updated V_{CC} and MR descriptions. Power Supply Characteristics Table - revised V_{CC} parameter to reflect the pin description. Updated 200MHz Clock Output in Freq. Domain diagram. Updated format.	2/5/03
B	T3B	1 2 4	General Description and Features - changed Output Frequency minimum from 95MHz to 125MHz, and VCO minimum from 190MHz to 250MHz. Functional Description - changed VCO minimum from 190MHz to 250MHz. Programmable VCO Frequency Table - table was changed to reflect the VCO minimum value.	4/22/03
C	T2 T5	2 6	Pin Characteristics Table - changed CIN from 4pF max. to 4pF typical.Crystal Table - changed ESR value from 70 max. to 30 max.	6/16/03
D	T5	3 6	Absolute Maximum Ratings - changed Output rating. Crystal Table - changed ESR value from 30Ω max. to 40Ω max.	6/20/03
D	T8	14	Ordering Information Table - add Lead-Free part number.	10/21/04
D		1 18	Updated Format Product Discontinuation Notice - Last time buy expires April 25, 2015, PDN# CQ-14-03 Updated support email address	5/14/14

We've Got Your Timing Solution

www.IDT.com

6024 Silver Creek Valley Road
San Jose, California 95138

Sales
800-345-7015 (inside USA)
+408-284-8200 (outside USA)
Fax: 408-284-2775
www.IDT.com/go/contactIDT

Technical Support Sales
Clocks@idt.com
+480-763-2056