STK10C68AM

CMOS/SNOS nvSRAM
Military
High Performance
8K x 8 Non-Volatile Static RAM

PRELIMINARY

FEATURES

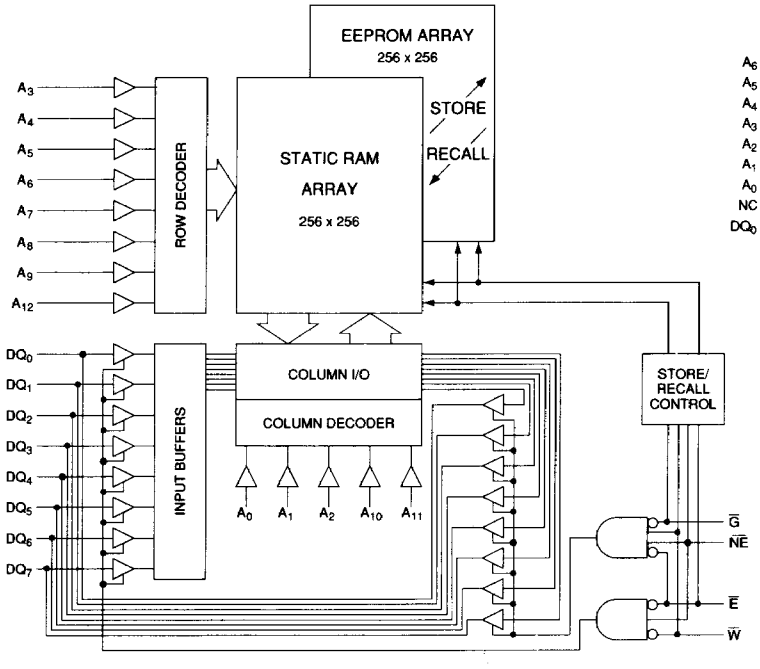
- **Non-Volatile Data Integrity**
- **45, 55 and 70ns Address Access Times**
- **45, 55 and 70ns Chip Enable Access Times**
- **Unlimited Read and Write to SRAM**
- **Unlimited Recall cycles from EEPROM**
- **10^5 Store cycles to EEPROM**
- **Hardware Store Protection**
- **Automatic Recall on Power Up**
- **Automatic Store Timing**
- **Single 5V ±10% Operation**
- **Military Temperature Range –55°C to 125°C**
- **10 year data retention in EEPROM**
- **JEDEC NVRAM pinout in 600 mil 28 pin DIP**
- **JEDEC NVRAM pinout in a 32 pin LCC**
- **Available in an industry standard 300 mil DIP**

DESCRIPTION

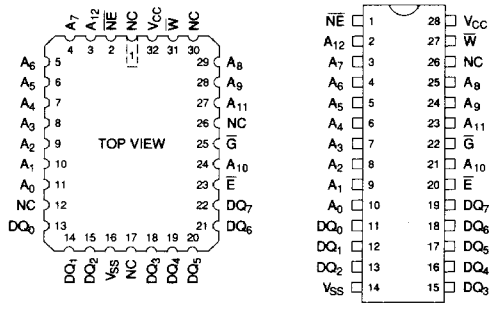
The Simtek STK10C68AM is a fast static RAM (35, 45 and 55ns), with a non-volatile electrically-erasable PROM (EEPROM) cell incorporated in each static memory cell. The SRAM can be read and written an unlimited number of times, while independent non-volatile data resides in EEPROM. Data may easily be transferred from the SRAM to the EEPROM (STORE), and from the EEPROM back to the SRAM (RECALL) using the $\overline{NE}$ pin. A RECALL also takes place upon power-up. It combines the high performance and ease of use of a fast SRAM with the data integrity of non-volatility.

The STK10C68AM features the JEDEC standard pinout for 64K non-volatile RAMs in a 28-pin 600 mil dual in line package, a 32 pin LCC or a 28-pin 300 mil DIP. will be screened to MIL-STD method 5004 and 5005. Simtek is currently establishing a military standard compliant program.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATIONS



PIN NAMES

$A_0 - A_{12}$	Address Inputs
$\overline{W}$	Write Enable
$DQ_0 - DQ_7$	Data In/Out
$\overline{E}$	Chip Enable
$\overline{G}$	Output Enable
$\overline{NE}$	Non-Volatile Enable
V_{CC}	Power (+5V)
V_{SS}	Ground

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ABSOLUTE MAXIMUM RATINGS[a]

Voltage on typical input relative to V_{SS} ..... –0.6V to 7.0V
Voltage on DQ_{0-7} and $\overline{W}$ ..... –0.5V to (V_{CC}+0.5V)
Temperature under bias ..... –55°C to 125°C
Storage temperature ..... –65°C to 150°C
Power dissipation 1W
DC output current 15mA
(One output at a time, one second duration)

Note a: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	NOTES
V_{CC}	Supply Voltage	4.5	5.0	5.5	V	
V_{IH}	Input Logic "1" Voltage	2.0		V_{CC}+.5	V	All Inputs
V_{IL}	Input Logic "0" Voltage	V_{SS}–.5		0.8	V	All Inputs
T_A	Ambient Operating Temperature	-55		125	°C	

DC ELECTRICAL CHARACTERISTICS[b,c]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{CC}	Average V_{CC} Power Supply Current		90 85 80	mA mA mA	t_{AVAV}=45ns t_{AVAV}=55ns t_{AVAV}=70ns
I_{SB_1}	V_{CC} Power Supply Current (Standby, Cycling TTL Input Levels)		19 19 19	mA mA mA	t_{AVAV}=45ns t_{AVAV}=55ns t_{AVAV}=70ns $\overline{E}$≥V_{IH} all other inputs cycling
I_{SB_2}	V_{CC} Power Supply Current (Standby, Stable CMOS Input Levels)		2	mA	$\overline{E}$≥(V_{CC}–0.2V) All other inputs at V_{IN}≤ 0.2V or ≥(V_{CC}–0.2V)
I_{ILK}	Input Leakage Current (Any Input)		±1	µA	V_{CC}=max V_{IN}=V_{SS} to V_{CC}
I_{OLK}	Off State Output Leakage Current		±5	µA	V_{CC}=max V_{IN}=V_{SS} to V_{CC}
V_{OH}	Output Logic "1" Voltage	2.4		V	I_{OUT}=–4mA
V_{OL}	Output Logic "0" Voltage		0.4	V	I_{OUT}=8mA

Note b: I_{CC} is dependent on output loading and cycle rate. The specified values are obtained with outputs unloaded.
Note c: Bringing $\overline{E}$≥V_{IH} will not produce standby currents levels until any non-volatile cycle in progress has timed out. See MODE SELECTION table.

AC TEST CONDITIONS

Input Pulse Levels	V_{SS} to 3V
Input Rise and Fall Times	≤ 5ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figure 1

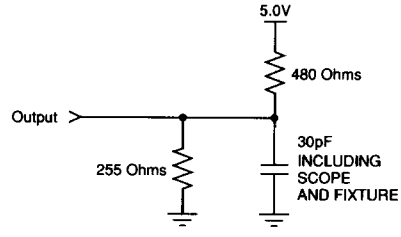

Figure 1: AC Output Loading

CAPACITANCE (T_A=25°C, f=1.0MHz)[d]

SYMBOL	PARAMETER	MAX	UNITS	CONDITIONS
C_{IN}	Input Capacitance	5	pF	ΔV=0 to 3V
C_{OUT}	Output Capacitance	7	pF	ΔV=0 to 3V

Note d: This parameter is characterized and not 100% tested.

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PRELIMINARY

SRAM MEMORY OPERATION

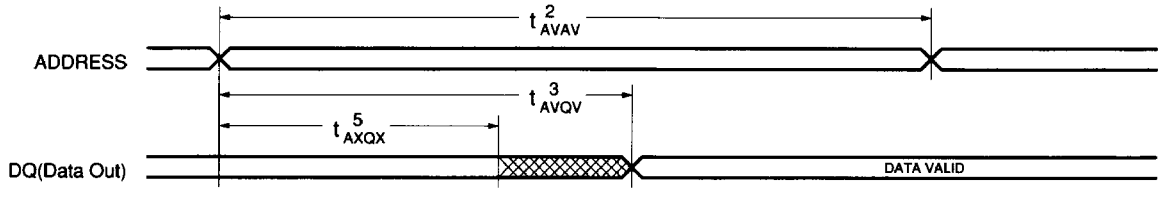
READ CYCLES 1 & 2[e]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

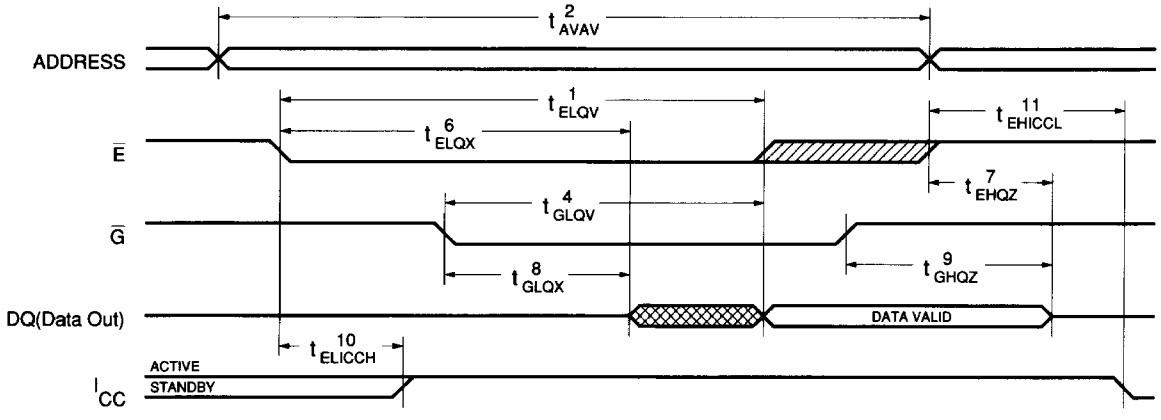
NO.	SYMBOL		PARAMETER	STK10C68AM-45		STK10C68AM-55		STK10C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{ELQV}	t_{ACS}	Chip Enable Access Time		45		55		70	ns	
2	t_{AVAV}	t_{RC}	Read Cycle Time	45		55		70		ns	f
3	t_{AVQV}	t_{AA}	Address Access Time		45		55		70	ns	g
4	t_{GLQV}	t_{OE}	Output Enable to Data Valid		20		25		30	ns	
5	t_{AXQX}	t_{OH}	Output Hold After Address Change	5		5		5		ns	
6	t_{ELQX}	t_{LZ}	Chip Enable to Output Active	5		5		5		ns	
7	t_{EHQZ}	t_{OHZ}	Chip Disable to Output Inactive		20		25		30	ns	h
8	t_{GLQX}	t_{OLZ}	Output Enable to Output Active	0		0		0		ns	
9	t_{GHQZ}	t_{HZ}	Output Disable to Output Inactive		20		25		30	ns	h
10	t_{ELICCH}	t_{PA}	Chip Enable to Power Active	0		0		0		ns	i
11	t_{EHICCL}	t_{PS}	Chip Enable to Power Standby		25		25		25	ns	b,i

Note b: Bringing $\overline{E}$≥V_{IH} will not produce standby currents until any non-volatile cycle in progress has timed out. See MODE SELECTION table.
Note e: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must make the transition between V_{IH} (min) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion. $\overline{NE}$ must be ≥V_{IH} during entire cycle.
Note f: For READ CYCLE 1 and 2, $\overline{W}$ and $\overline{NE}$ must be high for entire cycle.
Note g: Device is continuously selected with $\overline{E}$ low, and $\overline{G}$ low.
Note h: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note i: Parameter guaranteed but not tested.

READ CYCLE 1[f,g]



READ CYCLE 2[f]



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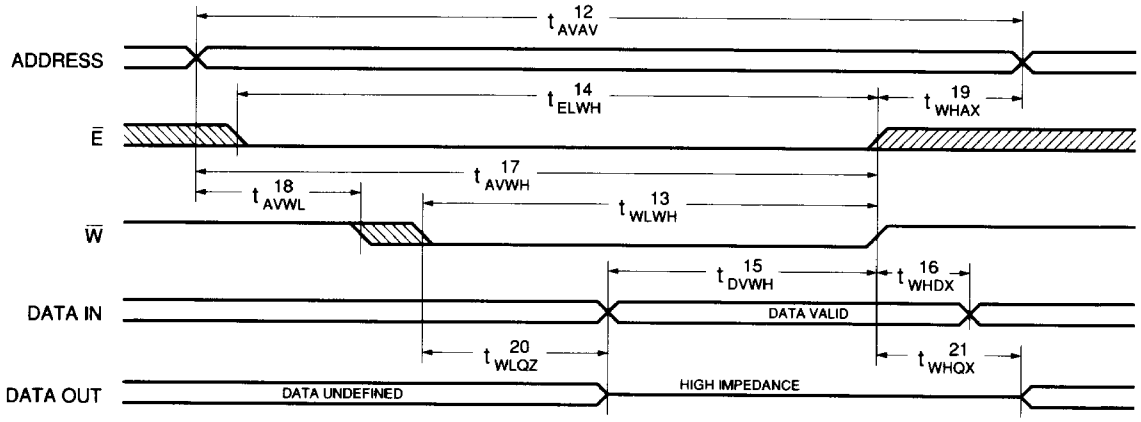
PRELIMINARY

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[e,j]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK10C68AM-45		STK10C68AM-55		STK10C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
12	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
13	t_{WLWH}	t_{WP}	Write Pulse Width	40		50		65		ns	
14	t_{ELWH}	t_{CW}	Chip Enable to End of Write	40		50		65		ns	
15	t_{DVWH}	t_{DW}	Data Set-up to End of Write	15		20		25		ns	
16	t_{WHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
17	t_{AVWH}	t_{AW}	Address Set-up to End of Write	40		50		65		ns	
18	t_{AVWL}	t_{AS}	Address Set-up to Start of Write	0		0		0		ns	
19	t_{WHAX}	t_{WR}	Address Hold After End of Write	5		5		5		ns	
20	t_{WLQZ}	t_{WZ}	Write Enable to Ouput Disable		25		30		40	ns	h
21	t_{WHQX}	t_{OW}	Output Active After End of Write	5		5		5		ns	k

WRITE CYCLE 1: $\overline{W}$ CONTROLLED[e,j]



WRITE CYCLE 2: $\overline{E}$ CONTROLLED[e,j]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK10C68AM-45		STK10C68AM-55		STK10C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
22	t_{AVAV}	t_{WC}	Write Cycle Time	45		55		70		ns	
23	t_{WLEH}	t_{WP}	Write Pulse Width	40		50		65		ns	
24	t_{ELEH}	t_{CW}	Chip Enable to End of Write	40		50		65		ns	
25	t_{DVEH}	t_{DW}	Data Set-up to End of Write	20		25		35		ns	
26	t_{EHDX}	t_{DH}	Data Hold After End of Write	0		0		0		ns	
27	t_{AVEH}	t_{AW}	Address Set-up to End of Write	40		50		65		ns	
28	t_{EHAX}	t_{AS}	Address Hold After End of Write	5		5		5		ns	
29	t_{AVEL}	t_{WR}	Address Set-up To Start of Write	0		0		0		ns	
30	t_{WLQZ}	t_{WZ}	Write Enable to Ouput Disable		25		25		40	ns	h

Note e: $\overline{E}$, $\overline{G}$ and $\overline{W}$ must make the transition between V_{IH} (max) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion. $\overline{NE}$ must be ≥V_{IH} during entire cycle.
Note h: Measured ±200mV from steady state output voltage. Load capacitance is 5pF.
Note j: $\overline{E}$ or $\overline{W}$ must be ≥V_{IH} during address transitions.
Note k: If $\overline{W}$ is low when $\overline{E}$ goes low, the outputs remain in the high impedance state.

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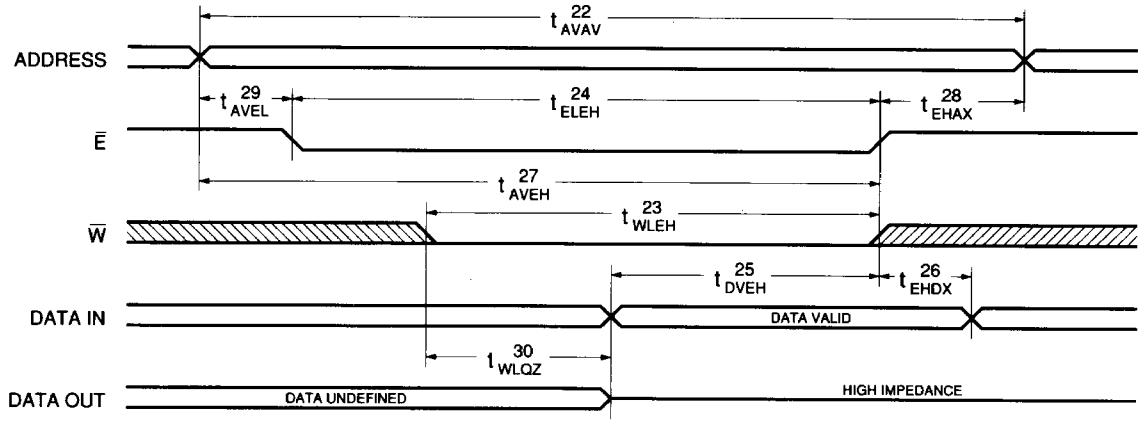
WRITE CYCLE 2: $\overline{E}$ CONTROLLED[e,j]



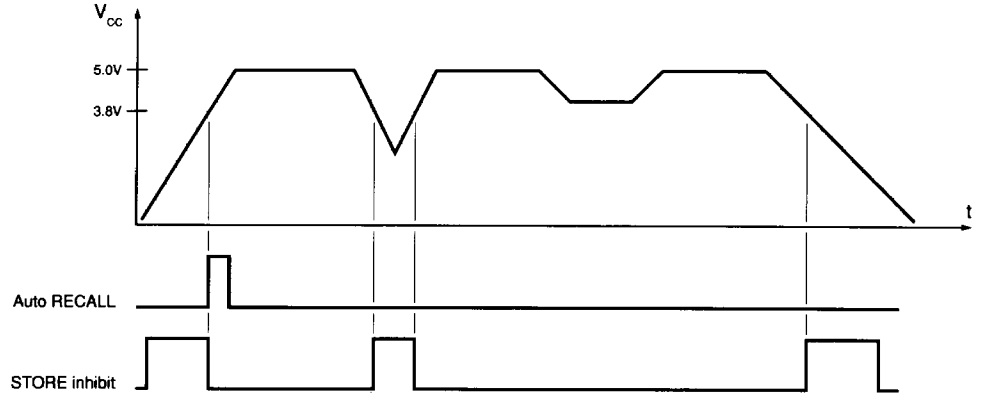
NON-VOLATILE MEMORY OPERATION

MODE SELECTION

$\overline{E}$	$\overline{W}$	$\overline{G}$	$\overline{NE}$	Mode	Power
H	X	X	X	Not Selected	Standby
L	H	L	H	Read RAM	Active
L	L	X	H	Write RAM	Active
L	H	L	L	Array Recall[m]	Active
L	L	H	L	Non-Volatile Storing	Active

Note m: An automatic RECALL also takes place on chip power-up. It takes 40µs, starting when V_{CC}=3.8V.

AUTOMATIC RECALL AND STORE INHIBIT:



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PRELIMINARY

STORE CYCLE 1: $\overline{W}$ CONTROLLED[n]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK10C68AM-45		STK10C68AM-55		STK10C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
31	t_{WLQV1}	t_{STC}	Store Cycle Time		11		11		11	ms	o
32	t_{GHNL}		Output Disable Set-up to $\overline{NE}$ Fall	0		0		0		ns	
33	t_{GHNH}		Output Disable to $\overline{NE}$ Rise	45		45		45		ns	
34	t_{NLWL}		Non-volatile Set-up to Write Low	0		0		0		ns	
45	t_{WLNH}	t_{SP}	Write Low to $\overline{NE}$ Rise	45		45		45		ns	p
36	t_{ELNH}		Chip Enable to $\overline{NE}$ Rise	45		45		45		ns	

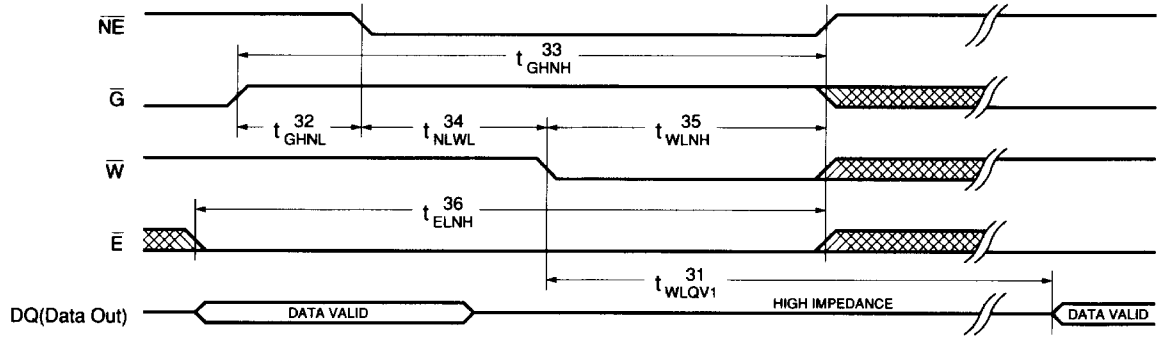
STORE CYCLE 2: $\overline{E}$ CONTROLLED[n]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

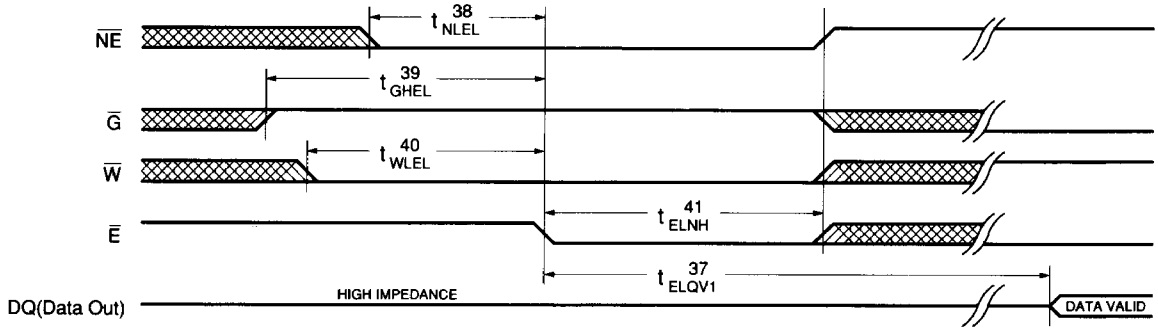
NO.	SYMBOL		PARAMETER	STK10C68AM-45		STK10C68AM-55		STK10C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
37	t_{ELQV1}	t_{STC}	Store Cycle Time		11		11		11	ms	o
38	t_{NLEL}		$\overline{NE}$ Set-up to Chip Enable	5		5		5		ns	
39	t_{GHEL}		Output Enable Set-up to Chip Enable	5		5		5		ns	
40	t_{WLEL}		Write Enable Set-up to Chip Enable	5		5		5		ns	
41	t_{ELNH}	t_{SP}	Chip Enable to $\overline{NE}$ Rise	45		45		45		ns	p

Note n: $\overline{E}$, $\overline{G}$, $\overline{NE}$, and $\overline{W}$ must make the transition between V_{IH} (max) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note o: Measured with $\overline{W}$ and $\overline{NE}$ both returned high, and $\overline{G}$ returned low. Note that store cycles are inhibited/aborted by V_{CC} < 3.8V (STORE inhibit).
Note p: Once t_{SP} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the store cycle is completed automatically, ignoring all inputs.

STORE CYCLE 1: $\overline{W}$ CONTROLLED[n]



STORE CYCLE 2: $\overline{E}$ CONTROLLED[n]



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PRELIMINARY

RECALL CYCLE 1: $\overline{NE}$ or $\overline{G}$ CONTROLLED[n]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

NO.	SYMBOL		PARAMETER	STK10C68AM-45		STK10C68AM-55		STK10C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
42	t_{NLQV1}	t_{RCC}	Array Recall Cycle Time		40		40		40	µs	q
43	t_{GLQV1}	t_{RCC}	Array Recall Cycle Time		40		40		40	µs	q
44	t_{GLNH}	t_{RCP}	Output Enable to $\overline{NE}$ Rise	45		45		45		ns	r
45	t_{WHNL}		Write Disable Set-up to $\overline{NE}$ Fall	0		0		0		ns	
46	t_{WHNH}		Write Disable to $\overline{NE}$ Rise	45		45		45		ns	
47	t_{ELNH}	t_{RCP}	Chip Enable to $\overline{NE}$ Rise	45		45		45		ns	
48	t_{NLQZ}		$\overline{NE}$ Fall to Outputs Inactive	0	45	0	45	0	45	ns	

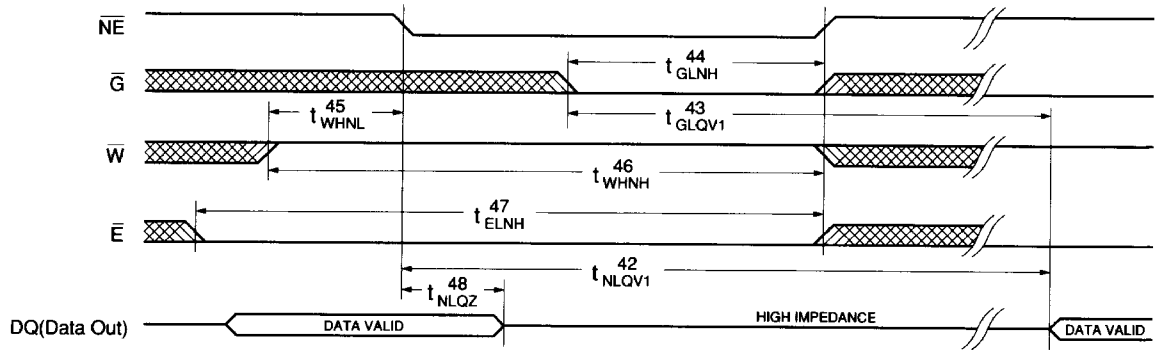
RECALL CYCLE 2: $\overline{E}$ CONTROLLED[n]

(-55°C≤T_A≤125°C) (V_{CC}=5.0V ±10%)

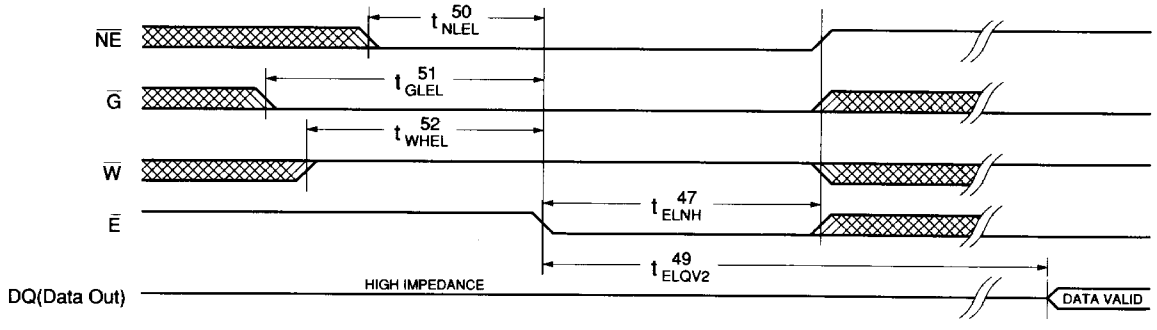
NO.	SYMBOL		PARAMETER	STK10C68AM-45		STK10C68AM-55		STK10C68AM-70		UNITS	NOTES
	Standard	Alternate		MIN	MAX	MIN	MAX	MIN	MAX		
49	t_{ELQV2}	t_{RCC}	Array Recall Cycle Time		40		40		40	µs	q
50	t_{NLEL}		$\overline{NE}$ Set-up to Chip Enable	0		0		0		ns	
51	t_{GLEL}		Output Enable Set-up to Chip Enable	0		0		0		ns	
52	t_{WHEL}		Write Disable Set-up to Chip Enable	0		0		0		ns	

Note n: $\overline{E}$, $\overline{G}$, $\overline{NE}$ and $\overline{W}$ must make the transition between V_{IH} (max) to V_{IL} (max), or V_{IL} (max) to V_{IH} (min) in a monotonic fashion.
Note q: Measured with $\overline{W}$ and $\overline{NE}$ both returned high, and $\overline{G}$ returned low. t_{NLQV1} applies if $\overline{NE}$ goes low after $\overline{G}$, and t_{GLQV1} applies if $\overline{G}$ goes low after $\overline{NE}$.
Note r: Once t_{RCP} has been satisfied by $\overline{NE}$, $\overline{G}$, $\overline{W}$ and $\overline{E}$, the recall cycle is completed automatically, ignoring all inputs.

RECALL CYCLE 1: $\overline{NE}$ or $\overline{G}$ CONTROLLED[n]



RECALL CYCLE 2: $\overline{E}$ CONTROLLED[n]



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DEVICE OPERATION

The STK10C68AM has two separate modes of operation: SRAM mode and non-volatile mode. In SRAM mode $\overline{NE}$ is held HIGH and the memory operates as an ordinary static RAM. In non-volatile operation, data is transferred from SRAM to EEPROM or from EEPROM to SRAM. In this mode SRAM functions are disabled.

SRAM READ

The STK10C68AM performs a read cycle whenever $\overline{E}$ and $\overline{G}$ are LOW and $\overline{NE}$ and $\overline{W}$ are HIGH. The address specified by the 13 addresses, A_{0-12} specify which of the 8192 data bytes will be accessed. If the read cycle is initiated by an address transition, the outputs will be valid at t_{AVQV} (READ CYCLE 1). If the cycle is initiated by a clock signal the outputs will be valid at t_{ELQV} or at t_{GLQV}, whichever is later (READ CYCLE 2). As long as the clocks remain in the READ state the outputs will repeatedly respond to address changes within t_{AVQV} access time without the need for additional clocking cycles. The outputs remain valid until another address change or until $\overline{E}$ or $\overline{G}$ is brought HIGH or $\overline{W}$ or $\overline{NE}$ is brought LOW.

SRAM WRITE

A write cycle is performed whenever $\overline{E}$ and $\overline{W}$ are LOW and $\overline{NE}$ is HIGH. The address inputs must be stable prior to entering the WRITE cycle and must remain stable until either $\overline{E}$ or $\overline{W}$ go HIGH at the end of the cycle. The data on the eight inputs, DQ_{0-7}, will be written into the memory location specified by the address inputs. The DQ data may be changed during the write cycle. Valid data must, however, be present t_{DVWH} before the end of a $\overline{W}$ controlled WRITE or t_{DVEH} before the end of an $\overline{E}$ controlled WRITE for the memory cells to be fully written.

It is recommended that $\overline{G}$ be kept HIGH during the entire WRITE cycle to avoid data bus contention on the common I/O's. If $\overline{G}$ is left LOW however, internal circuitry will turn off the output buffers t_{WHQZ} after $\overline{W}$ goes LOW. Until that time, data bus contention is possible.

NON-VOLATILE STORE

A STORE cycle is performed when $\overline{NE}$, $\overline{E}$ and $\overline{W}$ are LOW and $\overline{G}$ is HIGH. The cycle is initiated when the last of the four signals goes to the required state. However, only $\overline{W}$ initiation (STORE CYCLE 1) and $\overline{E}$ initiation (STORE CYCLE 2) are practical without risking an unintentional SRAM WRITE that would disturb SRAM data. During the STORE cycle, an erase of the previous non-volatile data is first performed, followed by a program of the non-volatile elements.

The program operation copies the SRAM data into non-volatile storage. Once a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

If $\overline{E}$ and $\overline{G}$ are LOW and $\overline{W}$ and $\overline{NE}$ are HIGH at the end of the cycle, a READ will be performed and the outputs will go active. Until that time the outputs remain off. This signals the end of the STORE operation and the start of normal SRAM operation.

HARDWARE PROTECT

The STK10C68AM offers two levels of protection to suppress inadvertent STORE cycles. If the clock signals remain in the STORE condition at the end of a STORE cycle, a second STORE cycle will *not* be started. This feature prevents an inadvertent retriggering of the long, non-volatile cycle by initiating the cycle only after a HIGH to LOW transition on $\overline{NE}$. Because the STORE cycle is initiated by an $\overline{NE}$ transition, powering up the chip with $\overline{NE}$ LOW will *not* initiate a STORE cycle either. In addition to multi-trigger protection, the STK10C68AM offers hardware protection through V_{CC} Sense. A STORE cycle will not be initiated, and one in progress will discontinue, if V_{CC} goes below 3.8V.

NON-VOLATILE RECALL

A RECALL cycle is performed when $\overline{E}$, $\overline{G}$, and $\overline{NE}$ are LOW and $\overline{W}$ is HIGH. Like the STORE cycle, RECALL is initiated when the last of the four clock signals goes to the RECALL state. If $\overline{NE}$ or $\overline{G}$ initiates the cycle, the outputs will go active at t_{NLQV1} or t_{GLQV1}, whichever is later (RECALL CYCLE 1). If the cycle is initiated by $\overline{E}$, the outputs will go active at t_{ELQV2}. Once initiated, the RECALL cycle will run to completion. As in the STORE cycle, the outputs going active indicates the end of the RECALL cycle.

Internally, RECALL is a two step procedure. First, the SRAM data is cleared and second, the non-volatile information is transferred into the SRAM cells. The RECALL operation in no way alters the data in the EEPROM cells. The non-volatile data can be recalled an unlimited number of times.

There is also multi-trigger protection in the RECALL initiation to prevent repeating the long cycle. On power-up, once V_{CC} exceeds the V_{CC} sense voltage of 3.8V, a RECALL cycle is automatically initiated. For this reason, SRAM operation cannot commence until t_{NLQV1} after V_{CC} is high.

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