

Document Title

128Kx8 bit Low Power CMOS Static RAM

Revision History

<u>Revision No.</u>	<u>History</u>	<u>Draft Data</u>	<u>Remark</u>
0.0	Initial draft	July 15, 2002	Preliminary

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K6X1008T2D Family

128Kx8 bit Super Low Power and Low Voltage full CMOS Static RAM

FEATURES

- Process Technology: Full CMOS
- Organization: 128K x 8
- Power Supply Voltage: 2.7~3.6V
- Low Data Retention Voltage: 1.5V(Min)
- Three state output and TTL Compatible
- Package Type: 32-SOP-525, 32-TSOP1-0820F/R
32-TSOP1-0813.4F/R

GENERAL DESCRIPTION

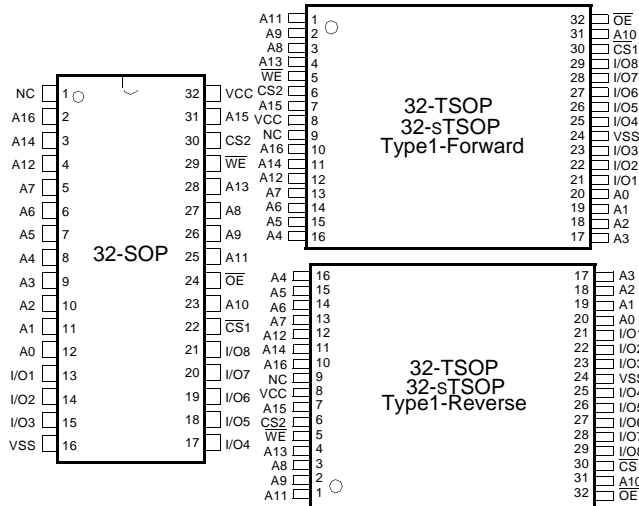
The K6X1008T2D families are fabricated by SAMSUNG's advanced CMOS process technology. The families support various operating temperature ranges and have various package types for user flexibility of system design. The families also support low data retention voltage for battery back-up operation with low data retention current.

PRODUCT FAMILY

Product Family	Operating Temperature	Vcc Range	Speed	Power Dissipation		PKG Type
				Standby (I _{sb1} , Max)	Operating (I _{cc2} , Max)	
K6X1008T2D-F	Industrial(-40~85°C)	2.7~3.6V	70 ¹⁾ /85ns	10μA	25mA	32-SOP-525, 32-TSOP1-0820F/R 32-TSOP1-0813.4F/R
K6X1008T2D-Q	Automotive(-40~125°C)			20μA		32-SOP-525, 32-TSOP1-0820F 32-TSOP1-0813.4F

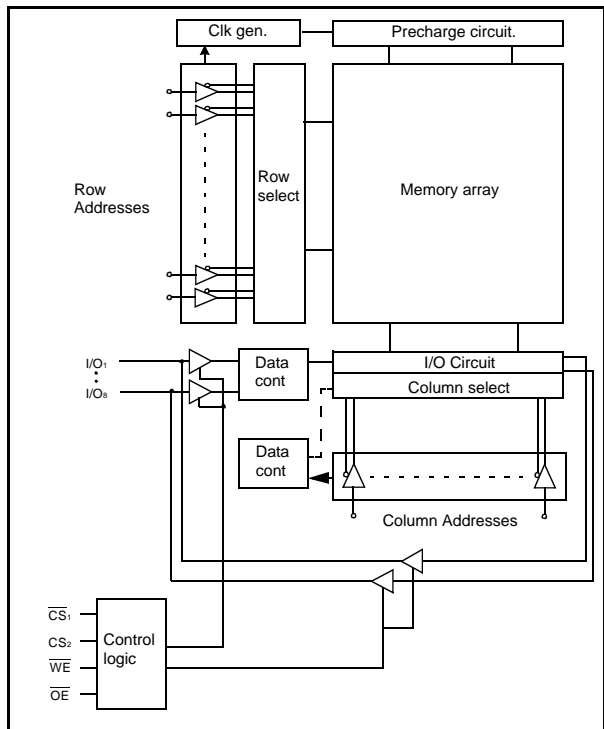
1. The parameters are tested with 30pF test load

PIN DESCRIPTION



Name	Function
A0~A16	Address Inputs
\overline{WE}	Write Enable Input
$\overline{CS1}, \overline{CS2}$	Chip Select Input
\overline{OE}	Output Enable Input
I/O1~I/O8	Data Inputs/Outputs
Vcc	Power
Vss	Ground
NC	No Connection

FUNCTIONAL BLOCK DIAGRAM



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PRODUCT LIST

Industrial Temp. Products(-40~85°C)		Automotive Temp. Products(-40~125°C)	
Part Name	Function	Part Name	Function
K6X1008T2D-GF70	32-SOP, 70ns, LL Pwr	K6X1008T2D-GQ70	32-SOP, 70ns, L Pwr
K6X1008T2D-GF85	32-SOP, 85ns, LL Pwr	K6X1008T2D-GQ85	32-SOP, 85ns, L Pwr
K6X1008T2D-TF70	32-TSOP-F, 70ns, LL Pwr	K6X1008T2D-TQ70	32-TSOP-F, 70ns, L Pwr
K6X1008T2D-TF85	32-TSOP-F, 85ns, LL Pwr	K6X1008T2D-TQ85	32-TSOP-F, 85ns, L Pwr
K6X1008T2D-RF70	32-TSOP-R, 70ns, LL Pwr	K6X1008T2D-YQ70	32-sTSOP-F, 70ns, L Pwr
K6X1008T2D-RF85	32-TSOP-R, 85ns, LL Pwr	K6X1008T2D-YQ85	32-sTSOP-F, 85ns, L Pwr
K6X1008T2D-YF70	32-sTSOP-F, 70ns, LL Pwr		
K6X1008T2D-YF85	32-sTSOP-F, 85ns, LL Pwr		
K6X1008T2D-NF70	32-sTSOP-R, 70ns, LL Pwr		
K6X1008T2D-NF85	32-sTSOP-R, 85ns, LL Pwr		

FUNCTIONAL DESCRIPTIO

\overline{CS}_1	CS_2	\overline{OE}	\overline{WE}	I/O	Mode	Power
H	X ¹⁾	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
X ¹⁾	L	X ¹⁾	X ¹⁾	High-Z	Deselected	Standby
L	H	H	H	High-Z	Output Disabled	Active
L	H	L	H	Dout	Read	Active
L	H	X ¹⁾	L	Din	Write	Active

1. X means don't care (Must be in high or low states)

ABSOLUTE MAXIMUM RATINGS¹⁾

Item	Symbol	Ratings	Unit	Remark
Voltage on any pin relative to Vss	V _{IN} ,V _{OUT}	-0.2 to V _{CC} +0.3V(Max. 3.9V)	V	-
Voltage on Vcc supply relative to Vss	V _{CC}	-0.2 to 3.9	V	-
Power Dissipation	P _D	1.0	W	-
Storage temperature	T _{STG}	-65 to 150	°C	-
Operating Temperature	T _A	-40 to 85	°C	K6X1008T2D-F
		-40 to 125	°C	K6X1008T2D-Q

1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation should be restricted to recommended operating condition. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS¹⁾

Item	Symbol	Min	Typ	Max	Unit
Supply voltage	V _{CC}	2.7	3.0/3.3	3.6	V
Ground	V _{SS}	0	0	0	V
Input high voltage	V _{IH}	2.2	-	V _{CC} +0.2 ²⁾	V
Input low voltage	V _{IL}	-0.2 ³⁾	-	0.6	V

Note:

1. Industrial Product: T_A=-40 to 85°C, Otherwise specified
Automotive Product: T_A=-40 to 125°C, Otherwise specified
2. Overshoot: V_{CC}+3.0V in case of pulse width≤30ns.
3. Undershoot: -3.0V in case of pulse width≤30ns.
4. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE¹⁾ (f=1MHz, T_A=25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input capacitance	C _{IN}	V _{IN} =0V	-	8	pF
Input/Output capacitance	C _{IO}	V _{IO} =0V	-	10	pF

1. Capacitance is sampled, not 100% tested

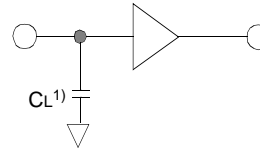
DC AND OPERATING CHARACTERISTICS

Item	Symbol	Test Conditions	Min	Typ	Max	Unit	
Input leakage current	I _{LI}	V _{IN} =V _{SS} to V _{CC}	-1	-	1	μA	
Output leakage current	I _{LO}	$\overline{CS}_1=V_{IH}$ or $CS_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$, V _{IO} =V _{SS} to V _{CC}	-1	-	1	μA	
Operating power supply current	I _{CC}	I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, V _{IN} =V _{IH} or V _{IL} , Read	-	-	3	mA	
Average operating current	I _{CC1}	Cycle time=1μs, 100%duty, I _{IO} =0mA, $\overline{CS}_1 \leq 0.2V$, $CS_2 \geq V_{CC}-0.2V$, V _{IN} ≤0.2V or V _{IN} ≥V _{CC} -0.2V	-	-	3	mA	
	I _{CC2}	Cycle time=Min, 100% duty, I _{IO} =0mA, $\overline{CS}_1=V_{IL}$, $CS_2=V_{IH}$, V _{IN} =V _{IH} or V _{IL}	-	-	25	mA	
Output low voltage	V _{OL}	I _{OL} =2.1mA	-	-	0.4	V	
Output high voltage	V _{OH}	I _{OH} =-1.0mA	2.4	-	-	V	
Standby Current(TTL)	I _{SB}	$\overline{CS}_1=V_{IH}$, $CS_2=V_{IL}$, Other inputs=V _{IH} or V _{IL}	-	-	0.3	mA	
Standby Current(CMOS)	I _{SB1}	$\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$ or $CS_2 \leq 0.2V$, Other inputs=0~V _{CC}	K6X1008T2D-F	-	-	10	μA
			K6X1008T2D-Q	-	-	20	μA

AC OPERATING CONDITIONS

TEST CONDITIONS (Test Load and Input/Output Reference)

Input pulse level: 0.4 to 2.2V
 Input rising and falling time: 5ns
 Input and output reference voltage: 1.5V
 Output load(see right): $C_L=100\text{pF}+1\text{TTL}$
 $C_L=30\text{pF}+1\text{TTL}$



1. Including scope and jig capacitance

AC CHARACTERISTICS (V_{CC}=2.7~3.6V, Industrial product: T_A=-40 to 85°C, Automotive product: T_A=-40 to 125°C)

Parameter List		Symbol	Speed Bins				Units
			70ns		85ns		
			Min	Max	Min	Max	
Read	Read Cycle Time	t _{RC}	70	-	85	-	ns
	Address Access Time	t _{AA}	-	70	-	85	ns
	Chip Select to Output	t _{CO}	-	70	-	85	ns
	Output Enable to Valid Output	t _{OE}	-	35	-	40	ns
	Chip Select to Low-Z Output	t _{LZ}	10	-	10	-	ns
	Output Enable to Low-Z Output	t _{OLZ}	5	-	5	-	ns
	Chip Disable to High-Z Output	t _{HZ}	0	25	0	25	ns
	Output Disable to High-Z Output	t _{OHZ}	0	25	0	25	ns
	Output Hold from Address Change	t _{OH}	10	-	15	-	ns
Write	Write Cycle Time	t _{WC}	70	-	85	-	ns
	Chip Select to End of Write	t _{CW}	60	-	70	-	ns
	Address Set-up Time	t _{AS}	0	-	0	-	ns
	Address Valid to End of Write	t _{AW}	60	-	70	-	ns
	Write Pulse Width	t _{WP}	50	-	60	-	ns
	Write Recovery Time	t _{WR}	0	-	0	-	ns
	Write to Output High-Z	t _{WHZ}	0	25	0	30	ns
	Data to Write Time Overlap	t _{DW}	25	-	35	-	ns
	Data Hold from Write Time	t _{DH}	0	-	0	-	ns
		End Write to Output Low-Z	t _{OW}	5	-	5	-

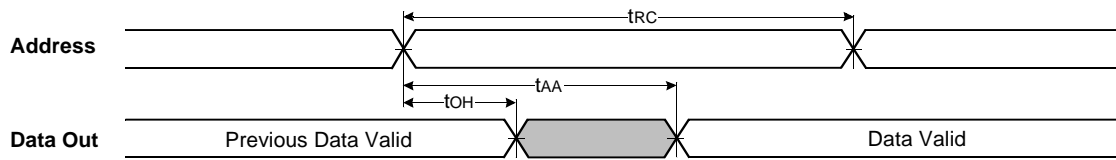
DATA RETENTION CHARACTERISTICS

Item	Symbol	Test Condition	Min	Typ	Max	Unit	
V _{CC} for data retention	V _D R	$\overline{CS}_1 \geq V_{CC}-0.2V^1$	2.0	-	3.6	V	
Data retention current	I _D R	V _{CC} =3.0V, $\overline{CS}_1 \geq V_{CC}-0.2V^1$	K6X1008T2D-F	-	-	10	μA
			K6X1008T2D-Q	-	-	20	μA
Data retention set-up time	t _S DR	See data retention waveform	0	-	-	ms	
Recovery time	t _R DR		5	-	-		

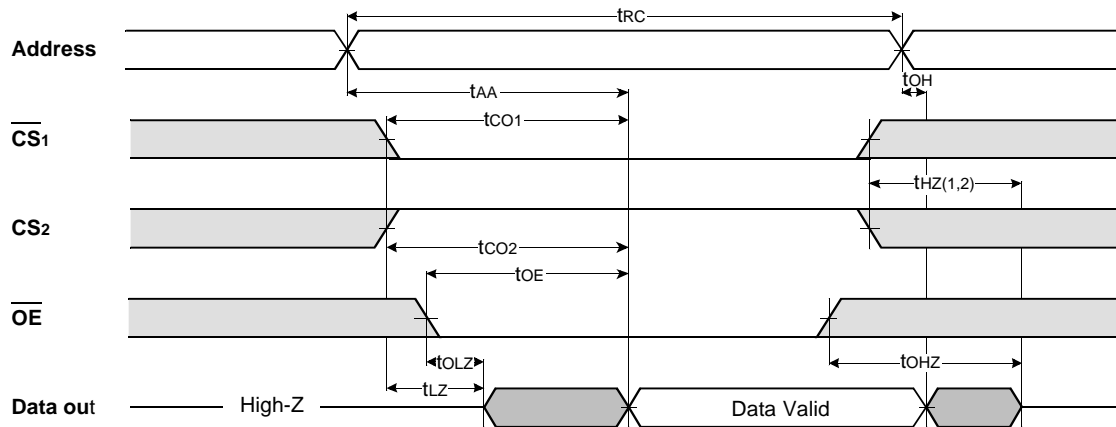
1. $\overline{CS}_1 \geq V_{CC}-0.2V$, $CS_2 \geq V_{CC}-0.2V$, or $CS_2 \leq 0.2V$

TIMING DIAGRAMS

TIMING WAVEFORM OF READ CYCLE(1) (Address Controlled, $\overline{CS1}=\overline{OE}=V_{IL}$, $CS2=\overline{WE}=V_{IH}$)



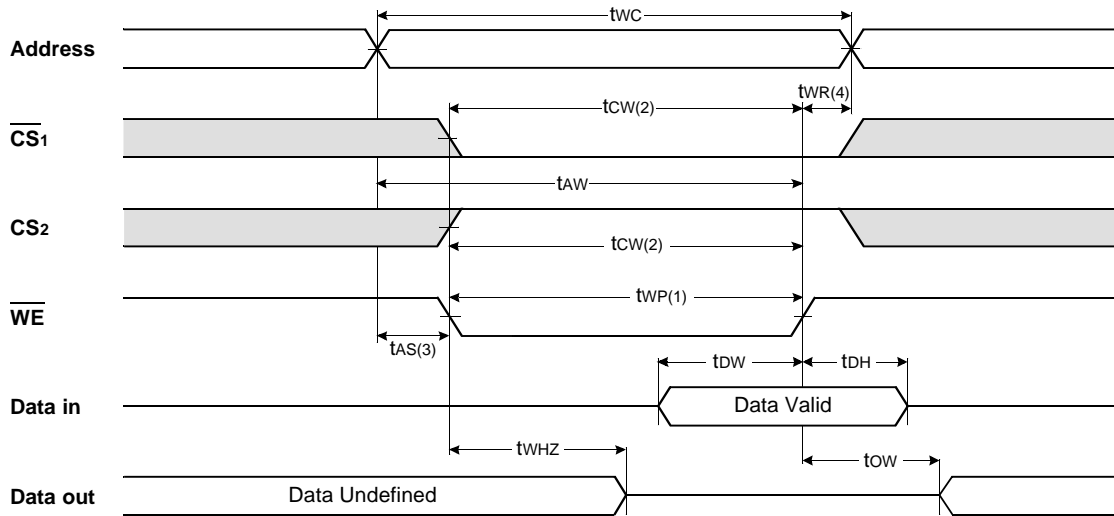
TIMING WAVEFORM OF READ CYCLE(2) ($\overline{WE}=V_{IH}$)



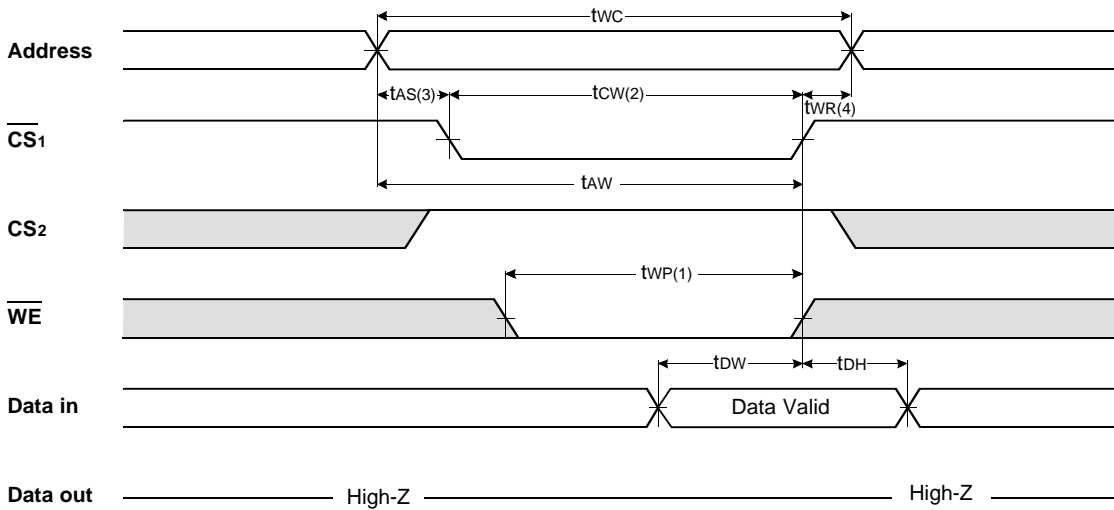
NOTES (READ CYCLE)

1. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition, $t_{HZ}(\text{Max.})$ is less than $t_{LZ}(\text{Min.})$ both for a given device and from device to device interconnection.

TIMING WAVEFORM OF WRITE CYCLE(1) (\overline{WE} Controlled)



TIMING WAVEFORM OF WRITE CYCLE(2) ($\overline{CS1}$ Controlled)



TIMING WAVEFORM OF WRITE CYCLE(3) (CS₂ Controlled)

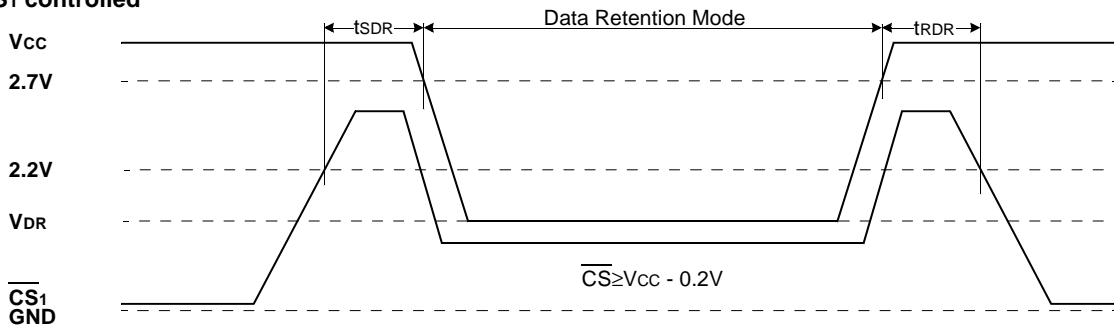


NOTES (WRITE CYCLE)

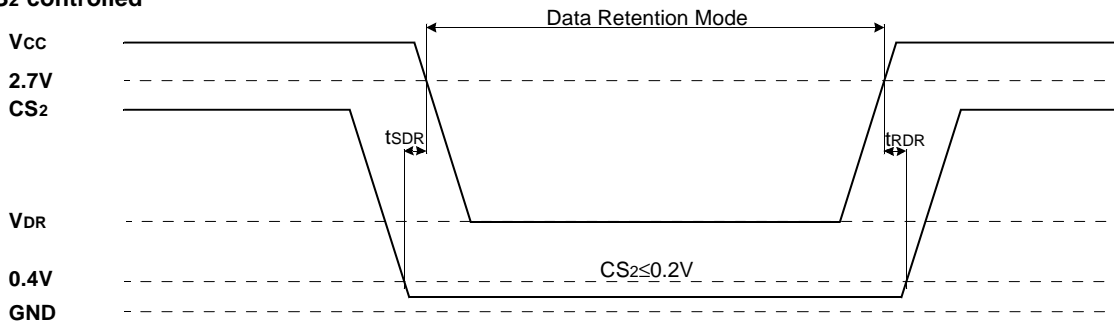
1. A write occurs during the overlap of a low $\overline{CS_1}$, a high CS₂ and a low \overline{WE} . A write begins at the latest transition among $\overline{CS_1}$ goes low, CS₂ going high and \overline{WE} going low: A write ends at the earliest transition among CS₁ going high, CS₂ going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from the $\overline{CS_1}$ going low or CS₂ going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS_1}$ or \overline{WE} going high t_{WR2} applied in case a write ends as CS₂ going to low.

DATA RETENTION WAVE FORM

CS₁ controlled



CS₂ controlled



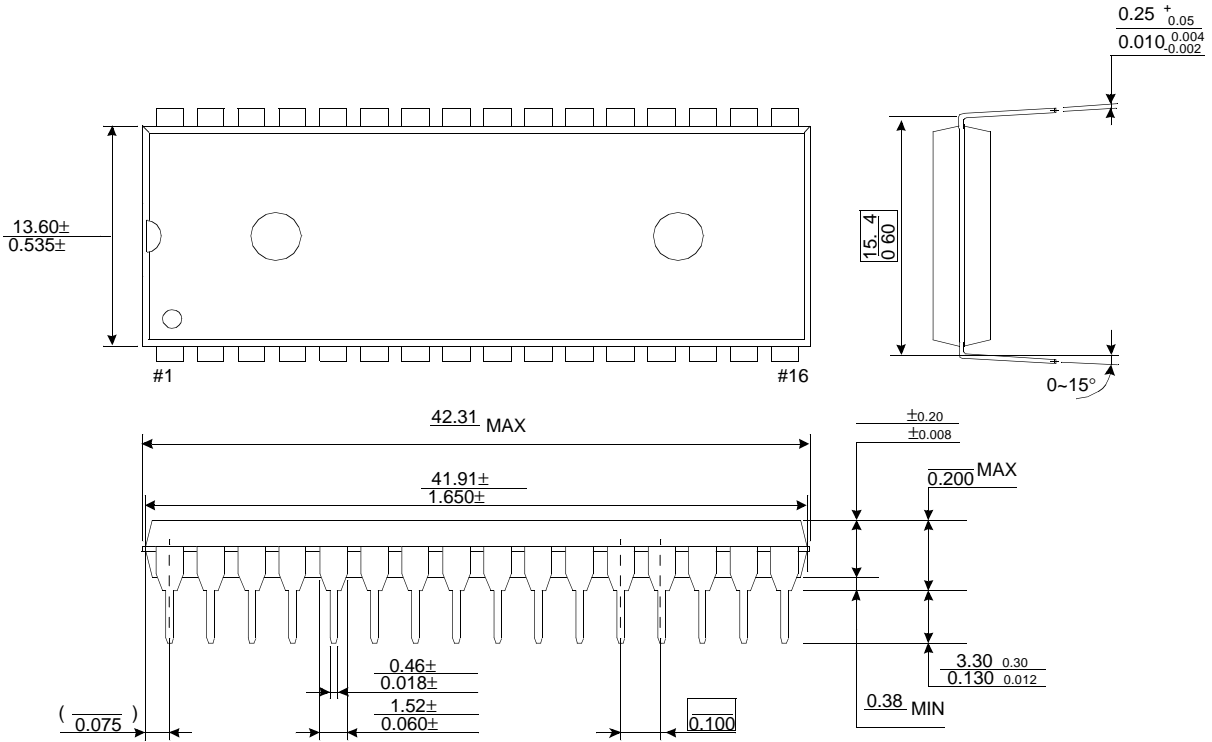
K6X1008T2D Family

**Preliminary
CMOS SRAM**

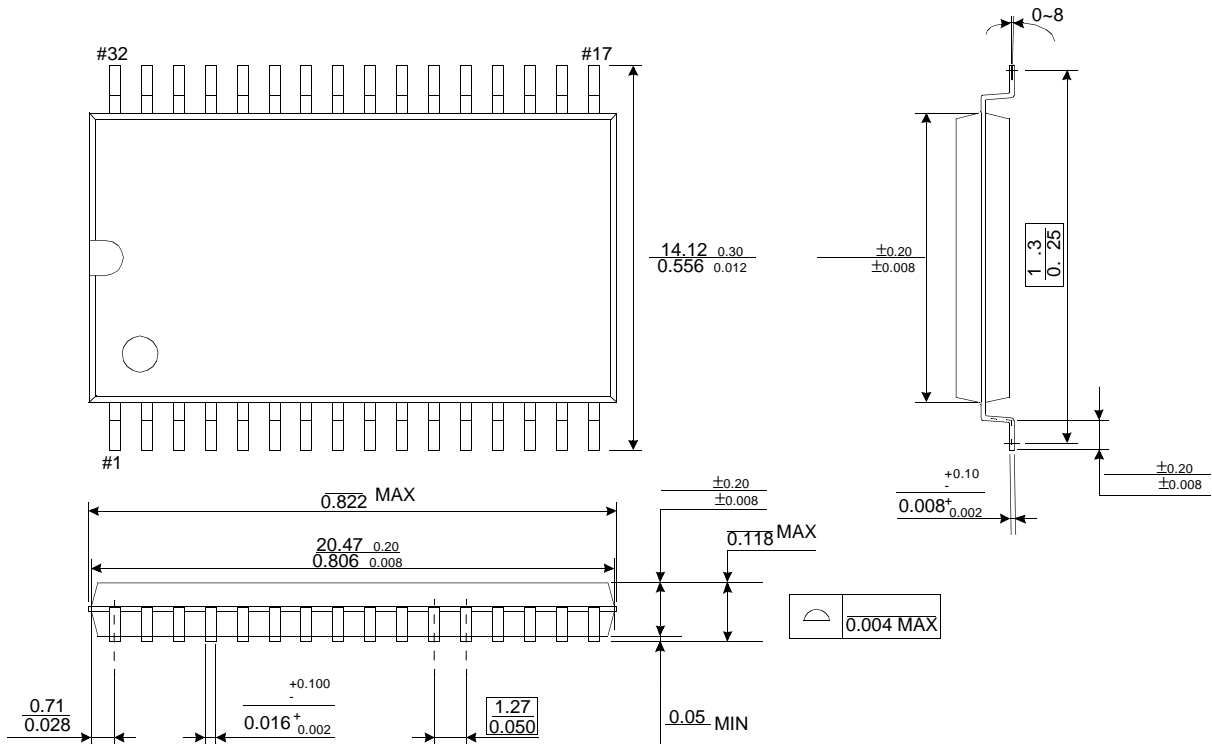
PACKAGE DIMENSIONS

32 DUAL INLINE PACKAGE (600mil)

Units: millimeters(inches)



32 PLASTIC SMALL OUTLINE PACKAGE (525mil)



K6X1008T2D Family

Preliminary
CMOS SRAM

PACKAGE DIMENSIONS

Units: millimeters(inches)

32 PIN THIN SMALL OUTLINE PACKAGE TYPE I (0820F)

