

MX23C3211

with page mode

$32M-BIT(4M \times 2M \times 16)$ **CMOS MASK ROM**

FEATURES

- With page mode function
- · Switchable configuration
 - 4M x 8(byte mode)
 - 2M x 16(word mode)
- Single +5V power supply
- Fast access time: 100/120/150ns (max)
- Fast page mode access time: 45/50/70ns

- Totally static operation
- Completely TTL compatible
- · Operating current: 60mA
- Standby current: 100µA
- Package
 - 42 pin DIP (600 mil)/(word mode only)
 - 44 pin SOP (500 mil)

GENERAL DESCRIPTION

The MX23C3211 is a 5V only, 32M-bit, Read Only Memory with page mode. It is organized as 4M x 8 bits (byte mode) or as 2M x 16 bit (word mode) depending on BYTE (pin 32/44 SOP) voltage level. MX23C3211 has a static standby mode, and has an access time of 100/120/ 150ns. It is designed to be compatible with all microprocessors and similar applications in which high performance, large bit storage and simple interfacing are important design considerations.

MX23C1611 offers automatic power-down, with powerdown controlled by the chip enable(CE/CE) Input. When CE/CE is not selected, the device automatically powers down and remains in a low-power standby mode as long as CE/CE stays in the unselected mode.

The OE/OE inputs as well as CE/CE input may be programmed either active High or Low.

PIN CONFIGURATIONS 42 PDIP

A18		1		42	Ь	A19
A17		2		41	Ь	A8
A 7		3		40	Ь	A9
A6		4		39	Ь	A10
A5		5		38	Þ	A11
A4		6		37	Þ	A12
A3		7		36	Þ	A13
A2		8	=	35		A14
A1		9	짒	34	⊳	A15
A0		10	MX23C3211	33	Þ	A16
CE/CE	d	11	2	32	Þ	A20
VSS	d	12	×	31	Þ	VSS
OE/OE		13	2	30	Þ	Q15/A-1
Q0	Ц	14		29	b b	Q7
Q8		15		28		Q14
Q1		16		27	Þ	Q6
Q9		17		26	Þ	Q13
Q2		18		25	Þ	Q5
Q10		19		24	P	Q12
Q3		20		23	P	Q4
Q11		21		22	Р	VCC

44 SOP

