74ALVCH162373

LOW VOLTAGE CMOS 16-BIT BUS BUFFER (3-STATE) WITH 3.6V TOLERANT INPUTS AND OUTPUTS

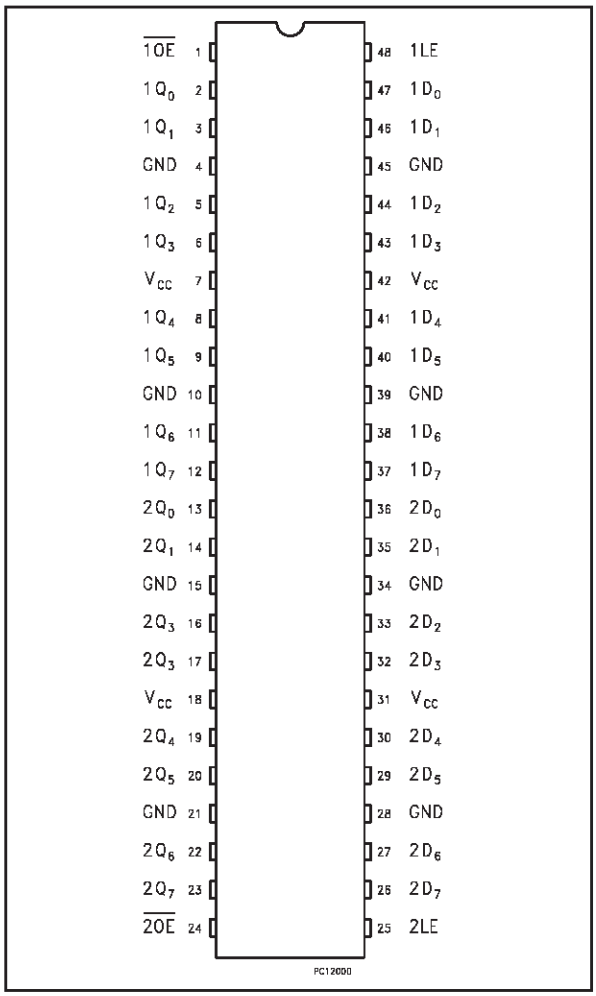
- 3.6V TOLERANT INPUTS AND OUTPUTS
- HIGH SPEED :
  t_{PD} = 3.0 ns (MAX.) at V_{CC} = 3.0 to 3.6V
  t_{PD} = 3.5 ns (MAX.) at V_{CC} = 2.3 to 2.7V
  t_{PD} = 3.6 ns (MAX.) at V_{CC} = 1.65V
- POWER DOWN PROTECTION ON INPUTS AND OUTPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
  $|I_{OH}| = I_{OL}$ = 24mA (MIN) at V_{CC} = 3.0V
  $|I_{OH}| = I_{OL}$ = 18mA (MIN) at V_{CC} = 2.3V
  $|I_{OH}| = I_{OL}$ = 4mA (MIN) at V_{CC} = 1.65V
- 26Ω SERIE RESISTORS IN OUTPUTS
- OPERATING VOLTAGE RANGE:
  V_{CC}(OPR) = 1.8V to 3.6V
- PIN AND FUNCTION COMPATIBLE WITH 74 SERIES 16240
- LATCH-UP PERFORMANCE EXCEEDS 300mA (JESD 17)
- ESD PERFORMANCE:
  HBM > 2000V (MIL STD 883 method 3015);
  MM > 200V

TSSOP

ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74ALVCH162373T

PIN CONNECTION



DESCRIPTION

The 74VCXH16373 is a low voltage CMOS 16 BIT D-TYPE LATCH with 3 STATE OUTPUTS NON INVERTING fabricated with sub-micron silicon gate and five-layer metal wiring C^2MOS technology. It is ideal for low power and very high speed 1.8 to 3.6V applications; it can be interfaced to 3.6V signal environment for both inputs and outputs.

These 16 bit D-TYPE latches are bite controlled by two latch enable inputs (nLE) and two output enable inputs ($\overline{OE}$).

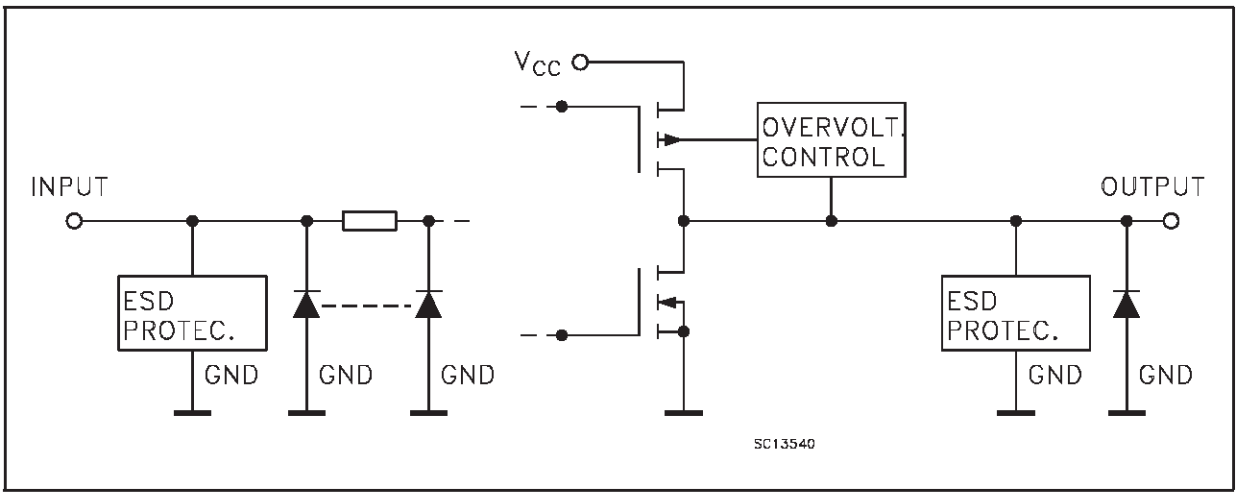
While the nLE input is held at a high level, the nQ outputs will follow the data input precisely.

When the nLE is taken low, the nQ outputs will be in a normal logic state (high or low logic level) and while high level the outputs will be in a high impedance state.This device is designed to be used with 3 state memory address drivers, etc.

The device circuits is including 26Ω series resistance in the outputs. These resistors permit to reduce line noise in high speed applications.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

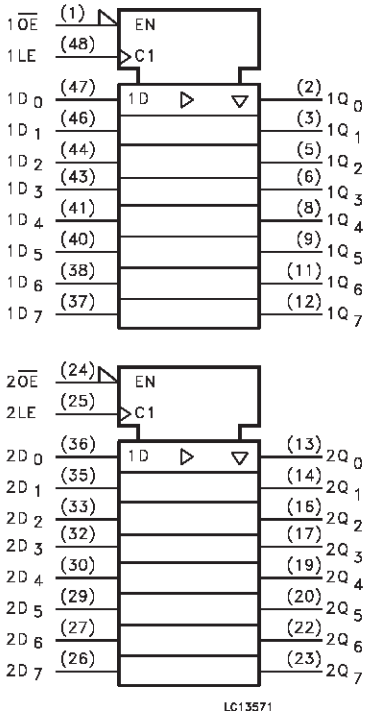
PIN No	SYMBOL	NAME AND FUNCTION
1	$1\overline{OE}$	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	$2\overline{OE}$	3 State Output Enable Input (Active LOW)
25	2LE	Latch Enable Input
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1LE	Latch Enable Input
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V_{CC}	Positive Supply Voltage

TRUTH TABLE

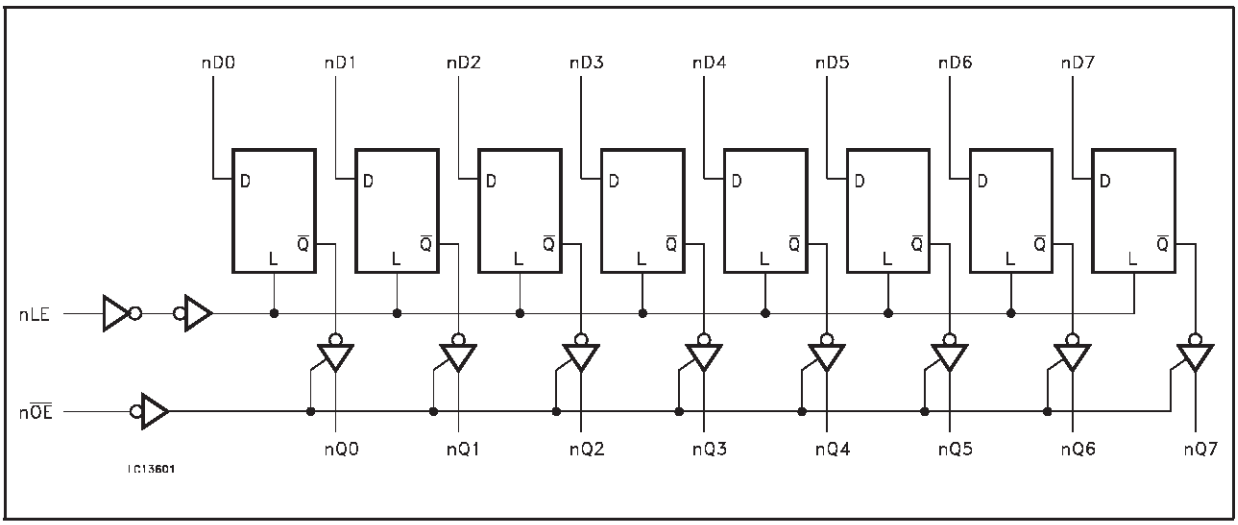
INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
H	X	X	Z
L	L	X	NO CHANGE *
L	H	L	L
L	H	H	H

X : Don't Care
Z : High Impedance
* : Q outputs are latched at the time when the LE input is taken low logic level.

IEC LOGIC SYMBOLS



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +4.6	V
V_I	DC Input Voltage	-0.5 to +4.6	V
V_O	DC Output Voltage (OFF State)	-0.5 to +4.6	V
V_O	DC Output Voltage (High or Low State) (note 1)	-0.5 to V_{CC} + 0.5	V
I_{IK}	DC Input Diode Current	- 50	mA
I_{OK}	DC Output Diode Current (note 2)	- 50	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current per Supply Pin	± 100	mA
P_D	Power Dissipation	400	mW
T_{stg}	Storage Temperature	-65 to +150	°C
T_L	Lead Temperature (10 sec)	300	°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied

1) I_O absolute maximum rating must be observed

2) $V_O < GND$, $V_O > V_{CC}$

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	1.65 to 3.6	V
V_I	Input Voltage	-0.3 to 3.6	V
V_O	Output Voltage (OFF State)	0 to 3.6	V
V_O	Output Voltage (High or Low State)	0 to V_{CC}	V
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 3.0 to 3.6V)	± 24	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 2.3 to 2.7V)	± 18	mA
I_{OH}, I_{OL}	High or Low Level Output Current (V_{CC} = 1.8V)	± 6	mA
T_{op}	Operating Temperature	-55 to 125	°C
dt/dv	Input Rise and Fall Time (note 1)	0 to 10	ns/V

1) V_{IN} from 0.8V to 2V at V_{CC} = 3.0V

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value				Unit
		V_{CC} (V)		-40 to 85 °C		-55 to 125 °C		
				Min.	Max.	Min.	Max.	
V_{IH}	High Level Input Voltage	1.65 to 1.95		0.65 Vcc		0.65 Vcc		V
		2.3 to 2.7		1.7		1.7		
		2.7 to 3.6		2.0		2.0		
V_{IL}	Low Level Input Voltage	1.65 to 1.95			0.35 Vcc		0.35 Vcc	
		2.3 to 2.7			0.7		0.7	
		2.7 to 3.6			0.8		0.8	
V_{OH}	High Level Output Voltage	1.65 to 3.6	I_O=-100 µA	V_{CC}-0.2		V_{CC}-0.2		V
		1.65	I_O=-2 mA	1.2		1.2		
		2.3	I_O=-3 mA	2.0		2.0		
		2.3	I_O=-6 mA	1.7		1.7		
		2.7	I_O=-62 mA	2.2		2.2		
		3.0	I_O=-6 mA	2.4		2.4		
		3.0	I_O=-12 mA	2.0		2.0		
V_{OL}	Low Level Output Voltage	1.65 to 3.6	I_O=100 µA		0.2		0.2	V
		1.65	I_O=2 mA		0.45		0.45	
		2.3	I_O=3 mA		0.4		0.4	
		2.3	I_O=6 mA		0.7		0.7	
		2.7	I_O=6 mA		0.4		0.4	
		3.0	I_O=12 mA		0.55		0.55	
I_I	Input Leakage Current	3.6	V_I = 0 or 3.6V		± 5		± 5	µA
I_{IHOLD}	Bus Hold Input Leakage Current	1.65	V_I =0.58 V	+ 25		+ 25		µA
		1.65	V_I =1.07 V	- 25		- 25		
		2.3	V_I =0.7 V	+ 45		+ 45		
		2.3	V_I =1.7 V	- 45		- 45		
		3.0	V_I =0.8 V	+ 75		+ 75		
		3.0	V_I =2 V	- 75		- 75		
I_{off}	Power Off Leakage Current	0	V_I or V_O = 3.6V		10		20	µA
I_{OZ}	High Impedance Output Leakage Current	3.6	V_I = V_{IH} or V_{IL} V_O = 0 to V_{CC}		± 5		± 10	µA
I_{CC}	Quiescent Supply Current	3.6	V_I = V_{CC} or GND I_O= 0		20		40	µA
ΔI_{CC}	I_{CC} incr. per Input	3.0 to 3.6	V_{IH} = V_{CC} - 0.6V		500		750	µA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Condition				Value				Unit
		V_{CC} (V)	C_L (pF)	R_L (Ω)	$t_s = t_r$ (ns)	-40 to 85 °C		-55 to 125 °C		
						Min.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay Time Dn to Qn	1.8	30	1000	2.0					ns
		2.3 to 2.7	30	500	2.0	1	3.7	1	4.0	
		2.7	50	500	2.5	1	3.6	1	4.0	
		3.0 to 3.6	50	500	2.5	1	3.0	1	3.3	
t_{PLH} t_{PHL}	Propagation Delay Time LE to Qn	1.8	30	1000	2.0					ns
		2.3 to 2.7	30	500	2.0	1	3.7	1	4.0	
		2.7	50	500	2.5	1	3.6	1	4.0	
		3.0 to 3.6	50	500	2.5	1	3.0	1	3.3	
t_{PZL} t_{PZH}	Output Enable Time	1.8	30	1000	2.0					ns
		2.3 to 2.7	30	500	2.0	1	5.7	1	6.3	
		2.7	50	500	2.5	1	5.4	1	6.0	
		3.0 to 3.6	50	500	2.5	1	4.4	1	4.9	
t_{PLZ} t_{PHZ}	Output Disable Time	1.8	30	1000	2.0					ns
		2.3 to 2.7	30	500	2.0	1	5.2	1	5.8	
		2.7	50	500	2.5	1	4.6	1	5.1	
		3.0 to 3.6	50	500	2.5	1	4.1	1	4.5	
t_s	Setup TIme, HIGH or LOW level Dn to LE	1.8	30	1000	2.0					ns
		2.3 to 2.7	30	500	2.0					
		2.7	50	500	2.5					
		3.0 to 3.6	50	500	2.5					
t_h	Hold Time High or LOW level Dn to LE	1.8	30	1000	2.0					ns
		2.3 to 2.7	30	500	2.0					
		2.7	50	500	2.5					
		3.0 to 3.6	50	500	2.5					
t_w	LE Pulse Width, HIGH	1.8	30	1000	2.0					ns
		2.3 to 2.7	30	500	2.0					
		2.7	50	500	2.5					
		3.0 to 3.6	50	500	2.5					

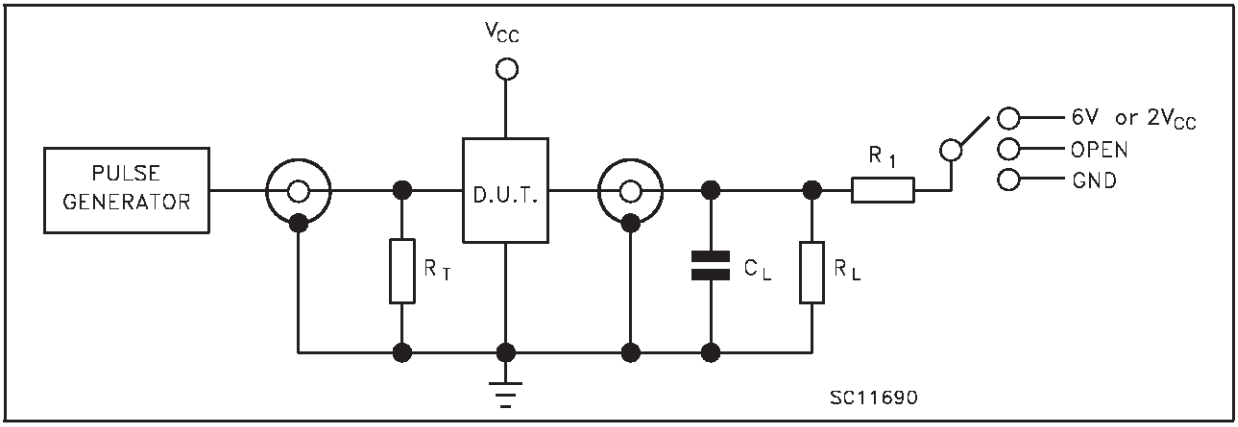
1) Skew is defined as the absolute value of the difference between the actual propagation delay for any two outputs of the same device switching in the same direction, either HIGH or LOW ($t_{OSLH} = |t_{PLHm} - t_{PLHn}|$, $t_{OSHL} = |t_{PHLm} - t_{PHLn}|$)
2) Parameter guaranteed by design

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value			Unit
		V_{CC} (V)		T_A = 25 °C			
				Min.	Typ.	Max.	
C_{IN}	Input Capacitance Control Inputs	3.3	V_{IN} =V_{CC} or GND		3		pF
C_{IN}	Input Capacitance Data Inputs	3.3	V_{IN} =V_{CC} or GND		6		pF
C_{OUT}	Output Capacitance	3.3	V_{IN} = 0 to V_{CC}		7		pF
C_{PD}	Power Dissipation Capacitance Output enabled (note 1)	3.3	f_{IN} = 10MHz C_L=50pF V_{IN} = 0 or V_{CC}		19		pF
		2.5			16		
C_{PD}	Power Dissipation Capacitance Output disabled (note 1)	3.3			5		
		2.5			4		

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. $I_{CC(opr)} = C_{PD} \times V_{CC} \times f_{IN} + I_{CC}/16$ (per circuit)

TEST CIRCUIT



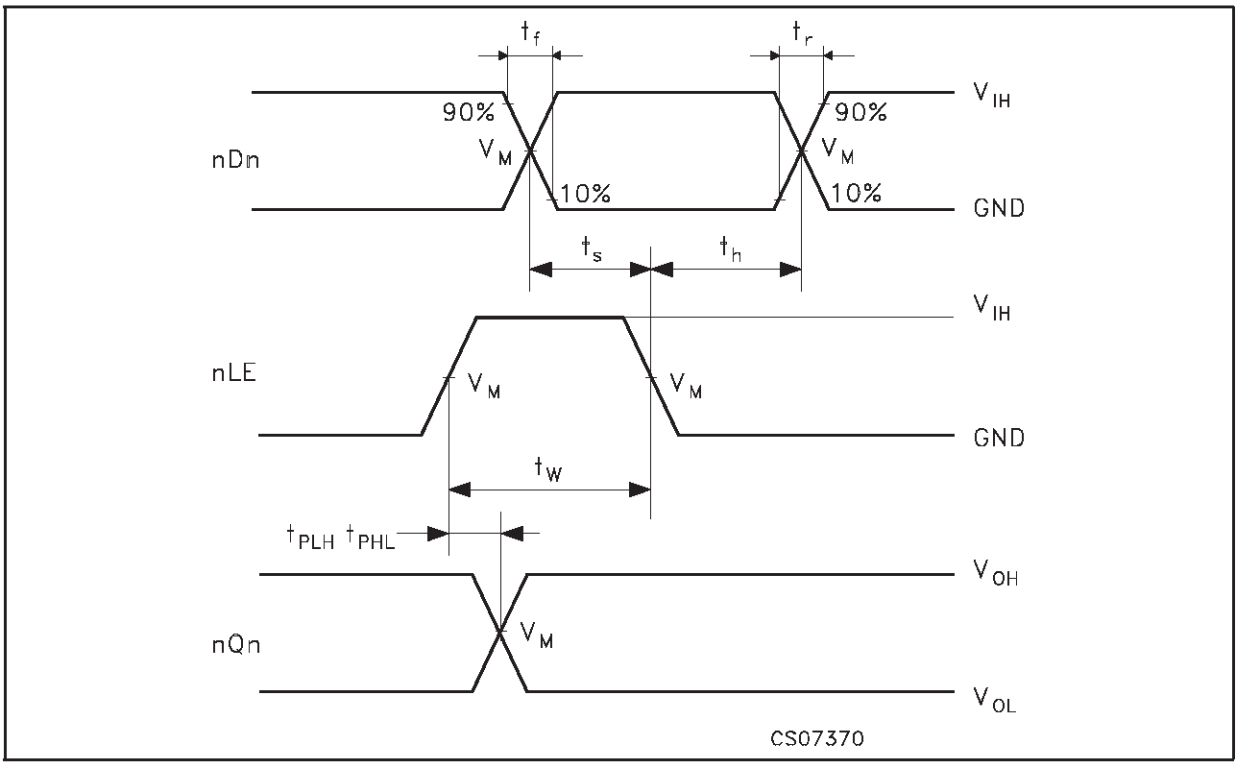
TEST	SWITCH
t_{PLH}, t_{PHL}	Open
t_{PZL}, t_{PLZ} (V_{CC} = 3.0 to 3.6V)	6V
t_{PZL}, t_{PLZ} (V_{CC} = 2.3 to 2.7V)	2V_{CC}
t_{PZH}, t_{PHZ}	GND

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

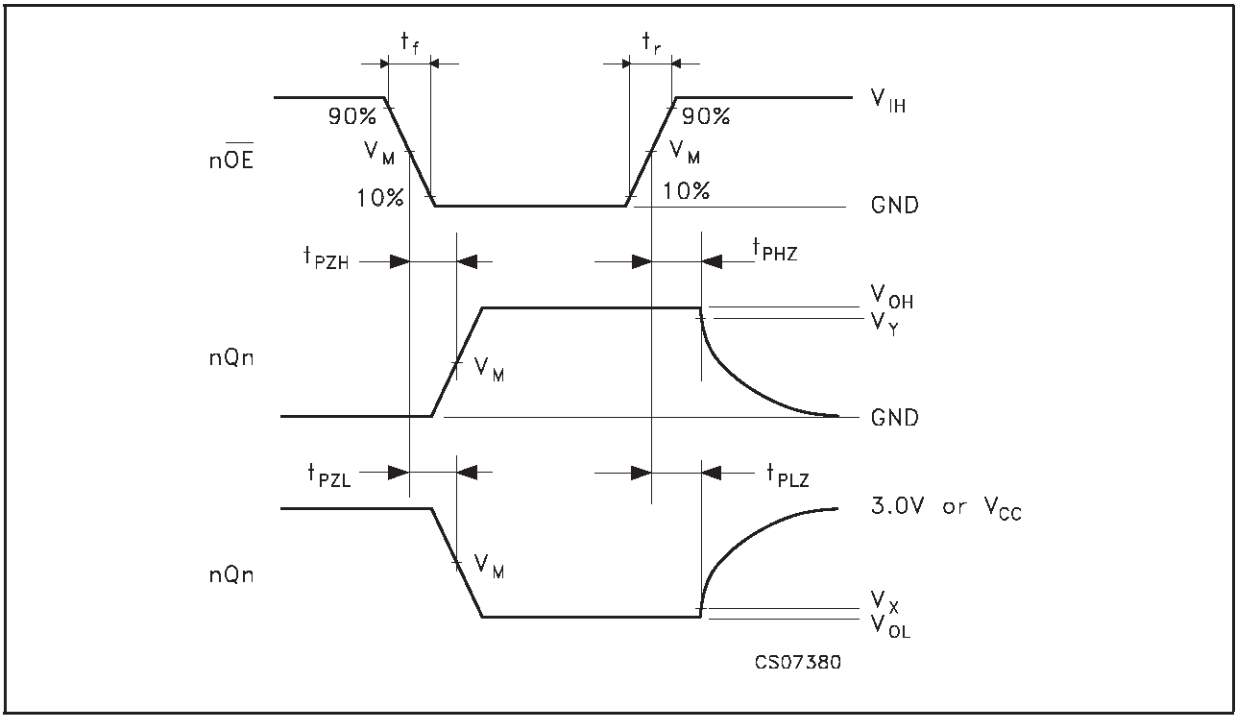
TEST CIRCUIT AND WAVEFORM SYMBOL VALUE

Symbol	V_{CC}			
	3.0 to 3.6V	2.7V	2.3 to 2.7V	1.65 to 1.95V
V_{IH}	2.7V	2.7V	V_{CC}	V_{CC}
V_M	1.5V	1.5V	V_{CC}/2	V_{CC}/2
V_X	V_{OL} +0.3V	V_{OL} +0.3V	V_{OL} +0.15V	V_{OL} +0.15V
V_Y	V_{OH} -0.3V	V_{OH} -0.3V	V_{OH} -0.15V	V_{OH} -0.15V
C_L	50pF	50pF	30pF	30pF
R_L=R_1	500Ω	500Ω	500Ω	1000Ω
t_f = t_r	<2.5ns	<2.5ns	<2.0ns	<2.0ns

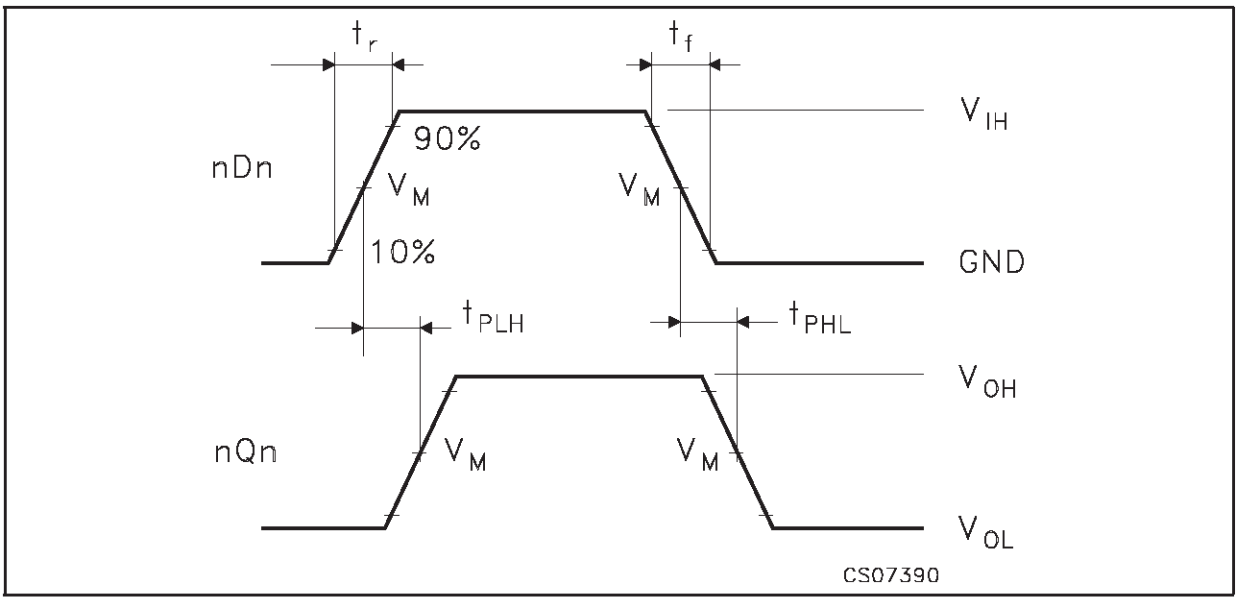
WAVEFORM 1 : LE TO Qn PROPAGATION DELAYS, LE MINIMUM PULSE WIDTH, Dn TO LE SETUP AND HOLD TIMES (f=1MHz; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIME (f=1MHz; 50% duty cycle)

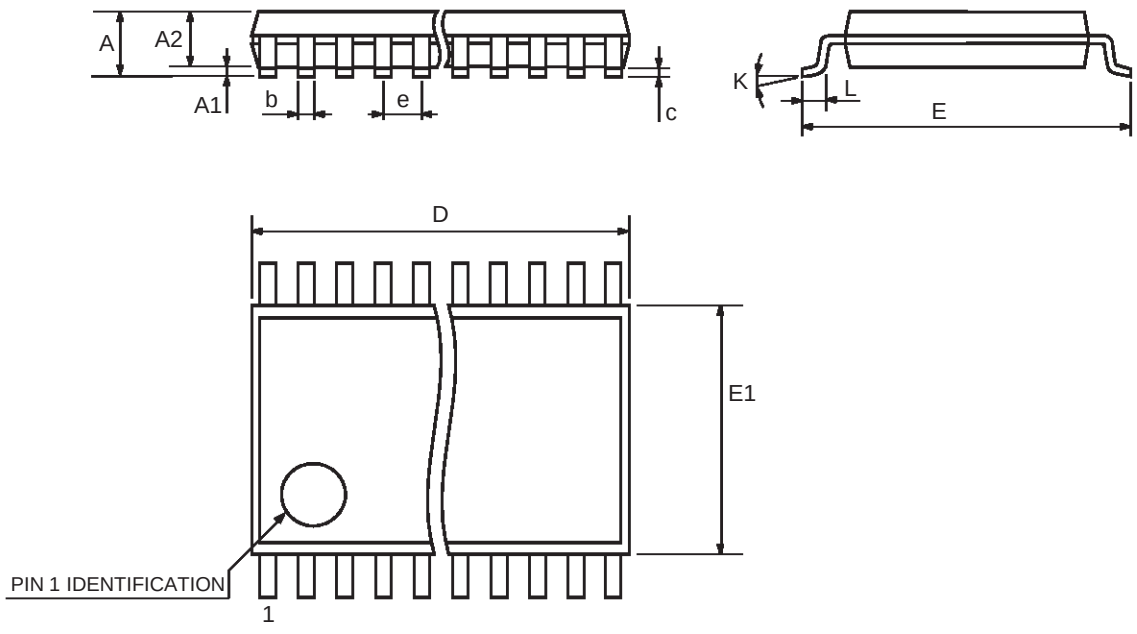


WAVEFORM 3 : PROPAGATION DELAY TIME (f=1MHz; 50% duty cycle)



TSSOP48 MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			1.2			0.047
A1	0.05		0.15	0.002		0.006
A2		0.9			0.035	
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4		12.6	0.408		0.496
E		8.1 BSC			0.318 BSC	
E1	6.0		6.2	0.236		0.244
e		0.5 BSC			0.0197 BSC	
K	0°		8°	0°		8°
L	0.50		0.75	0.020		0.030



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