Datasheet

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceed the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-35835
  - Class Q Military
  - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)

  • Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.
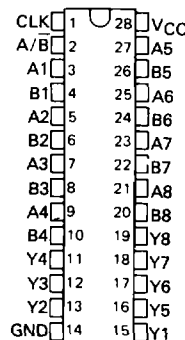
(TIM99604, TIM99606, TIM99607)

- Choice of Outputs:
  Three State ('LS604, 'LS606)
  Open-Collector ('LS607)

- **16 D-Type Registers, One for Each Data Input**

- **Multiplexer Selects Stored Data from Either A Bus or B Bus**

- Application Oriented:
  Maximum Speed ('LS604)
  Glitch-Free Operation ('LS606, 'LS607)

SN54LS604, SN54LS606, SN54LS607 . . . JD PACKAGE
SN74LS604, SN74LS606, SN74LS607 . . . JD OR N PACKAGE
(TOP VIEW)

```
        CLK [ 1    U  28 ] VCC
        A/B [ 2       27 ] A5
         A1 [ 3       26 ] B5
         B1 [ 4       25 ] A6
         A2 [ 5       24 ] B6
         B2 [ 6       23 ] A7
         A3 [ 7       22 ] B7
         B3 [ 8       21 ] A8
         A4 [ 9       20 ] B8
         B4 [ 10      19 ] Y8
         Y4 [ 11      18 ] Y7
         Y3 [ 12      17 ] Y6
         Y2 [ 13      16 ] Y5
        GND [ 14      15 ] Y1
```

description

The 'LS604, 'LS606, and 'LS607 multiplexed latches are ideal for storing data from two input buses, A and B, and providing the output bus with stored data from either the A or B register.

The clock loads data on the positive-going (low-level to high-level) transition. The clock pin also controls the active and high-impedance states of the outputs. When the clock pin is low, the outputs are in the high-impedance or off state. When the clock pin is high, the outputs are enabled.

The 'LS604 is optimized for high-speed operation. The 'LS606 and 'LS607 are especially designed to eliminate decoding voltage spikes.

These functions are ideal for interface from a 16-bit microprocessor to a 64K RAM board. The row and column addresses can be loaded as one word from the microprocessor and then multiplexed sequentially to the RAM during the time that RAS and CAS are active.

SN54LS604, SN54LS606, SN54LS607 . . . FK PACKAGE
(TOP VIEW)

```
              B1  A1 A/B CLK VCC A5  B5
               4   3  2   1  28  27 26
        A2 [ 5                      25 ] A6
        B2 [ 6                      24 ] B6
        A3 [ 7                      23 ] A7
        B3 [ 8                      22 ] B7
        A4 [ 9                      21 ] A8
        B4 [ 10                     20 ] B8
        Y4 [ 11                     19 ] Y8
              12 13 14 15 16 17 18
              Y3 Y2 GND Y1 Y5 Y6 Y7
```

TTL Devices 2

The SN54LS604, SN54LS606, and SN54LS607 are characterized for operation over the full military temperature range of −55°C to 125°C; the SN74LS604, SN74LS606, and SN74LS607 are characterized for operation from 0°C to 70°C.
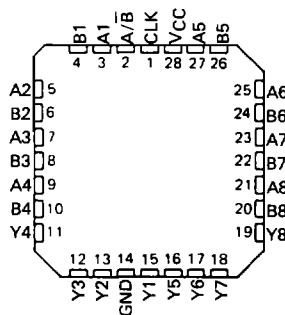
FUNCTION TABLE

INPUTS				OUTPUTS
A1-A8	B1-B8	SELECT A/B̄	CLOCK	Y1-Y8
A data	B data	L	↑	B data
A data	B data	H	↑	A data
X	X	X	L	Z or Off
X	X	L	H	B register stored data
X	X	H	H	A register stored data

H = high level (steady state)　　　　　　　　L = low level (steady state)

X = irrelevant　　　　　　　　　　　　　　　Z = high-impedance state

Off = H if pull-up resistor is connected to open-collector output

↑ = transistion from low to high level

TEXAS INSTRUMENTS

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schematics of inputs and outputs

EQUIVALENT OF A AND B INPUTS

EQUIVALENT OF CLOCK INPUTS

EQUIVALENT OF SELECT INPUTS

TYPICAL OF ALL OUTPUTS
('LS604, 'LS606)

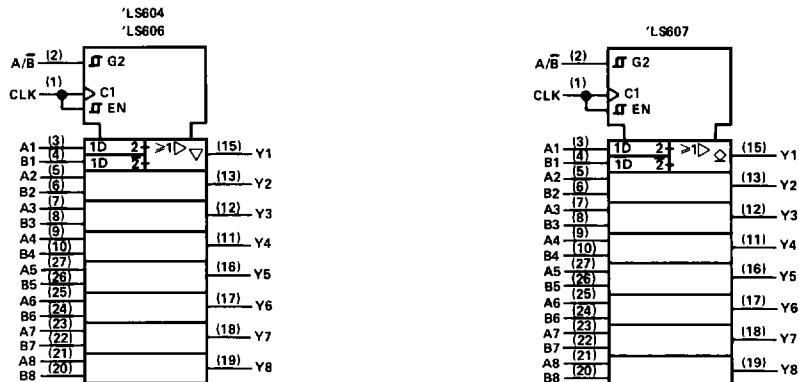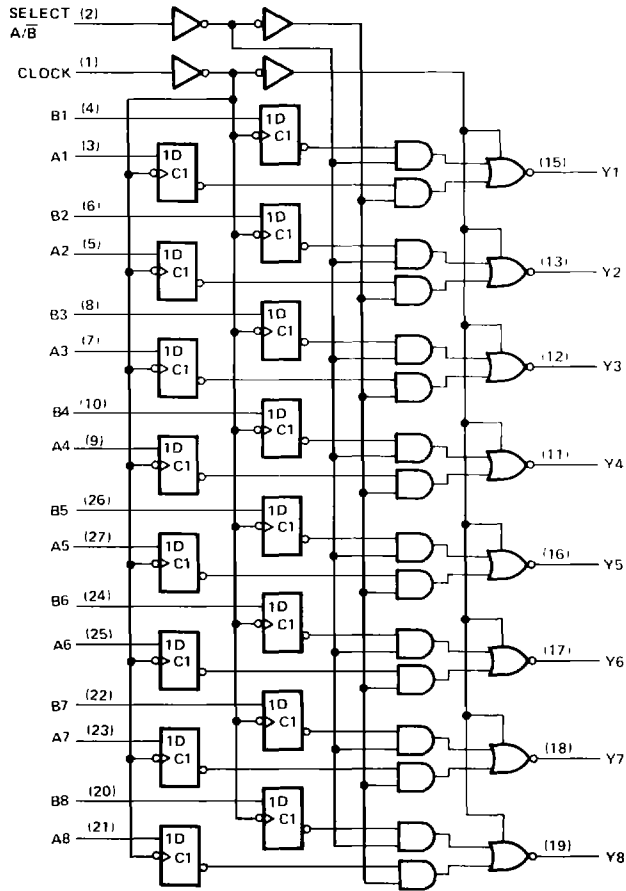TYPICAL OF ALL OUTPUTS
('LS607)
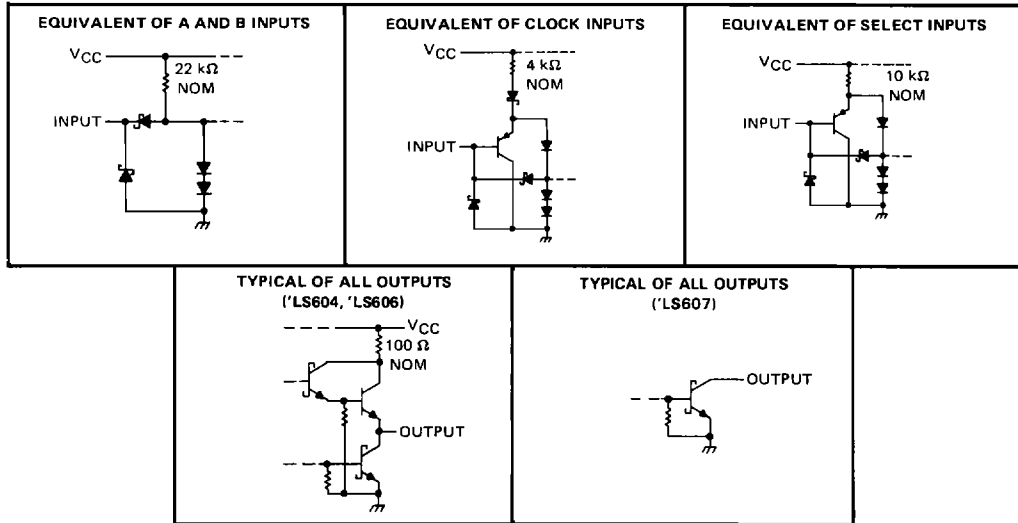
logic symbols†

†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12.
Pin numbers shown are for JD and N packages.

logic diagram (positive logic)

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TTL Devices

recommended operating conditions

	SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			−1			−2.6	mA
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20↑			20↑			ns
Hold time, t_h	0↑			0↑			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1: Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS604 SN54LS606			SN74LS604 SN74LS606			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 2.7 V			20			20	µA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_O = 0.4			−20			−20	µA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 7 V, A, B			0.1			0.1	mA
			CLK, SELECT			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V, A, B			20			20	µA
			CLK, SELECT			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.4 V, A, B			−0.4			−0.4	mA
			CLK, SELECT			−0.2			−0.2	
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		55	70		55	70	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C
§Note more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second
NOTE 2 I_{CC} is tested with all inputs grounded and all outputs open

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS604			'LS606			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Select A/$\overline{B}$			15	25		36	50	ns
t_{PHL}	(Data: A = H, B = L)			23	35		16	30	
t_{PLH}	Select A/$\overline{B}$	C_L = 45 pF, R_L = 667 Ω,		31	45		22	35	ns
t_{PHL}	(Data: A = L, B = H)	See Note 3		19	30		22	35	
t_{PZH}	Clock			19	30		27	40	ns
t_{PZL}				28	40		35	50	
t_{PHZ}	Clock	C_L = 5 pF, R_L = 667 Ω,		20	30		20	30	ns
t_{PLZ}		See Note 3		15	25		15	25	

t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, low-to-high-level output
t_{PZH} ≡ output enable time to high level
t_{PZL} ≡ output enable time to low level
t_{PHZ} ≡ output disable time from high level
t_{PLZ} ≡ output disable time from low level
NOTE 3· Load circuits and voltage waveforms are shown in Section 1.

recommended operating conditions

	SN54LS607			SN74LS607			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	4.5	5	5.5	4.75	5	5.25	V
High-level output voltage, V_{OH}			5.5			5.5	V
Low-level output current, I_{OL}			12			24	mA
Width of clock pulse, t_w	20			20			ns
Setup time, t_{su}	20†			20†			ns
Hold time, t_h	0†			0†			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTE 1. Voltage values are with respect to network ground terminal.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54LS607			SN74LS607			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.7			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, V_{OH} = 5.5 V			250			250	μA
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 12 mA	0.25		0.4	0.25		0.4	V
			I_{OL} = 24 mA				0.35		0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V	A, B			0.1			0.1	mA
			CLK, SELECT			0.1			0.1	
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V	A, B			20			20	μA
			CLK, SELECT			20			20	
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V	A, B			−0.4			−0.4	mA
			CLK, SELECT			−0.2			−0.2	
I_{CC}	Supply current	V_{CC} = MAX,	See Note 2		40	60		40	60	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
NOTE 2: I_{CC} is tested with all inputs grounded and all outputs open.

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TEST CONDITIONS	'LS607			UNIT
			MIN	TYP	MAX	
t_{PLH}	Select A/B̄			51	70	ns
t_{PHL}	(Data: A = H, B = L)			21	30	
t_{PLH}	Select A/B̄	C_L = 45 pF, R_L = 667 Ω, See Note 3		28	40	ns
t_{PHL}	(Data: A = L, B = H)			28	40	
t_{PLH}	Clock			30	45	ns
t_{PHL}				32	45	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1

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TTL Devices