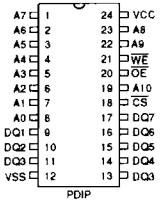
DESCRIPTION

The HY6116A is a high-speed, low power 2,048 x 8-bits CMOS static RAM fabricated using high performance CMOS process technology. This high reliability process coupled with innovative circuit design techniques, yields maximum access time of 85ns. The HY6116A has a data retention mode that guarantees data to remain valid at a minimum power supply voltage of 2.0 volt. Using CMOS technology, supply voltage from 2.0 to 5.5 volt have little effect on supply current in data retention mode. Reducing the supply voltage to minimize current drain is unnecessary with the HY6116A Series.

FEATURES

- **High speed -85/100/120/150ns (max.)**
- **Low power consumption**
  - **150mW typical operating**
  - **0.5μW typical standby (L-part)**
- **Battery backup : 2V Data Retention**
- **Fully Static Operation**
  - **No clock or refresh required.**
- **All inputs and outputs directly TTL compatible**
- **Tri-state output**
- **Standard Pin Configuration**
  HY6116AP : 600 mil, 24 pin PDIP

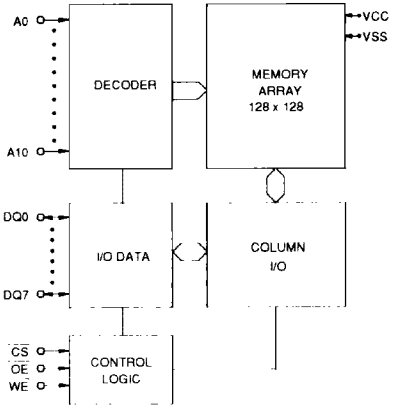
PIN CONNECTION



PIN DESCRIPTION

$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0-A10	Address Input
DQ0-DQ7	Data Input/Output
Vcc	Power
Vss	Ground

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS NOTE 1

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}, V_{IN}, V_{OUT}	Power Supply, Input/Output Voltage	– 0.5 to 7.0	V
T_{BIAS}	Temperature under Bias	– 10 to 125	°C
T_{STG}	Storage Temperature	– 55 to 125	°C
P_D	Power Dissipation	1.0	W
I_{OUT}	Data Output Current	50	mA
T_{SOLDER}	Lead Soldering Temperature & Time	260•10	°C•sec

NOTE :

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational of this specification is not implied. Exposure to absolute maximum rating conditions for extended period may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V_{CC}	Power Supply Voltage	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.2	3.5	6.0	V
V_{IL}	Input Low Voltage	–0.5[1]	-	0.4	V

NOTE :

1. V_{IL} = –3.5V for pulse width less than 20ns.

TRUTH TABLE

MODE	DQ OPERATION	$\overline{CS}$	$\overline{WE}$	$\overline{OE}$
Standby	High-Z	H	X	X
Output Disabled	High-Z	L	H	H
Read	Data Out	L	H	L
Write	Data In	L	L	X

NOTE : H= V_{IH}, L= V_{IL}, X= Don't Care

DC CHARACTERISTICS

(T_A= 0°C to 70°C)

SYMBOL	PARAMETER	TEST CONDITIONS		HY6116A MIN.	HY6116A TYP.	HY6116A MAX.	UNIT
I_{LI}	Input Leakage Current	$V_{SS} \leq V_{IN} \leq V_{CC}$		-2	-	2	μA
I_{LO}	Output Leakage Current	$V_{SS} \leq V_{OUT} \leq V_{CC}$ Output Disabled		-2	-	2	μA
I_{CC}	Operating Power Supply Current	$\overline{CS}$= V_{IL}, $I_{I/O}$= 0mA, Min. Duty Cycle= 100%		-	30	60	mA
I_{SB}	TTL Standby Current (TTL Inputs)	$\overline{CS}$= V_{IH}		-	0.5	3	mA
I_{SB1}	CMOS Standby Current (CMOS Inputs)	$\overline{CS} \geq V_{CC}$ -0.2V		-	4	50	μA
			L	-	0.1	5	μA
V_{OL}	Output Low Voltage	I_{OL}= 4.0mA		-	-	0.4	V
V_{OH}	Output High Voltage	I_{OH}= -1.0mA		2.4	-	-	V

NOTE :

1. Typical values are at V_{CC}= 5.0V, T_A= 25°C and specified loading.

AC CHARACTERISTICS

(TA= 0°C to 70°C)

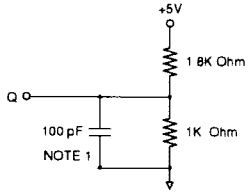
#	SYMBOL	PARAMETER	HY6116A								UNIT
			-85		-10		-12		-15		
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
	READ CYCLE										
1	tRC	Read Cycle Time	85	-	100	-	120	-	150	-	ns
2	tAA	Address Access Time	-	85	-	100	-	120	-	150	ns
3	tACS	Chip Select Access Time	-	85	-	100	-	120	-	150	ns
4	tOE	Output Enable to Output Valid	-	45	-	50	-	55	-	60	ns
5	tCLZ	Chip Select to Low-Z Output	10	-	10	-	10	-	10	-	ns
6	tOLZ	Output Enable to Low-Z Output	10	-	10	-	10	-	10	-	ns
7	tCHZ	Chip Disable to High-Z Output	0	40	0	40	0	40	0	50	ns
8	tOHZ	Output Disable to High-Z Output	0	40	0	40	0	40	0	50	ns
9	tOH	Output Hold from Address change	10	-	10	-	10	-	15	-	ns
	WRITE CYCLE NOTE 3										
10	tWC	Write Cycle Time	85	-	100	-	120	-	150	-	ns
11	tCW	Chip Select to Write End	60	-	65	-	70	-	90	-	ns
12	tAW	Address Valid to Write End	70	-	80	-	105	-	120	-	ns
13	tAS	Address Set-up Time	0	-	0	-	0	-	0	-	ns
14	tWP	Write Pulse Width	55	-	60	-	70	-	80	-	ns
15	tWR	Write Recovery Time	0	-	0	-	0	-	0	-	ns
16	tWHZ	Write to High-Z Output	0	30	0	30	0	35	0	40	ns
17	tDW	Data Set up to Write End	30	-	30	-	35	-	40	-	ns
18	tDH	Data Hold from Write End	0	-	0	-	0	-	0	-	ns
19	tOW	Output Active from Write End	10	-	10	-	10	-	10	-	ns

AC TEST CONDITIONS

(TA = 0°C to 70°C)

Parameter	Value
Input Pulse Level	0.8V to 2.4V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	1.5V

AC TEST LOADS



NOTE :
1. Including jig and scope capacitance.

CAPACITANCE

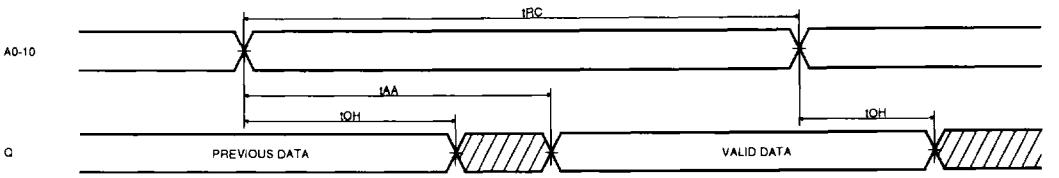
(TA= 25°C, f= 1MHz)

SYMBOL	PARAMETER	CONDITION	MAX.	UNIT
C_{IN}	Input Capacitance	V_{IN}= 0V	6	pF
$C_{I/O}$	Input/Output Capacitance	$V_{I/O}$= 0V	8	pF

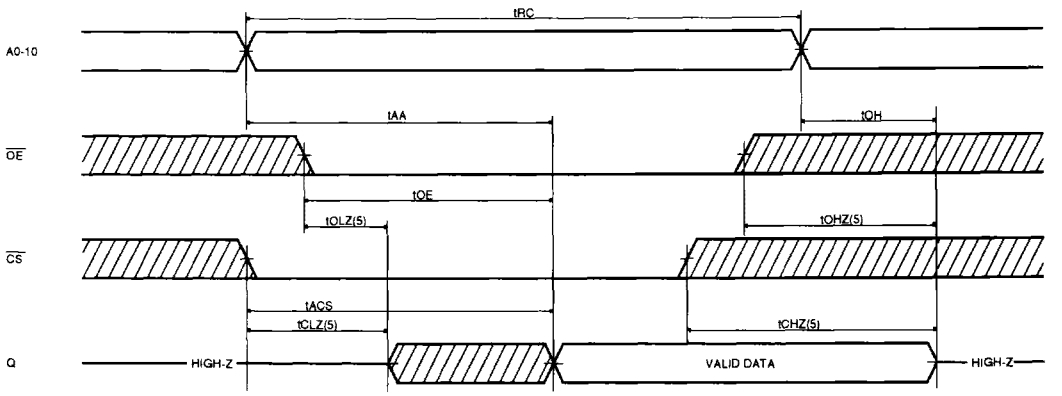
NOTE :
1. This parameter is determined by device characterization but is not production tested.

TIMING DIAGRAM

READ CYCLE 1 NOTE 1,2,4

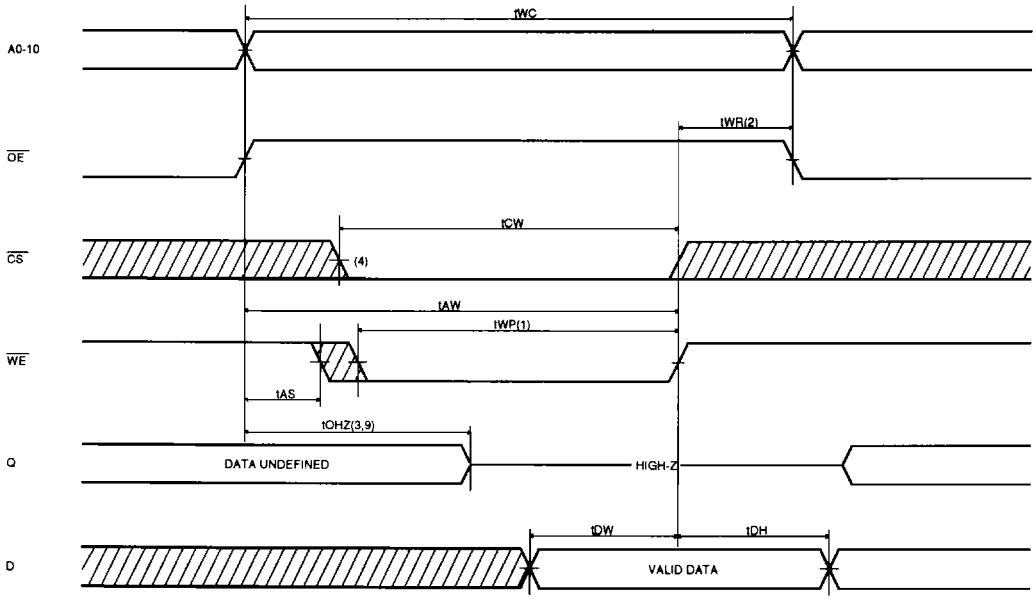


READ CYCLE 2 NOTE 1,3,4

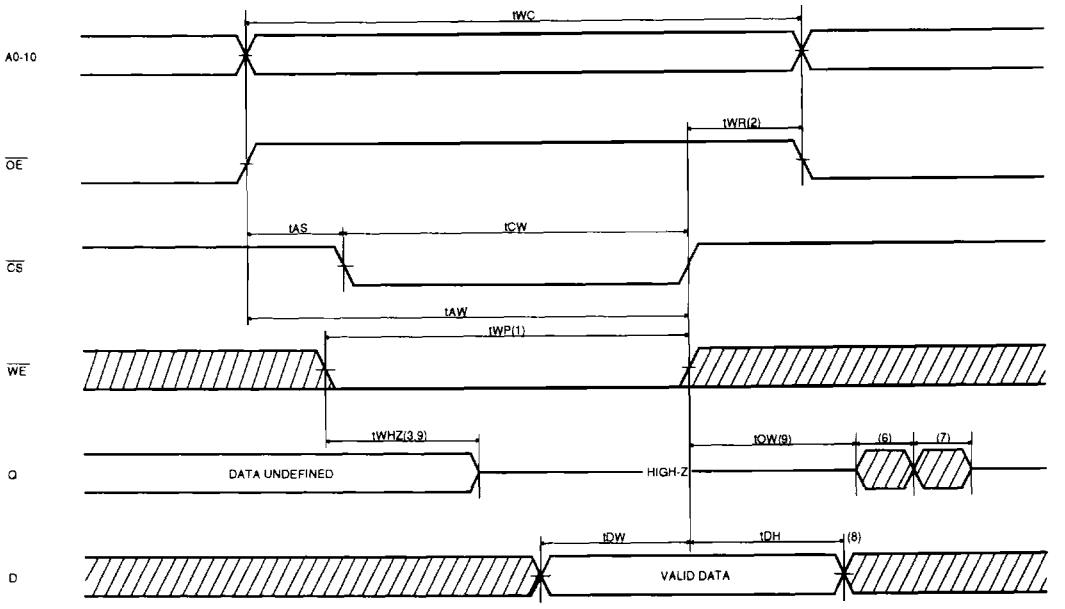


NOTES :
1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously selected $\overline{CS}$= VIL
3. Addresses are valid prior to coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$= VIL
5. Transition is measured ± 500mV from steady state.
   This parameter is sampled and not 100% tested.

WRITE CYCLE 1 NOTE 10



WRITE CYCLE 2 NOTE 5, 10



NOTES :

1. A write occurs during the overlap (tWP) of low $\overline{CS}$ and low $\overline{WE}$.
2. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high at the end of write cycle.
3. During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low Transitions or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. $\overline{OE}$ is continuously low ($\overline{OE}$= VIL)
6. Q is the same phase of write data of this write cycle.
7. Q is the read data of next address.
8. If $\overline{CS}$ is low during this period, DQ pins are in the output state.
   Then the data input signals of opposite phase to the outputs must not be applied to them.
9. Transition is measured ± 500mV from steady state.
   This parameter is sampled and not 100% tested.
10. $\overline{WE}$ must be high during all address transitions.

DATA RETENTION CHARACTERISTICS

(TA = 0°C to 70°C)

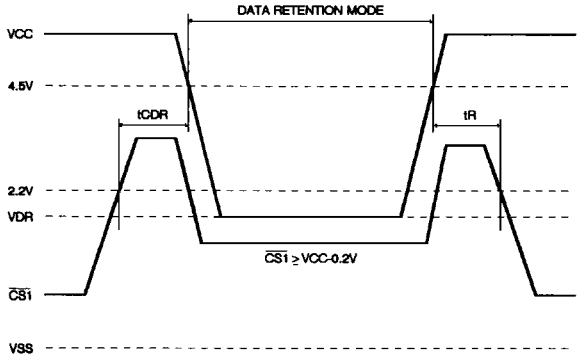
SYMBOL	PARAMETER	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
V_{DR}	V_{CC} for retention of data	V_{IN} = 0 to V_{CC}, $\overline{CS}$ ≥ V_{CC}-0.2V	2.0	-	5.5	V
I_{CCDR}	Data Retention Current	V_{CC} = 3.0V, V_{IN} = 0 to V_{CC} $\overline{CS}$ ≥ V_{CC}-0.2V	-	0.05	2.0	μA
t_{CDR}	Chip Disable to Data Retention Time	See Data Retention Timing Diagram	0	-	-	ns
t_R	Operating Recovery Time		t_{RC}[1]	-	-	ns

NOTE :

1. t_{RC} = Read Cycle Time.

DATA RETENTION TIMING DIAGRAM

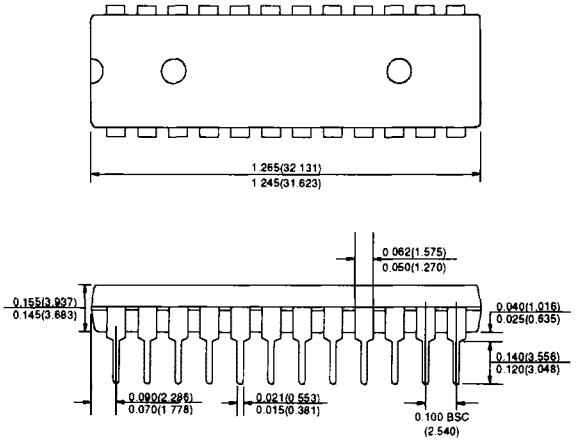
V_{CC} = 5.0V ± 10%

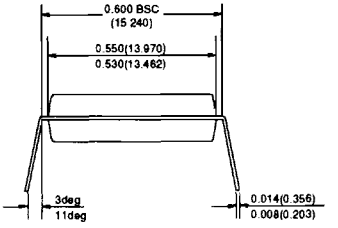


PACKAGE INFORMATION

600 mil 24 pin Plastic Dual In Line Package (P)

UNIT : INCH(mm) MAX/MIN





ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY6116AP	85/100/120/150		PDIP
HY6116ALP	85/100/120/150	L-part	PDIP