Integrated Device Technology, Inc.

CMOS PARALLEL-TO-SERIAL FIFO 2,048 x 9 and 4,096 x 9

IDT72131 IDT72141

FEATURES:

- 35ns parallel port access time, 45ns cycle time
- 50MHz serial port shift rate
- Expandable in depth and width with no external components
- Programmable word lengths including 7-9, 16-18, 32-36 bit using Flexishift™ serial output without using any additional components
- Multiple status flags: Full, Almost-Full (1/8 from full), Half-Full, Almost Empty (1/8 from empty), and Empty
- Asynchronous and simultaneous read and write operations
- Dual-Port zero fall-through architecture
- Retransmit capability in single device mode
- Produced with high-performance, low power CMOS technology
- Available in 28-pin plastic DIP
- Industrial temperature range (–40°C to +85°C) is available

DESCRIPTION:

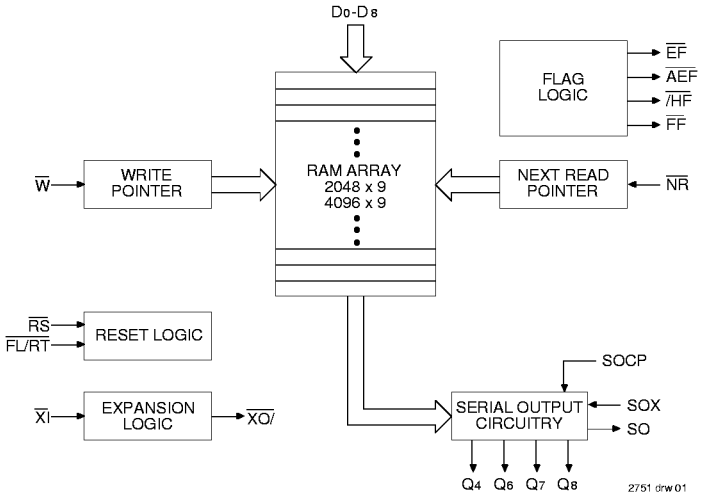
The IDT72131/72141 are high-speed, low power parallel-to-serial FIFOs. These FIFOs are ideally suited to serial communications applications, tape/disk controllers, and local area networks (LANs). These devices can be configured with the IDTs serial-to-parallel FIFOs (IDT72132/72142) for bidirectional serial data buffering.

The FIFO has a 9-bit parallel input port and a serial output port. Wider and deeper parallel-to-serial data buffers can be built using multiple IDT72131/72141 chips. IDTs unique Flexishift serial expansion logic (SOX, $\overline{NR}$) makes width expansion possible with no additional components. These FIFOs will expand to a variety of word widths including 8, 9, 16, and 32 bits. These devices can also be directly connected for depth expansion.

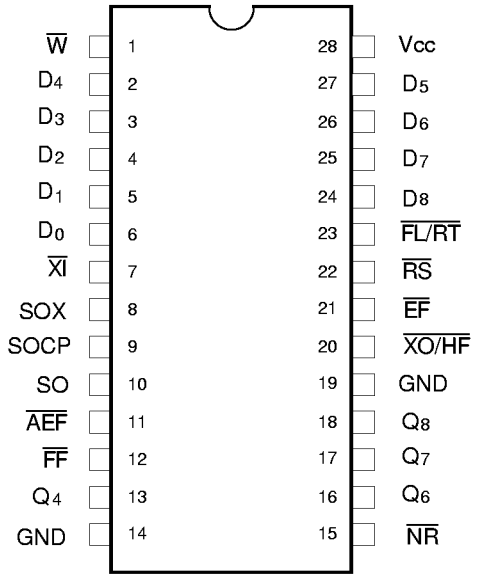
Five flags are provided to monitor the FIFO. The full and empty flags prevent any FIFO data overflow or underflow conditions. The Almost-Full (7/8), Half-Full, and Almost-Empty (1/8) flags signal memory utilization within the FIFO.

The IDT72131/72141 is fabricated using IDTs high-speed submicron CMOS technology.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



PLASTIC DIP (P28-1, order code: P)
TOP VIEW

PIN DESCRIPTIONS

Symbol	Name	I/O	Description
D_0–D_8	Inputs	I	Data inputs for 9-bit wide data.
$\overline{RS}$	Reset	I	When $\overline{RS}$ is set LOW, internal READ and WRITE pointers are set to the first location of the RAM array. $\overline{HF}$ and $\overline{FF}$ go HIGH, and $\overline{AEF}$ and $\overline{EF}$ go LOW. A reset is required before an initial WRITE after power-up. $\overline{W}$ must be HIGH and SOCP must be LOW during $\overline{RS}$ cycle.
$\overline{W}$	Write	I	A write cycle is initiated on the falling edge of WRITE if the Full Flag ($\overline{FF}$) is not set. Data set-up and hold times must be adhered to with respect to the rising edge of WRITE. Data is stored in the RAM array sequentially and independently of any ongoing read operation.
SOCP	Serial Output Clock	I	A serial bit read cycle is initiated on the rising edge of SOCP if the Empty Flag ($\overline{EF}$) is not set. In both Depth and Serial Word Width Expansion modes, all of the SOCP pins are tied together.
$\overline{NR}$	Next Read	I	To program the Serial Out data word width , connect $\overline{NR}$ with one of the Data Set pins (Q_4, Q_6, Q_7 and Q_8). For example, $\overline{NR}$ - Q_7 programs for a 8-bit Serial Out word width.
$\overline{FL}/\overline{RT}$	First Load/ Retransmit	I	This is a dual purpose input. In the single device configuration ($\overline{XI}$ grounded), activating retransmit ($\overline{FL}/\overline{RT}$-LOW) will set the internal READ pointer to the first location. There is no effect on the WRITE pointer. $\overline{W}$ must be high and SOCP must be low before setting $\overline{FL}/\overline{RT}$ LOW. Retransmit is not compatible with depth expansion. In the depth expansion configuration, $\overline{FL}/\overline{RT}$ grounded indicates the first activated device.
$\overline{XI}$	Expansion In	I	In the single device configuration, $\overline{XI}$ is grounded. In depth expansion or daisy chain expansion, $\overline{XI}$ is connected to $\overline{XO}$ (expansion out) of the previous device.
SOX	Serial Output Expansion	I	In the Serial Output Expansion mode, the SOX pin of the least significant device is tied HIGH. The SOX pin of all other devices is connected to the Q_8 pin of the previous device. Data is then clocked out least significant bit first. For single device operation, SOX is tied HIGH.
SO	Serial Output	O	Serial data is output on the Serial Output (SO) pin. Data is clocked out Least Significant Bit first. In the Serial Width Expansion mode the SO pins are tied together and each SO pin is tristated at the end of the byte.
$\overline{FF}$	Full Flag	O	When $\overline{FF}$ goes LOW, the device is full and further WRITE operations are inhibited. When $\overline{FF}$ is HIGH, the device is not full.
$\overline{EF}$	Empty Flag	O	When $\overline{EF}$ goes LOW, the device is empty and further READ operations are inhibited. When $\overline{EF}$ is HIGH, the device is not empty. See the description on page 6 for more details.
$\overline{AEF}$	Almost-Empty/ Almost-Full Flag	O	When $\overline{AEF}$ is LOW, the device is empty to 1/8 full or 7/8 to completely full. When $\overline{AEF}$ is HIGH, the device is greater than 1/8 full, but less than 7/8 full.
$\overline{XO}/\overline{HF}$	Expansion Out/ Half-Full Flag	O	This is a dual-purpose output. In the single device configuration ($\overline{XI}$ grounded), the device is more than half full when HF is LOW. In the depth expansion configuration ($\overline{XO}$ connected to $\overline{XI}$ of the next device), a pulse is sent from $\overline{XO}$ to $\overline{XI}$ when the last location in the RAM array is filled.
Q_4, Q_6, Q_7 and Q_8	Data Set	O	The appropriate Data Set pin (Q_4, Q_6, Q_7 and Q_8) is connected to $\overline{NR}$ to program the Serial Out data word width. For example: Q_6 - $\overline{NR}$ programs a 7-bit word width, Q_8 - $\overline{NR}$ programs a 9-bit word width, etc.
V_{CC}	Power Supply		Single Power Supply of 5V.
GND	Ground		Single ground at 0V.

2751 tbl 01

STATUS FLAGS

Number of Words in FIFO					
IDT72131	IDT72141	$\overline{FF}$	$\overline{AEF}$	$\overline{HF}$	$\overline{EF}$
0	0	H	L	H	L
1-255	1-511	H	L	H	H
256-1,024	512-2,048	H	H	H	H
1,025-1,792	2,049-3,584	H	H	L	H
1,793-2,047	3,585-4,095	H	L	L	H
2,048	4,096	L	L	L	H

2751 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	–50 to +50	mA

NOTE: 2751 tbl 03

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Commercial Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage Commercial	2.0	—	—	V
V_{IL}(1)	Input Low Voltage	—	—	0.8	V
T_A	Operating Temperature Commercial	0	—	70	°C

NOTE: 2751 tbl 04

1. 1.5V undershoots are allowed for 10ns once per cycle.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	10	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	12	pF

NOTE: 2751 tbl 05

1. Characterized values, not currently tested.

DC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	IDT72131 IDT72141 Commercial			Unit
		Min.	Typ.	Max.	
I_{IL}(1)	Input Leakage Current (Any Input)	–1	—	1	µA
I_{OL}(2)	Output Leakage Current	–10	—	10	µA
V_{OH}	Output Logic "1" Voltage, I_{OUT} = –8mA	2.4	—	—	V
V_{OL}	Output Logic "0" Voltage I_{OUT} = 16mA	—	—	0.4	V
I_{CC1}(3)	Active Power Supply Current	—	90	140	mA
I_{CC2}(3,4)	Standby Current ($\overline{W}$ = $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = V_{IH}; SOCP = V_{IL})	—	8	12	mA
I_{CC3}(3,4)	Power Down Current	—	—	2	mA

NOTES: 2751 tbl 06

1. Measurements with 0.4 ≤ V_{IN} ≤ V_{CC}.
2. SOCP ≤ V_{IL}, 0.4 ≤ V_{OUT} ≤ V_{CC}.
3. Tested with outputs open (I_{OUT} = 0).
4. $\overline{RS}$ = $\overline{FL}/\overline{RT}$ = $\overline{W}$ = V_{CC} -0.2V; SOCP ≤ 0.2V; all other inputs = V_{CC} - 0.2V or GND + 0.2V, which toggle at 20 MHz.

AC ELECTRICAL CHARACTERISTICS

(Commercial: V_{CC} = 5.0V ± 10%, T_A = 0°C to +70°C)

Symbol	Parameter	Commercial				Unit
		IDT72131L35 IDT72141L35		IDT72131L50 IDT72141L50		
		Min.	Max.	Min.	Max.	
t_S	Parallel Shift Frequency	—	22.2	—	15	MHz
t_{SOCP}	Serial-Out Shift Frequency	—	50	—	40	MHz
PARALLEL INPUT TIMINGS						
t_{DS}	Data Set-up Time	18	—	30	—	ns
t_{DH}	Data Hold Time	0	—	5	—	ns
t_{WC}	Write Cycle Time	45	—	65	—	ns
t_{WPW}	Write Pulse Width	35	—	50	—	ns
t_{WR}	Write Recovery Time	10	—	15	—	ns
t_{WEF}	Write High to $\overline{EF}$ HIGH	—	30	—	45	ns
t_{WFF}	Write Low to $\overline{FF}$ LOW	—	30	—	45	ns
t_{WF}	Write Low to Transitioning $\overline{HF}$, $\overline{AEF}$	—	45	—	65	ns
t_{WPF}	Write Pulse Width After $\overline{FF}$ HIGH	35	—	50	—	ns
SERIAL OUTPUT TIMINGS						
t_{SOHZ}	SOCP Rising Edge to SO at High-Z[1]	5	16	5	26	ns
t_{SOLZ}	SOCP Rising Edge to SO at Low-Z[1]	5	22	5	22	ns
t_{SOPD}	SOCP Rising Edge to Valid Data on SO	—	18	—	18	ns
t_{SOX}	SOX Set-up Time to SOCP Rising Edge	5	—	5	—	ns
t_{SOCW}	Serial In Clock Width HIGH/LOW	8	—	10	—	ns
t_{SOCEF}	SOCP Rising Edge (Bit 0 - Last Word) to $\overline{EF}$ LOW	—	20	—	25	ns
t_{SOCFF}	SOCP Rising Edge to $\overline{FF}$ HIGH	—	30	—	40	ns
t_{SOCF}	SOCP Rising Edge to $\overline{HF}$, $\overline{AEF}$, HIGH	—	30	—	40	ns
t_{REFSO}	Recovery Time SOCP After $\overline{EF}$ HIGH	35	—	50	—	ns
RESET TIMINGS						
t_{RSC}	Reset Cycle Time	45	—	65	—	ns
t_{RS}	Reset Pulse Width	35	—	50	—	ns
t_{RSS}	Reset Set-up Time	35	—	50	—	ns
t_{RSR}	Reset Recovery Time	10	—	15	—	ns
t_{RSF1}	Reset to $\overline{EF}$ and $\overline{AEF}$ LOW	—	45	—	65	ns
t_{RSF2}	Reset to $\overline{HF}$ and $\overline{FF}$ HIGH	—	45	—	65	ns
t_{RSQL}	Reset to Q LOW	20	—	35	—	ns
t_{RSQH}	Reset to Q HIGH	20	—	35	—	ns
RETRANSMIT TIMINGS						
t_{RTC}	Retransmit Cycle Time	45	—	65	—	ns
t_{RT}	Retransmit Pulse Width	35	—	50	—	ns
t_{RTS}	Retransmit Set-up Time	35	—	50	—	ns
t_{RTR}	Retransmit Recovery Time	10	—	15	—	ns
DEPTH EXPANSION MODE TIMINGS						
t_{XOL}	Read/Write to $\overline{XO}$ LOW	—	35	—	50	ns
t_{XOH}	Read/Write to $\overline{XO}$ HIGH	—	35	—	50	ns
t_{XI}	$\overline{XI}$ Pulse Width	35	—	50	—	ns
t_{XIR}	$\overline{XI}$ Recovery Time	10	—	10	—	ns
t_{XIS}	$\overline{XI}$ Set-up Time	15	—	15	—	ns

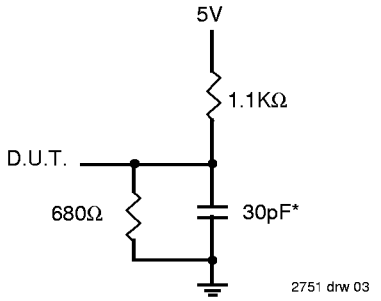
NOTE:
1. Guaranteed by design minimum times, not tested.

2751 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figure A

2751 tbl 08



or equivalent circuit

Figure A. Ouput Load
*Including jig and scope capacitances

FUNCTIONAL DESCRIPTION

Parallel Data Input

The data is written into the FIFO in parallel through the D_{0-8} input data lines. A write cycle is initiated on the falling edge of the Write ($\overline{W}$) signal provided the Full Flag ($\overline{FF}$) is not asserted. If the $\overline{W}$ signal changes from HIGH-to-LOW and the Full-Flag ($\overline{FF}$) is already set, the write line is inhibited internally from incrementing the write pointer and no write operation occurs.

Data set-up and hold times must be met with respect to the rising edge of Write. The data is written to the RAM at the write pointer. On the rising edge of $\overline{W}$, the write pointer is incremented. Write operations can occur simultaneously or asynchronously with read operations.

Serial Data Output

The serial data is output on the SO pin. The data is clocked out on the rising edge of SOCP providing the Empty Flag ($\overline{EF}$) is not asserted. If the Empty Flag is asserted then the next data word is inhibited from moving to the output register and being clocked out by SOCP. NOTE: SOCP should not be clocked once the last bit of the last word has been clocked out. If it is, then two things will occur. One, the SO pin will go High-Z and two, SOCP will be out of sync with Next Read ($\overline{NR}$).

The serial word is shifted out Least Significant Bit first, that is the first bit will be D0, then D1 and so on up to the serial word width. The serial word width must be programmed by connecting the appropriate Data Set line (Q4, Q6, Q7 or Q8) to the $\overline{NR}$ input. The Data Set lines are taps off a digital delay line. Selecting one of these taps, programs the width of the serial word to be read and shifted out.

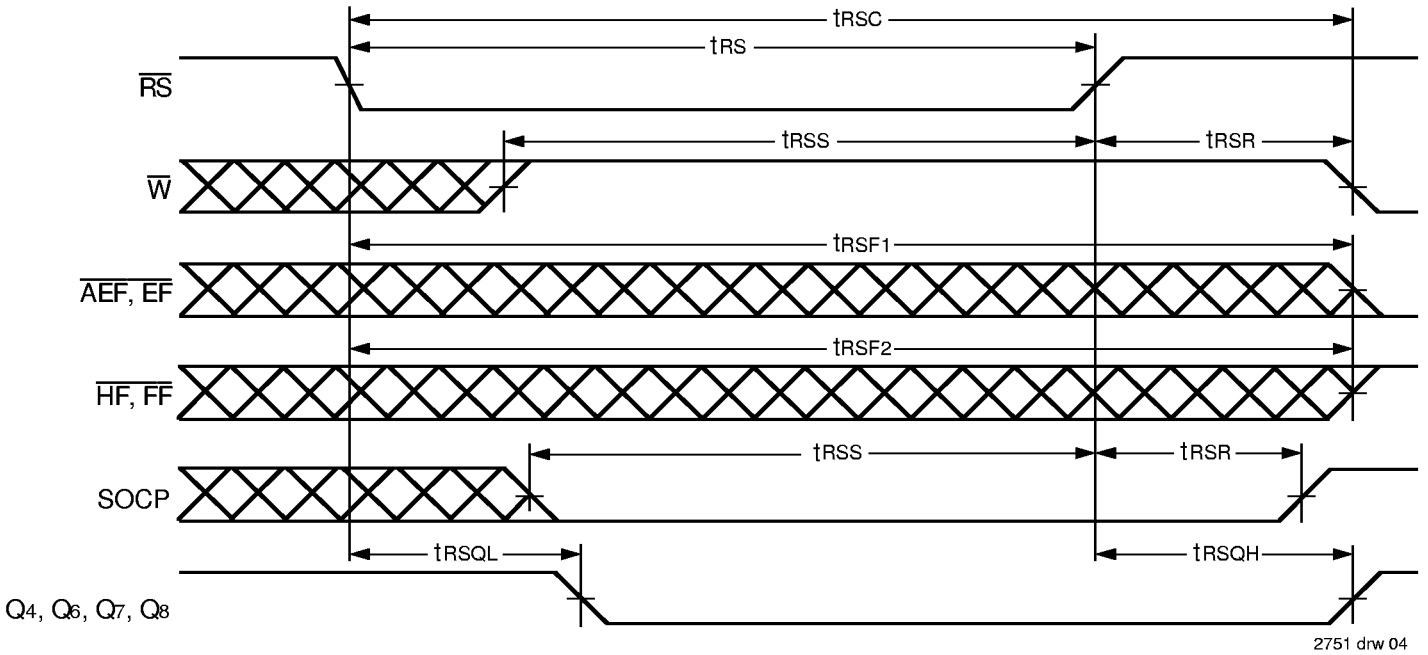


Figure 1. Reset

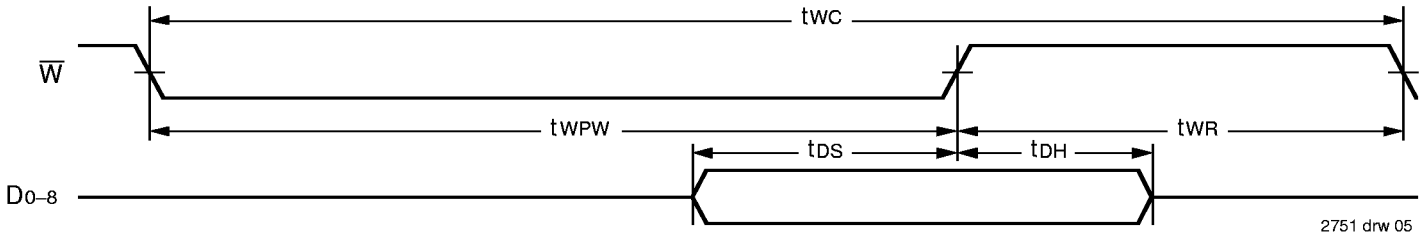
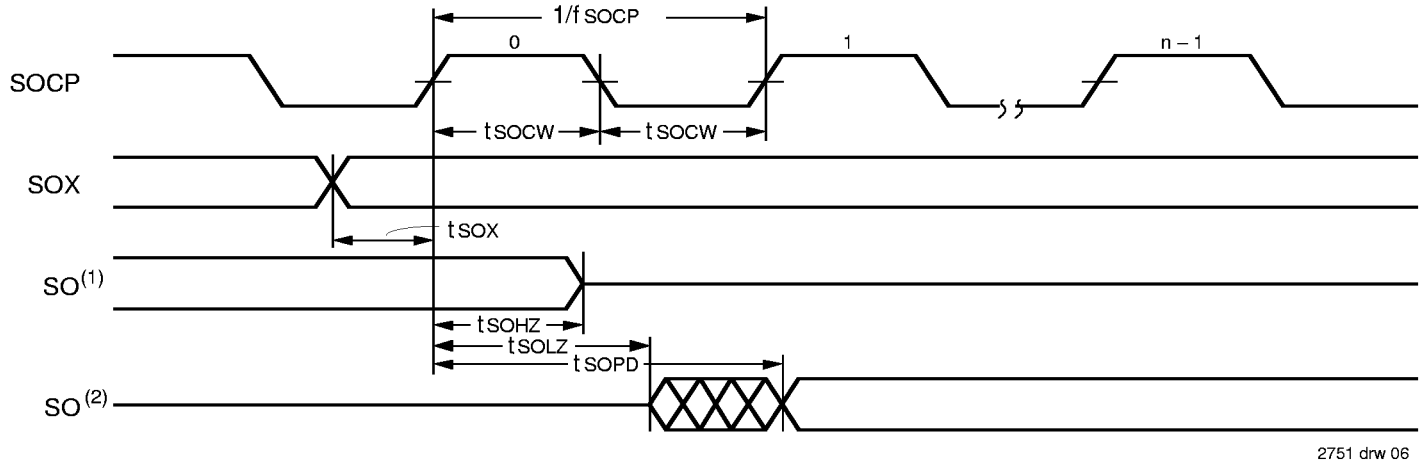


Figure 2. Write Operation



NOTES:
1. This timing applies to the Active Device in Width Expansion Mode.
2. This timing applies to Single Device Mode at Empty Boundary ($\overline{EF}$ = LOW) and the Next Active Device in Width Expansion Mode.

Figure 3. Read Operation

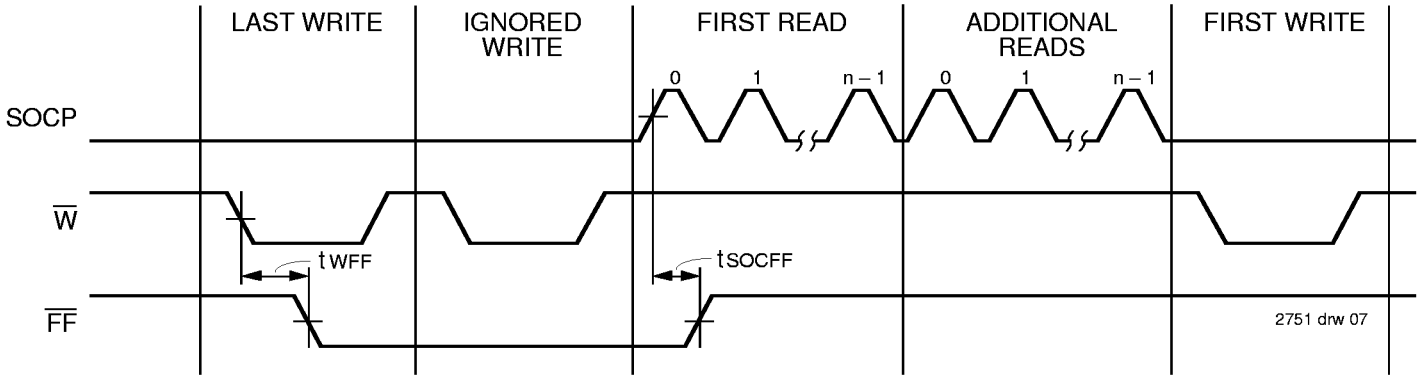
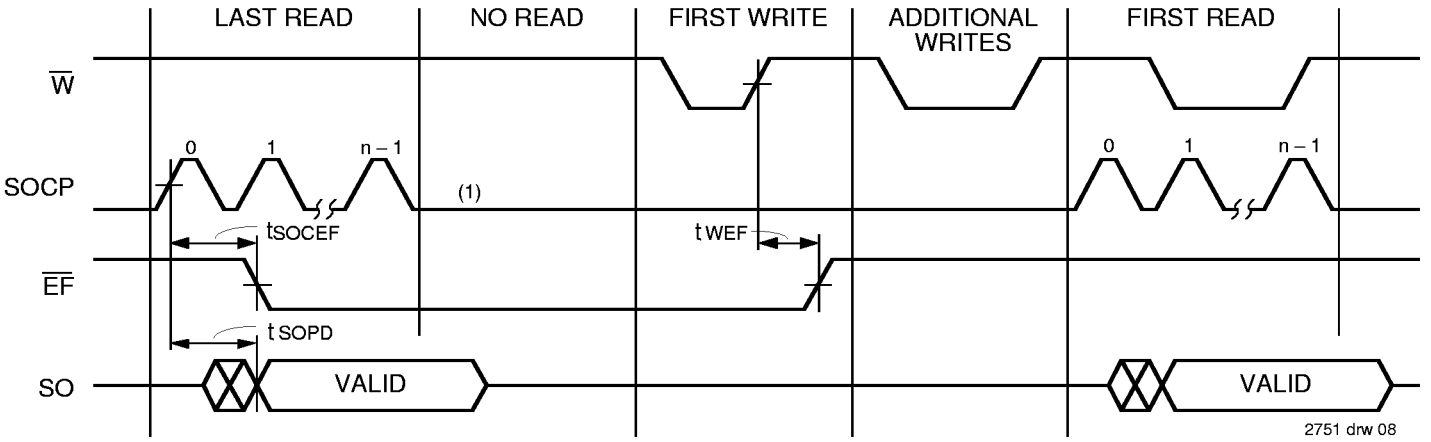
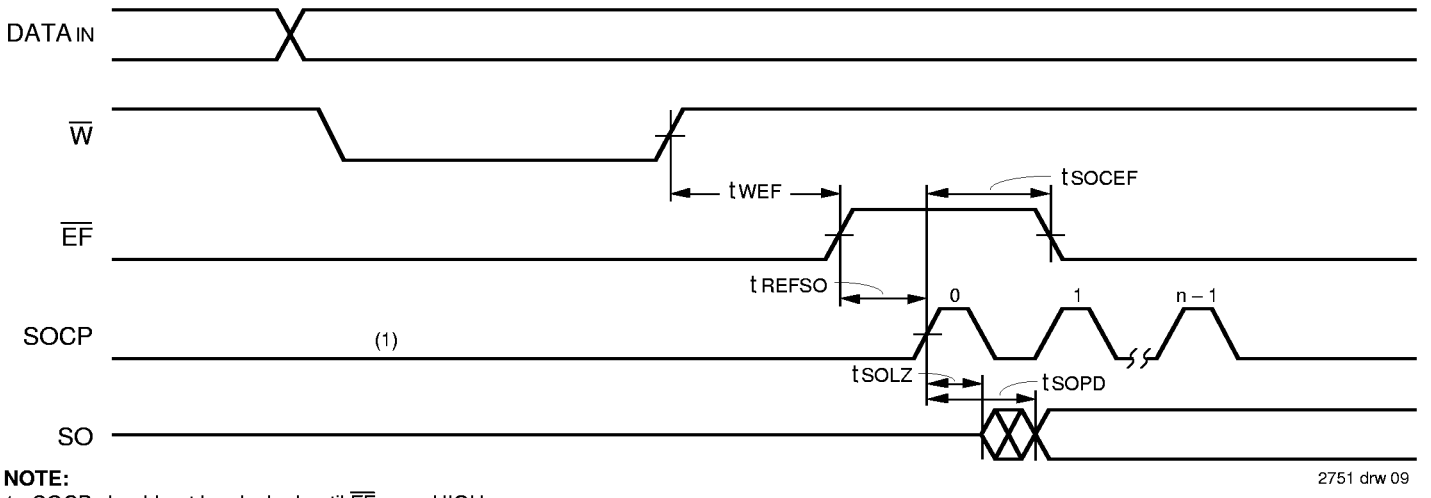


Figure 4. Full Flag from Last Write to First Read



NOTE:
1. Once $\overline{EF}$ has gone LOW and the last bit of the final word has been shifted out, SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 5. Empty Flag from Last Read to First Write



NOTE:
1. SOCP should not be clocked until $\overline{EF}$ goes HIGH.

Figure 6. Empty Boundary Condition Timing

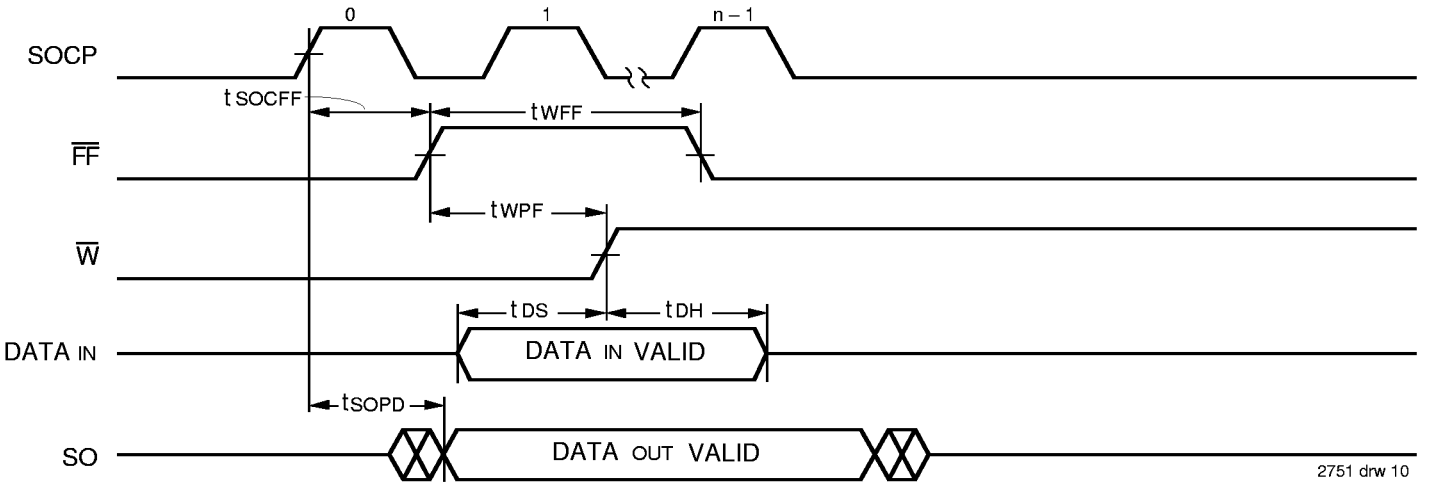


Figure 7. Full Boundry Condition Timing

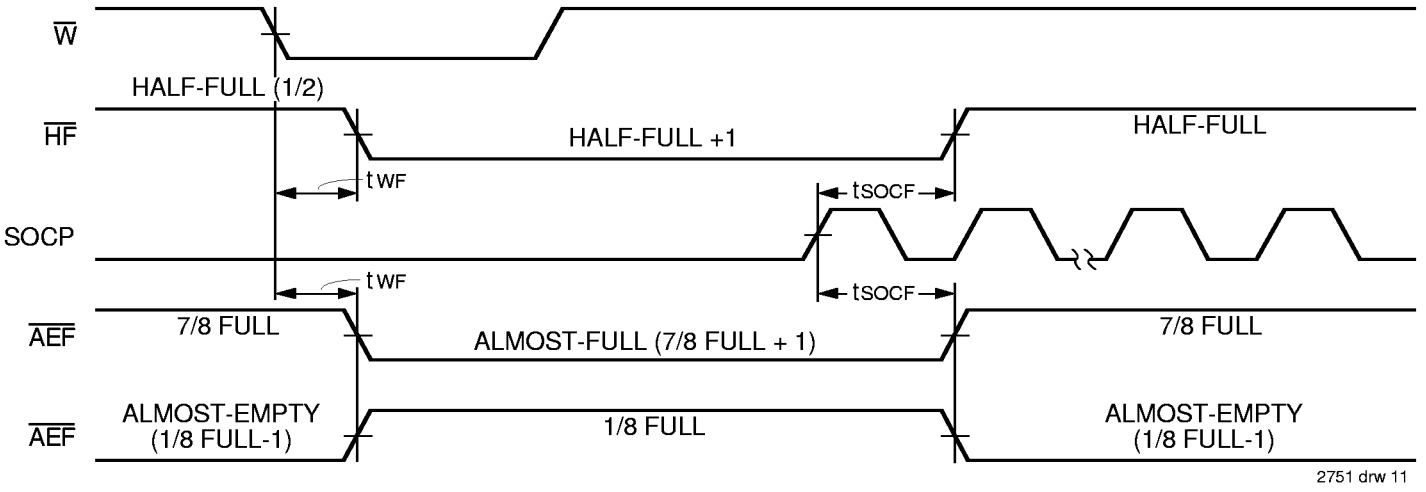
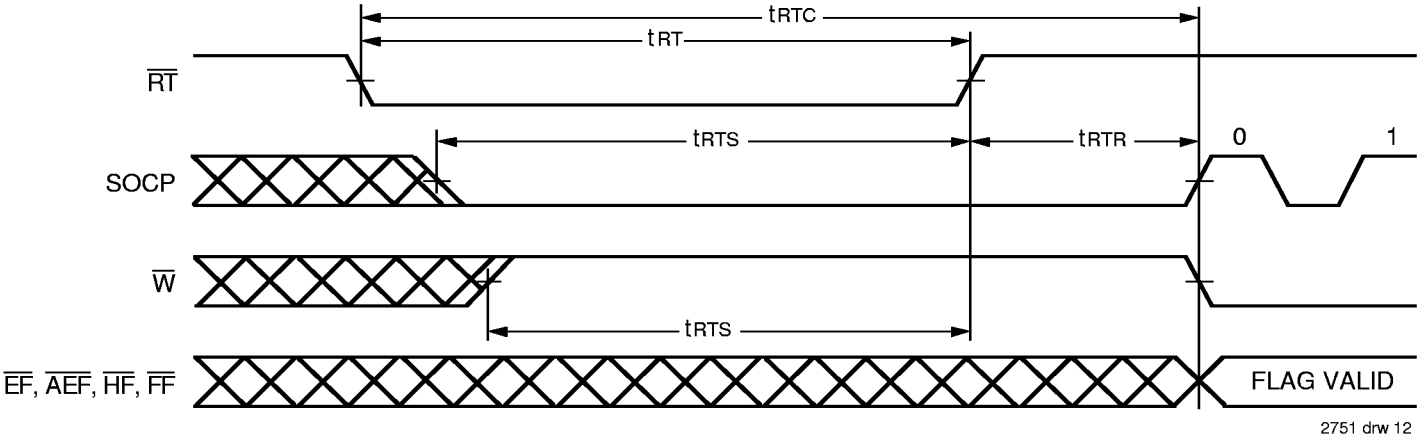


Figure 8. Half Full, Almost Full and Almost Empty Timings



NOTE:
1. $\overline{EF}$, $\overline{AEF}$, $\overline{HF}$ and $\overline{FF}$ may change status during Retransmit, but flags will be valid at t_{RTC}.

Figure 9. Retransmit

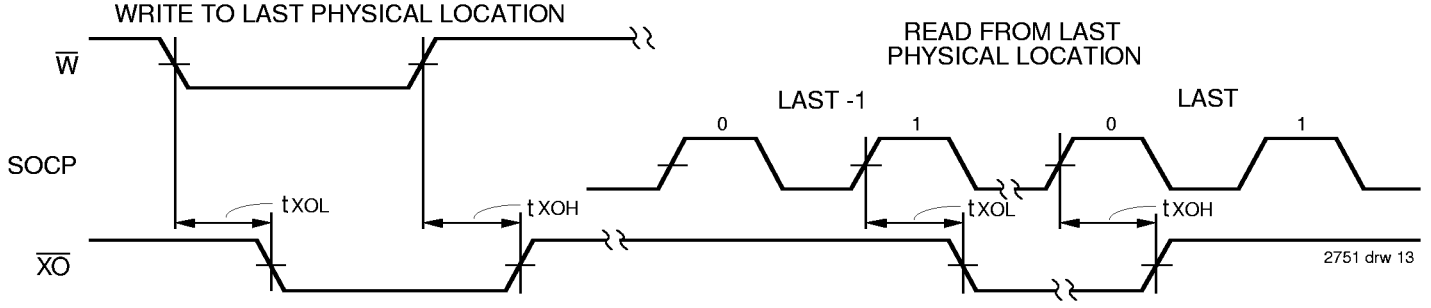


Figure 10. Expansion-Out

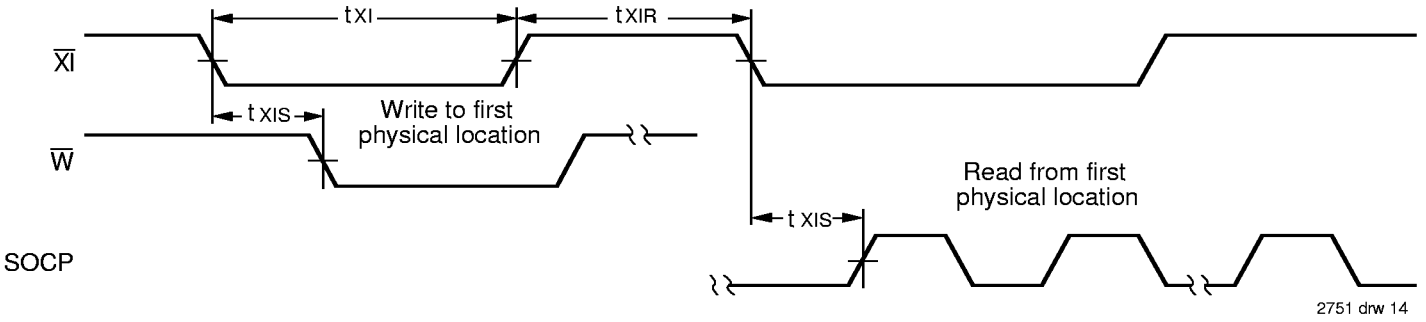


Figure 11. Expansion-In

OPERATING CONFIGURATIONS

Single Device Configuration

In the standalone case, the SOX line is tied HIGH and not used. On the first LOW-to-HIGH of the SOCP clock, all of the Data Set lines (Q4, Q6, Q7, Q8) go LOW and a new serial word is started. The Data Set lines then go HIGH on the equivalent SOCP clock pulse. This continues until the Q line connected to $\overline{NR}$ goes HIGH completing the serial word. The cycle is then repeated with the next LOW-to-HIGH transition of SOCP.

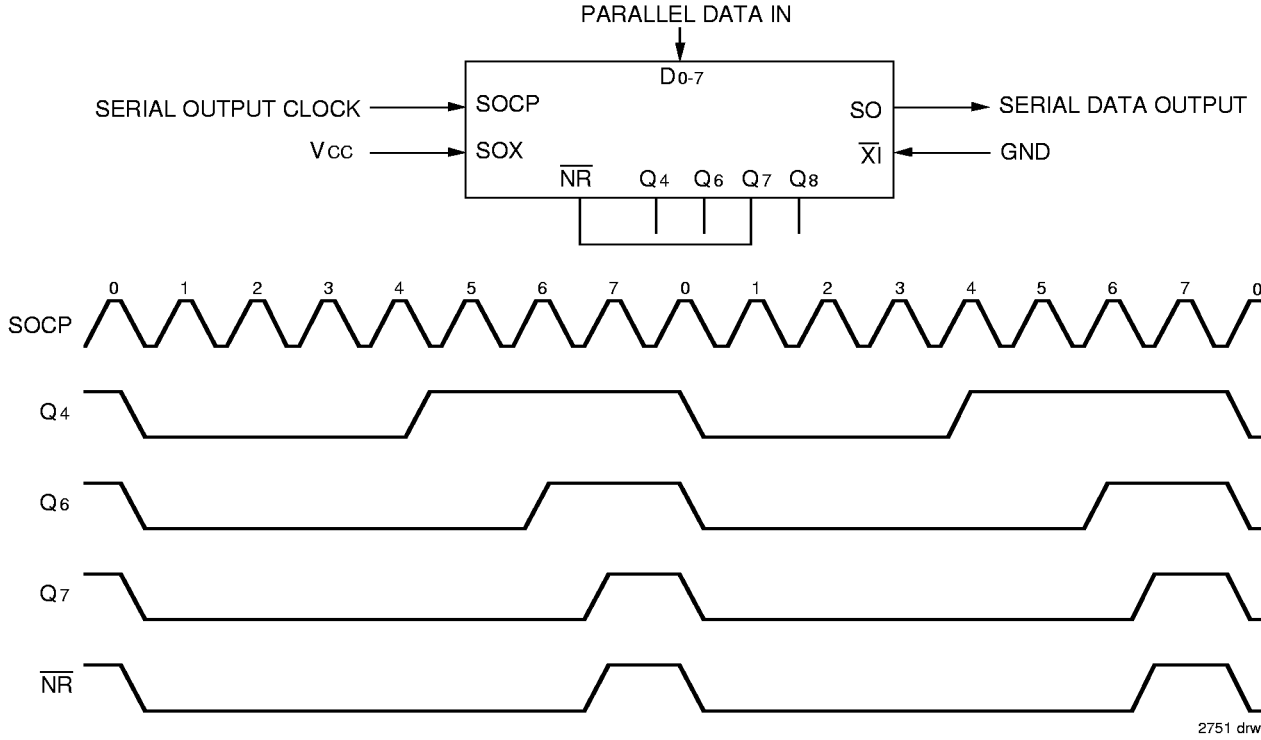


Figure 12. Eight-Bit Word Single Device Configuration

TRUTH TABLES
TABLE 1: RESET AND RETRANSMIT — SINGLE DEVICE CONFIGURATION/WIDTH EXPANSION MODE

Mode	Inputs			Internal Status		Outputs		
	$\overline{RS}$	$\overline{FL}/\overline{RT}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{AEF}$, $\overline{EF}$	$\overline{FF}$	$\overline{HF}$
Reset	0	X	0	Location Zero	Location Zero	0	1	1
Retransmit	1	0	0	Location Zero	Unchanged	X	X	X
Read/Write	1	1	0	Increment(1)	Increment(1)	X	X	X

NOTE:
1. Pointer will increment if appropriate flag is HIGH.

2751 tbl 09

Width Expansion Configuration

In the cascaded case, word widths of more than 9 bits can be achieved by using more than one device. By tying the SOX line of the least significant device HIGH and the SOX of the subsequent devices to the appropriate Data Set lines of the previous devices, a cascaded serial word is achieved.

On the first LOW-to-HIGH clock edge of SOCP, all lines go LOW. Just as in the standalone case, on each corresponding clock cycle, the equivalent Data Set line goes HIGH in order of least to most significant. When the Data Set line which is connected to the SOX input of the next device goes HIGH, the Do of that device goes HIGH, the cascading from one device to the next. The Data Set line of the most significant bit programs the serial word width by being connected to all NR inputs.

The Serial Data Output (SO) of each device in the serial word must be tied together. Since the SO pin is three stated, only the device which is currently shifting out is enabled and driving the 1-bit-bus.

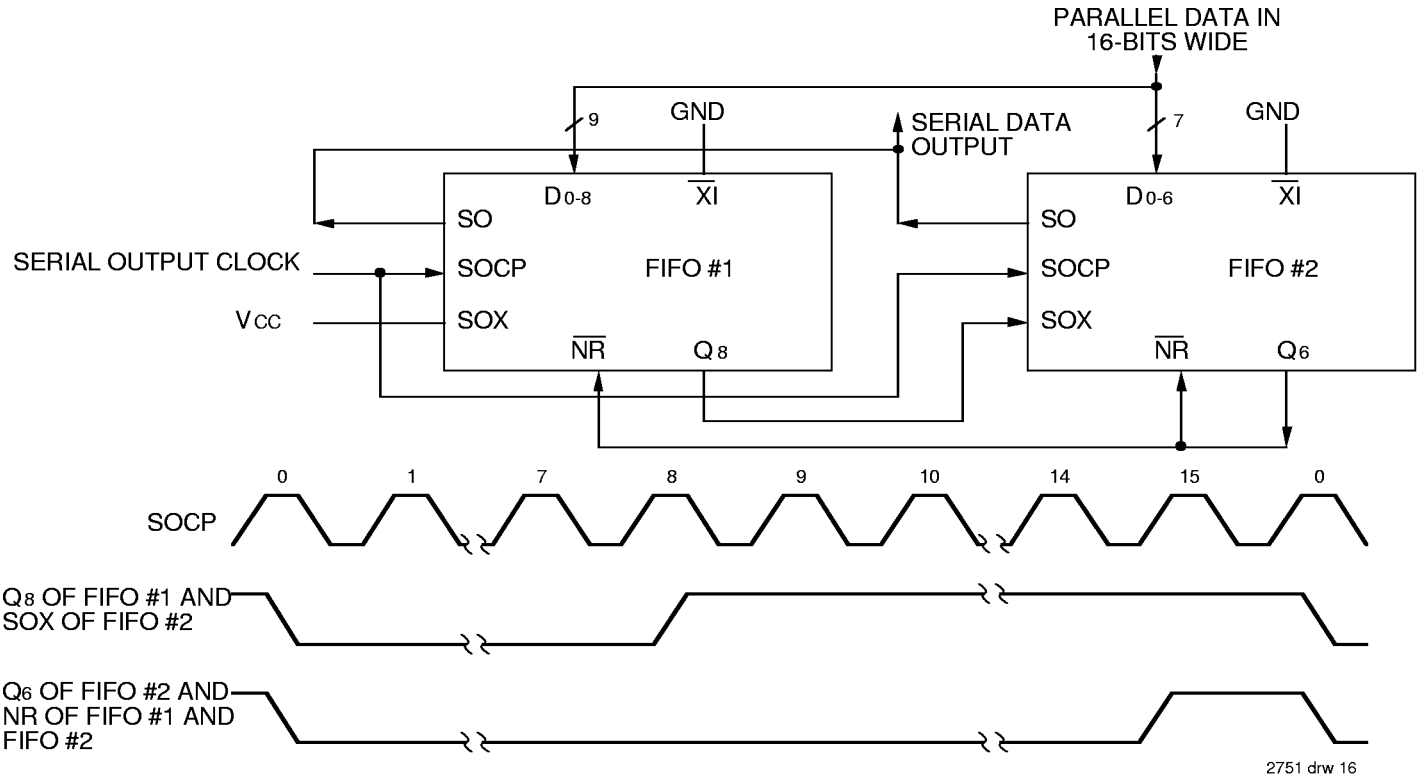


Figure 13. Width Wxpansion for 16-bit Parallel Data In. The Parallel Data In is tied to D_{0-8} of FIFO #1 and D_{0-6} of FIFO #2.

Depth Expansion (Daisy Chain) Mode

The IDT72131/72141 can be easily adapted to applications where the requirements are for greater than 2,048/4,096 words. Figure 14 demonstrates Depth Expansion using three IDT72131/72141. Any depth can be attained by adding additional IDT72131/72141 operates in the Depth Expansion configuration when the following conditions are met:

1. The first device must be designated by grounding the First Load ($\overline{FL}$) control input.
2. All other devices must have $\overline{FL}$ in the HIGH state.
3. The Expansion Out ($\overline{XO}$) pin of each device must be tied to the Expansion In ($\overline{XI}$) pin of the next device.
4. External logic is needed to generate a composite Full Flag ($\overline{FF}$) and Empty Flag ($\overline{EF}$). This requires the OR-ing of all $\overline{EF}$s and OR-ing of all $\overline{FF}$s (i.e., all must be set to generate the correct composite $\overline{FF}$ or $\overline{EF}$).
5. The Retransmit ($\overline{RT}$) function and Half-Full Flag ($\overline{HF}$) are not available in the Depth Expansion mode.

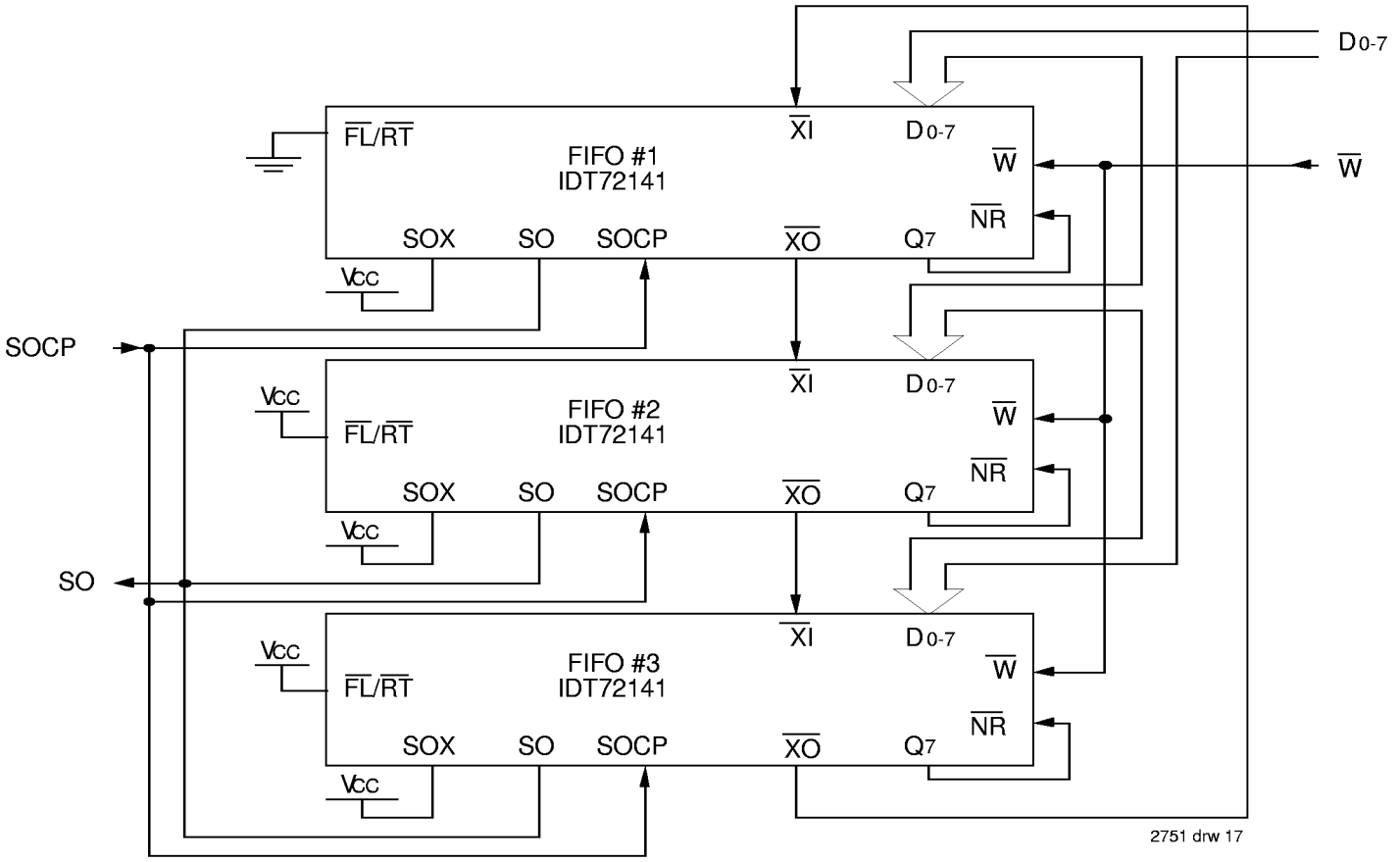


Figure 14. A 12K x 8 Parallel-In Serial-Out FIFO

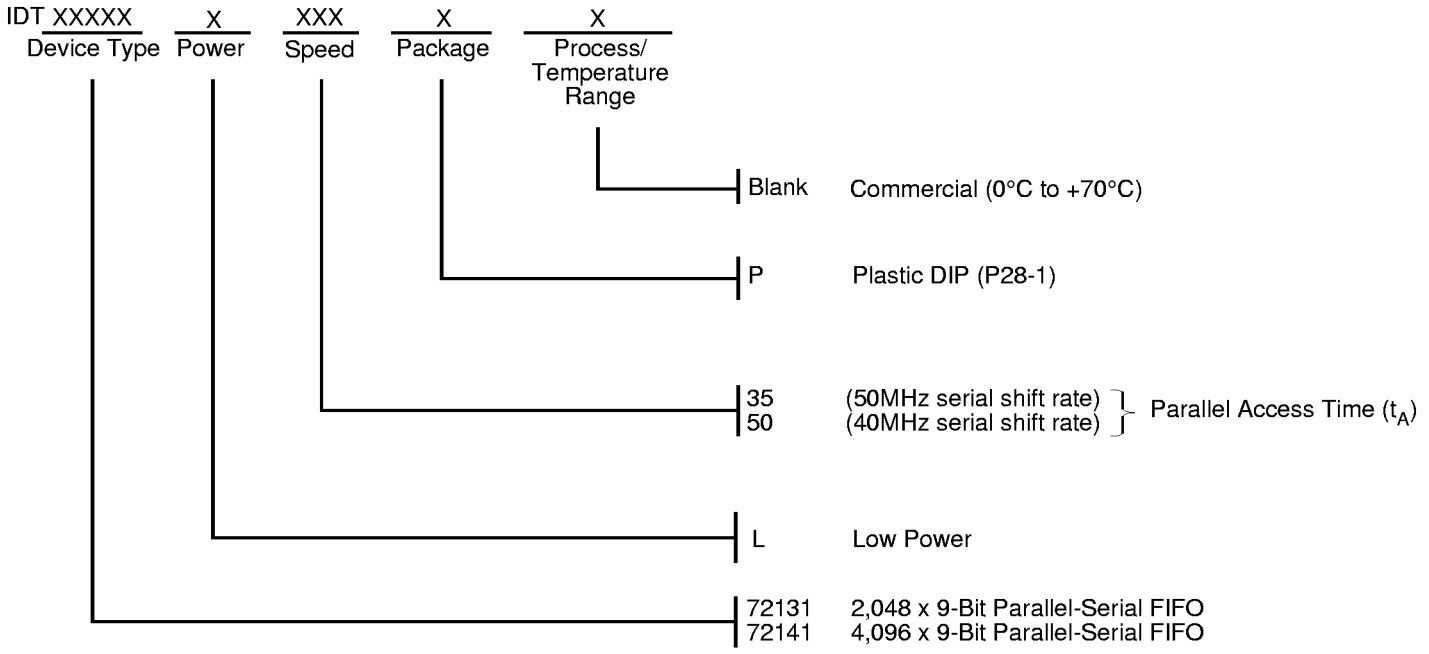
TABLE 2: RESET AND FIRST LOAD TRUTH TABLE — DEPTH EXPANSION/COMPOUND EXPANSION MODE

Mode	Inputs			Internal Status		Outputs	
	$\overline{RS}$	$\overline{FL}$	$\overline{XI}$	Read Pointer	Write Pointer	$\overline{EF}$	$\overline{FF}$
Reset-First Device	0	0	(1)	Location Zero	Location Zero	0	1
Reset-All Other Devices	0	1	(1)	Location Zero	Location Zero	0	1
Read/Write	1	X	(1)	X	X	X	X

2751 tbl 10

NOTES:
1. $\overline{XI}$ is connected to $\overline{XO}$ of previous device.
2. $\overline{RS}$ = Reset Input, $\overline{FL}/\overline{RT}$ = First Load/Retransmit, $\overline{EF}$ = Empty Flag Ouput, $\overline{FF}$ = Full Flag Output, $\overline{XI}$ = Expansion Input.

ORDERING INFORMATION

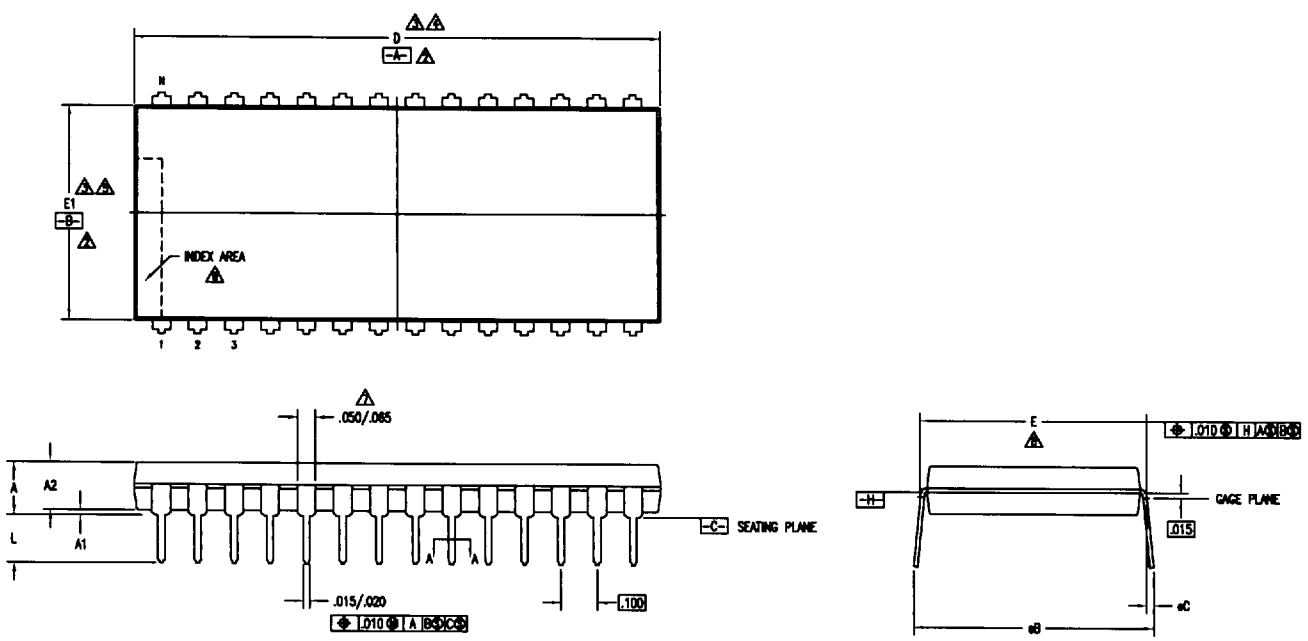


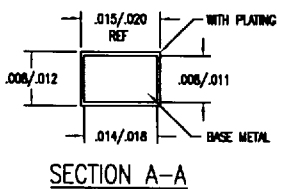
2751 drw 18

NOTE:
1. Industrial temperature range is available by special order.

PLASTIC DIP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27654	05	REDRAW TO JEDEC FORMAT	03/15/95	





SECTION A-A

TOLERANCES UNLESS SPECIFIED	
DECIMAL	ANGULAR
XX±	±
XXX±	
XXXX±	

APPROVALS	DATE
DRAWN dd	10/15/98
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
PHONE: (408) 727-6116
FAX: (408) 492-8674 TWX: 910-338-2070

TITLE: PD PACKAGE OUTLINE .600" BODY WIDTH PDIP .100" PITCH

SIZE	DRAWING No.	REV
C	PSC-4003	05

DO NOT SCALE DRAWING

PLASTIC DIP (Continued)

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
27684	05	REDRAW TO JEDEC FORMAT	03/15/95	

DWG #	P24-2				P28-1				P40-1				P48-1			
SYMBOL	JEDEC VARIATION AA			NOTE	JEDEC VARIATION AB			NOTE	JEDEC VARIATION AC			NOTE	JEDEC VARIATION AD			NOTE
	MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX		MIN	NOM	MAX	
A	.160	-	.185		.160	-	.185		.160	-	.185		.170	-	.200	
A1	.015	-	.035		.015	-	.035		.015	-	.035		.015	-	.035	
A2	.125	.150	.175		.125	.150	.175		.125	.150	.175		.125	.150	.175	
D	1.240	1.250	1.260	3,4	1.420	1.440	1.460	3,4	2.050	2.060	2.070	3,4	2.420	2.435	2.450	3,4
E	.600	.610	.620	8	.600	.610	.620	8	.600	.610	.620	8	.600	.610	.620	8
E1	.530	.540	.550	3,5	.530	.540	.550	3,5	.530	.540	.550	3,5	.530	.545	.560	3,5
eB	.610	-	.670		.610	-	.670		.610	-	.670		.610	-	.670	
eC	.000	-	.040		.000	-	.040		.000	-	.040		.000	-	.040	
L	.120	.135	.150		.120	.135	.150		.120	.135	.150		.120	.135	.150	
N	24				28				40				48			

NOTES:

1. ALL DIMENSIONING AND TOLERANCING CONFORM TO ANSI Y14.5M-1982
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS D AND E1 ARE TO BE DETERMINED AT DATUM PLANE -H-
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .010 PER SIDE
5. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSIONS. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEEED .010 PER SIDE
6. DETAIL OF PIN 1 IDENTIFIER IS OPTIONAL BUT MUST BE LOCATED WITHIN THE ZONE INDICATED
7. LEAD WIDTH DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS .010 MAXIMUM TOTAL PER LEAD
8. DIMENSION E IS MEASURED ON THE OUTSIDE SURFACE OF THE LEADS AT THE GAGE OF .015 BELOW DATUM PLANE -H-
9. ALL DIMENSIONS ARE IN INCHES
10. THIS OUTLINE CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MS-011, VARIATION AA, AB, AC & AD

TOLERANCES UNLESS SPECIFIED		Integrated Device Technology, Inc. 2975 Stender Way, Santa Clara, CA 95054 PHONE: (408) 727-6116 FAX: (408) 492-8674 TWX: 910-338-2070
DECIMAL .XX± .XXX± .XXXX±	ANGULAR ±	
APPROVALS	DATE	TITLE PD PACKAGE OUTLINE .600" BODY WIDTH PDIP .100" PITCH
DRAWN AA	10/15/95	
CHECKED		SIZE C DRAWING No. PSC-4003 REV 05
		DO NOT SCALE DRAWING