PMI

MAT-03

LOW NOISE, MATCHED,
DUAL PNP TRANSISTOR

Precision Monolithics Inc.

T-74-09-01

FEATURES

- **Dual Matched PNP Transistor**
- **Low Offset Voltage** ..... **100μV Max**
- **Low Noise** ..... **1nV/√Hz @ 1kHz Max**
- **High Gain** ..... **100 Min**
- **High Gain Bandwidth** ..... **190MHz Typ**
- **Tight Gain Matching** ..... **3% Max**
- **Excellent Logarithmic Conformance** ..... **$r_{BE} \simeq 0.3\Omega$ Typ**
- **Available in Die Form**

ORDERING INFORMATION†

T_A = +25°C V_{OS} MAX (μV)	PACKAGE		OPERATING TEMPERATURE RANGE
	TO-78	LCC	
100	MAT03AH*	MAT03ARC/883	MIL
100	MAT03EH	—	XIND
200	MAT03FH	—	XIND

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

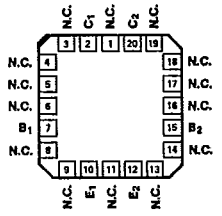
† Burn-in is available on industrial temperature range parts. For ordering information, see PMI's Data Book, Section 2.

GENERAL DESCRIPTION

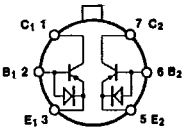
The MAT-03 dual monolithic PNP transistor offers excellent parametric matching and high frequency performance. Low noise characteristics (1nV/√Hz Max @ 1kHz), high bandwidth (190MHz typical), and low offset voltage (100μV Max), makes the MAT-03 an excellent choice for demanding preamplifier applications. Tight current gain matching (3% Max mismatch) and high current gain (100 Min), over a wide range of collector current, makes the MAT-03 an excellent choice for current mirrors. A low value of bulk resistance (typically 0.3Ω) also makes the MAT-03 an ideal component for applications requiring accurate logarithmic conformance.

Each transistor is individually tested to data sheet specifications. Device performance is guaranteed at 25°C and over the extended industrial and military temperature ranges. To insure the long-term stability of the matching parameters, internal protection diodes across the base-emitter junction clamp any reverse base-emitter junction potential. This prevents a base-emitter breakdown condition which can result in degradation of gain and matching performance due to excessive breakdown current.

PIN CONNECTIONS



MAT-03ARC/883
20-CONTACT LCC
(RC-Suffix)



TO-78
(H-Suffix)

ABSOLUTE MAXIMUM RATINGS (Note 1)

Collector-Base Voltage (BV_{CBO}) 36V
Collector-Emitter Voltage (BV_{CEO}) 36V
Collector-Collector Voltage (BV_{CC}) 36V
Emitter-Emitter Voltage (BV_{EE}) 36V
Collector Current (I_C) 20mA
Emitter Current (I_E) 20mA
Total Power Dissipation
Ambient Temperature ≤ 70°C (Note 2) 500mW
Operating Temperature Range
MAT-03A .....–55°C to +125°C
MAT-03E/F .....–40°C to +85°C

Operating Junction Temperature ..... –55°C to +150°C
Storage Temperature ..... –65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
Junction Temperature ..... –65°C to +150°C

NOTES:
1. Absolute maximum ratings apply to both DICE and packaged devices.
2. Rating applies to TO-78 not using a heat sink, and LCC; devices in free air only. For TO-78, derate linearly at 6.3mW/°C above 70°C ambient temperature; for LCC, derate at 7.8mW/°C.

ELECTRICAL CHARACTERISTICS at T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03A MIN	MAT-03A TYP	MAT-03A MAX	MAT-03E MIN	MAT-03E TYP	MAT-03E MAX	MAT-03F MIN	MAT-03F TYP	MAT-03F MAX	UNITS
Current Gain (Note 1)	h_{FE}	V_{CB} = 0V, –36V I_C = 1mA	100	165	—	100	165	—	80	165	—	
		I_C = 100µA	90	150	—	90	150	—	70	150	—	
		I_C = 10µA	80	120	—	80	120	—	60	120	—	
Current Gain Matching (Note 2)	Δh_{FE}	I_C = 100µA, V_{CB} = 0V	—	0.5	3	—	0.5	3	—	0.5	6	%
Offset Voltage (Note 3)	V_{OS}	V_{CB} = 0V, I_C = 100µA	—	40	100	—	40	100	—	40	200	µV
Offset Voltage Change vs Collector Voltage	$\Delta V_{OS}/\Delta V_{CB}$	I_C = 100µA V_{CB_1} = 0V V_{CB_2} = –36V	—	11	150	—	11	150	—	11	200	µV
Offset Voltage Change vs Collector Current	$\Delta V_{OS}/\Delta I_C$	V_{CB} = 0V I_{C_1} = 10µA, I_{C_2} = 1mA	—	12	50	—	12	50	—	12	75	µV
Bulk Resistance	r_{BE}	V_{CB} = 0V, 10µA ≤ I_C ≤ 1mA	—	0.3	0.75	—	0.3	0.75	—	0.3	0.75	Ω
Offset Current	I_{OS}	I_C = 100µA, V_{CB} = 0V	—	6	35	—	6	35	—	6	45	nA
Collector-Base Leakage Current	I_{CB_0}	V_{CB} = –36V = V_{MAX}	—	50	200	—	50	200	—	50	400	pA
Noise Voltage Density (Note 4)	e_N	I_C = 1mA, V_{CB} = 0 fo = 10Hz	—	0.8	2	—	0.8	—	—	0.8	—	nV/√Hz
		fo = 100Hz	—	0.7	1	—	0.7	—	—	0.7	—	
		fo = 1kHz	—	0.7	1	—	0.7	—	—	0.7	—	
		fo = 10kHz	—	0.7	1	—	0.7	—	—	0.7	—	
Collector Saturation Voltage	$V_{CE(SAT)}$	I_C = 1mA, I_B = 100µA	—	0.025	0.1	—	0.025	0.1	—	0.025	0.1	V

NOTES:
1. Current gain is measured at collector-base voltages (V_{CB}) swept from 0 to V_{MAX} at indicated collector current. Typicals are measured at V_{CB} = 0V.
2. Current gain matching (Δh_{FE}) is defined as:
$$\Delta h_{FE} = \frac{100\ (\Delta I_B)\ h_{FE}\ (MIN)}{I_C}.$$
3. Offset voltage is defined as:
$V_{OS} = V_{BE_1} - V_{BE_2}$,
where V_{OS} is the differential voltage for
$$I_{C_1} = I_{C_2}: V_{OS} = V_{BE_1} - V_{BE_2} = \frac{KT}{q} \ln\left(\frac{I_{C_1}}{I_{C_2}}\right).$$
4. Sample tested. Noise tested and specified as equivalent input voltage for each transistor.

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ELECTRICAL CHARACTERISTICS at $-55°C \leq T_A \leq +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03A MIN	MAT-03A TYP	MAT-03A MAX	UNITS
Current Gain	h_{FE}	$V_{CB} = 0V, -36V$ $I_C = 1mA$ $I_C = 100\mu A$ $I_C = 10\mu A$	 70 60 50	 110 100 85	 — — —	
Offset Voltage	V_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	—	40	150	μV
Offset Voltage Drift (Note 1)	TCV_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	—	0.3	0.5	$\mu V/°C$
Offset Current	I_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	—	15	85	nA
Breakdown Voltage	BV_{CEO}		36	54	—	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} \ll V_{BE}$) where $T = 298°K$ for $T_A = 25°C$.

ELECTRICAL CHARACTERISTICS at $-40°C \leq T_A \leq +85°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03E MIN	MAT-03E TYP	MAT-03E MAX	MAT-03F MIN	MAT-03F TYP	MAT-03F MAX	UNITS
Current Gain	h_{FE}	$V_{CB} = 0V, -36V$ $I_C = 1mA$ $I_C = 100\mu A$ $I_C = 10\mu A$	 70 60 50	 120 105 90	 — — —	 60 50 40	 120 105 90	 — — —	
Offset Voltage	V_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	—	30	135	—	30	265	μV
Offset Voltage Drift (Note 1)	TCV_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	—	0.3	0.5	—	0.3	1.0	$\mu V/°C$
Offset Current	I_{OS}	$I_C = 100\mu A, V_{CB} = 0V$	—	10	85	—	10	200	nA
Breakdown Voltage	BV_{CEO}		36	—	—	36	—	—	V

NOTE:
1. Guaranteed by V_{OS} test ($TCV_{OS} = V_{OS}/T$ for $V_{OS} \ll V_{BE}$) where $T = 298°K$ for $T_A = 25°C$.

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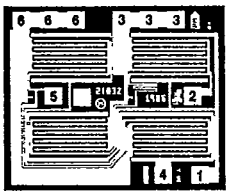
DICE CHARACTERISTICS



DIE SIZE 0.070 × 0.060 inch, 4,200 sq. mils
(1.78 × 1.52 mm, 2.70 sq. mm)

1. COLLECTOR 1
2. BASE 1
3. EMITTER 1
4. COLLECTOR 2
5. BASE 2
6. EMITTER 2

Substrate can be connected to V– or floated.

For additional DICE ordering information, refer to PMI's Data Book, Section 2.

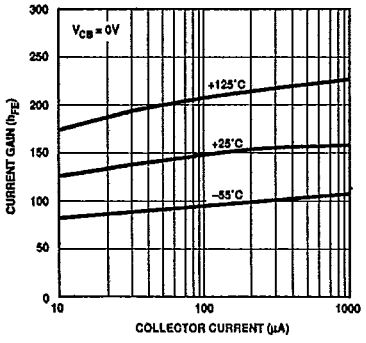
WAFER TEST LIMITS at 25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MAT-03N LIMITS	UNITS
Breakdown Voltage	BV_{CEO}		36	V MIN
Offset Voltage	V_{OS}	$I_C = 100\mu A$, $V_{CB} = 0V$ $10\mu A \le I_C \le 1mA$	200	μV MAX
Current Gain	h_{FE}	$I_C = 1mA$, $V_{CB} = 0V$, −36 V $I_C = 10\mu A$, $V_{CB} = 0V$, −36V	80 60	MIN
Current Gain Match	Δh_{FE}	$I_C = 100\mu A$, $V_{CB} = 0V$	6	% MAX
Offset Voltage Change vs. V_{CB}	$\Delta V_{OS}/\Delta V_{CB}$	$V_{CB_1} = 0V$, $I_C = 100\mu A$ $V_{CB_2} = -36V$	200	μV MAX
Offset Voltage Change vs. Collector Current	$\Delta V_{OS}/\Delta I_C$	$V_{CB} = 0$ $I_{C_1} = 10\mu A$, $I_{C_2} = 1mA$	75	μV MAX
Bulk Resistance	r_{BE}	$10\mu A \le I_C \le 1mA$	0.75	Ω MAX
Collector Saturation Voltage	$V_{CE(SAT)}$	$I_C = 1mA$ $I_B = 100\mu A$	0.1	V MAX

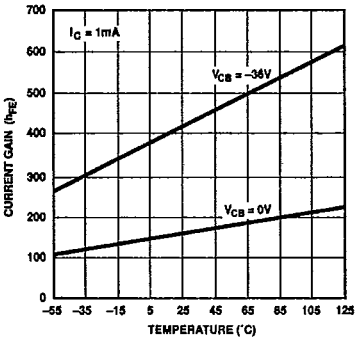
NOTE:
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL PERFORMANCE CHARACTERISTICS

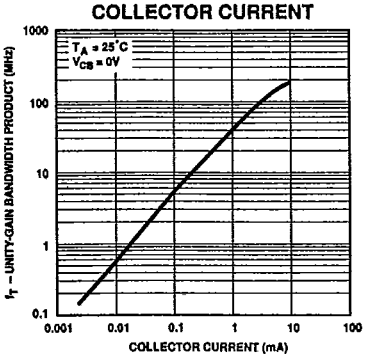
CURRENT GAIN vs COLLECTOR CURRENT



CURRENT GAIN vs TEMPERATURE



GAIN BANDWIDTH vs COLLECTOR CURRENT



9 MATCHED TRANSISTORS

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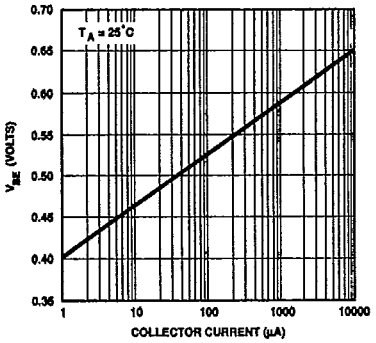
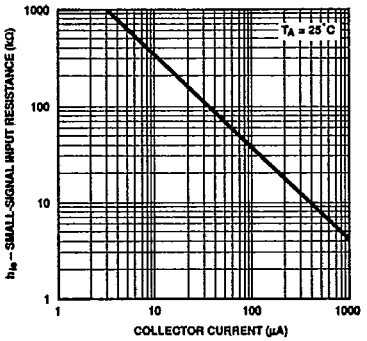
TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

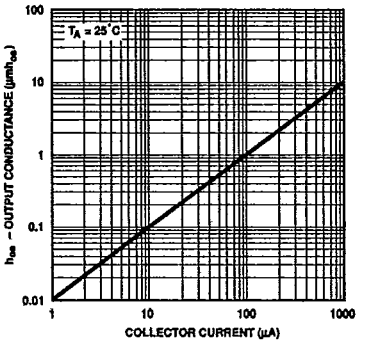
BASE-EMITTER VOLTAGE vs COLLECTOR CURRENT



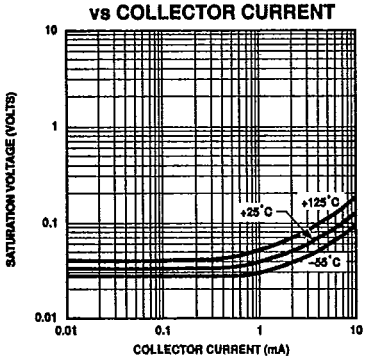
SMALL-SIGNAL INPUT RESISTANCE (h_{ie}) vs COLLECTOR CURRENT



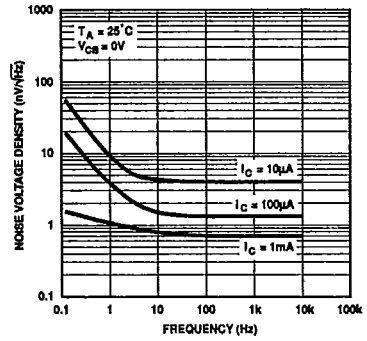
SMALL-SIGNAL OUTPUT CONDUCTANCE (h_{oe}) vs COLLECTOR CURRENT



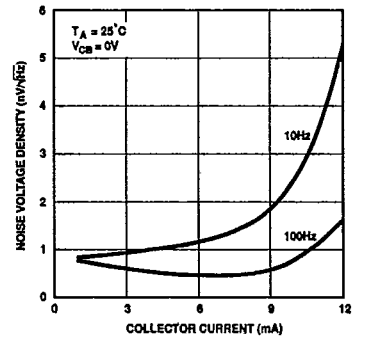
SATURATION VOLTAGE vs COLLECTOR CURRENT



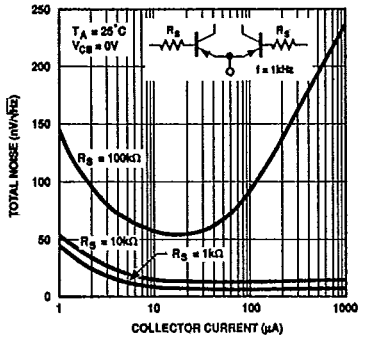
NOISE VOLTAGE DENSITY vs FREQUENCY



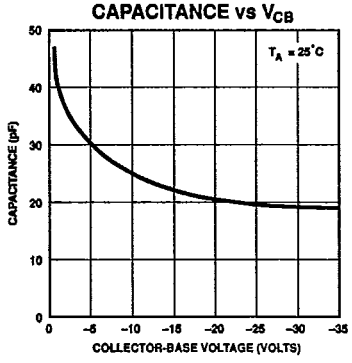
NOISE VOLTAGE DENSITY vs COLLECTOR CURRENT



TOTAL NOISE vs COLLECTOR CURRENT



COLLECTOR-BASE CAPACITANCE vs V_{CB}



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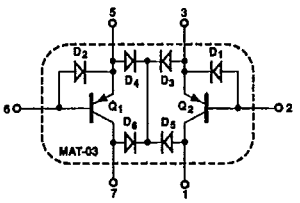

SPICE MODEL PARAMETERS
•SUBCKT MAT03 1 2 3 5 6 7
Q1 1 2 3 PMAT
Q2 7 6 5 PMAT
D1 2 3 DMAT1
D2 6 5 DMAT1
D3 3 4 DMAT1
D4 5 4 DMAT1
D5 1 4 DMAT2
D6 7 4 DMAT2
•MODEL DMAT1 D IS = 7.2E-16 RS = 20
•MODEL DMAT2 D IS = 1E-14 VJ = 0.6 CJ = 68P
•MODEL PMAT PNP BF = 160 IS = 1.4E-13 VAF = 60 BR = 5 VAR = 7 RB = 16
+ PC = 12 RE = 0.35 CJE = 57P VJE = 0.7 MJE = 0.4 IF = 1.08E-9
+ TR = 3E-8 CJC = 40P VJC = 0.55 MJC = 0.5 CJS = 0 IKF = 160M)

SABER* MODEL PARAMETERS
template mat03 n1 n2 n3 n5 n6 n7
electrical n1,n2,n3,n5,n6,n7
{
d..model dmat1 = (is = 7.2e-16,rs = 20)
d..model dmat2 = (is = 1e-14,vj = 0.6,cjo = 68p)
q..model pmat = (type = _p,bf = 160, is = 1.4e-13,vaf = 60,br = 5,var = 7,
rb = 16,rc = 12,re = 0.45,cje = 57p,vje = 0.7,mje = 0.4,tf = 1.08e-9,tr = 3e-8,
cjc = 40p,vjc = 0.55, mjc = 0.5,cjs = 0,ikf = 160m)
q.q1 n1 n2 n3 n4 = model = pmat
q.q2 n7 n6 n5 n4 = model = pmat
d.d1 n2 n3 = model = dmat1
d.d2 n6 n5 = model = dmat1
d.d3 n3 n4 = model = dmat1
d.d4 n5 n4 = model = dmat1
d.d5 n1 n4 = model = dmat2
d.d6 n7 n4 = model = dmat2
}

*SABER is a registered trademark of Analogy Inc.

FIGURE 1: *SPICE or SABER Model*

APPLICATIONS INFORMATION

MAT-03 MODELS

The MAT-03 model (Figure 1) includes parasitic diodes D_3 through D_6. D_1 and D_2 are internal protection diodes which prevent zenering of the base-emitter junctions.

The analysis programs, SPICE and SABER, are primarily used in evaluating the functional performance of systems. The models are provided only as an aid in utilizing these simulation programs.

MAT-03 NOISE MEASUREMENT

All resistive components (Johnson noise, $e_n^2 = 4kTBR$, or $e_n = 0.13\sqrt{R}$ nV/$\sqrt{Hz}$, where R is in kΩ) and semiconductor junctions (Shot noise, caused by current flowing through a junction, produces voltage noise in series impedances such as transistor-collector load resistors, $I_n = 0.566\sqrt{I}$ pA/$\sqrt{Hz}$ where I is in μA) contribute to the system input noise.

Figure 2 illustrates a technique for measuring the equivalent input noise voltage of the MAT-03. 1mA of stage current is used

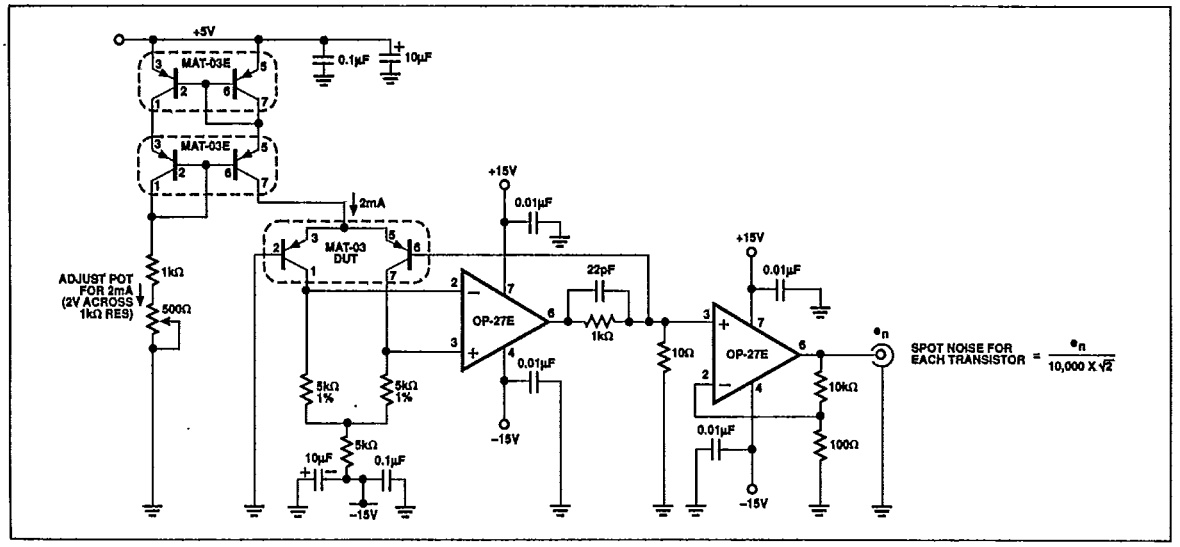

FIGURE 2: *MAT-03 Voltage Noise Measurement Circuit*

to bias each side of the differential pair. The 5kΩ collector resistors noise contribution is insignificant compared to the voltage noise of the MAT-03. Since noise in the signal path is referred back to the input, this voltage noise is attenuated by the gain of the circuit. Consequently, the noise contribution of the collector load resistors is only 0.048nV/$\sqrt{Hz}$. This is considerably less than the typical 0.8nV/$\sqrt{Hz}$ input noise voltage of the MAT-03 transistor.

The noise contribution of the OP-27 gain stages is also negligible due to the gain in the signal path. The op amp stages amplify the input referred noise of the transistors to increase the signal strength to allow the noise spectral density (e_{in} × 10000) to be measured with a spectrum analyzer. And, since we assume equal noise contributions from each transistor in the MAT-03, the output is divided by $\sqrt{2}$ to determine a single transistor's input noise.

Air currents cause small temperature changes that can appear as low frequency noise. To eliminate this noise source, the measurement circuit must be thermally isolated. Effects of extraneous noise sources must also be eliminated by totally shielding the circuit.

SUPER LOW NOISE AMPLIFIER

The circuit in Figure 3a is a super low noise amplifier with equivalent input voltage noise of 0.32nV/$\sqrt{Hz}$. By paralleling three MAT-03 matched pairs, a further reduction of amplifier noise is attained by a reduction of the base spreading resistance by a factor of 3, and consequently the noise by $\sqrt{3}$. Additionally, the shot noise contribution is reduced by maintaining a high collector current (2mA/device) which reduces the dynamic emitter resistance and decreases voltage noise. The voltage noise is inversely proportional to the square root of the stage current, and current noise increases proportionally to the square root of the stage current. Accordingly, this amplifier capitalizes on voltage noise reduction techniques at the expense of increasing the current noise. However, high current noise is not usually important when dealing with low impedance sources.

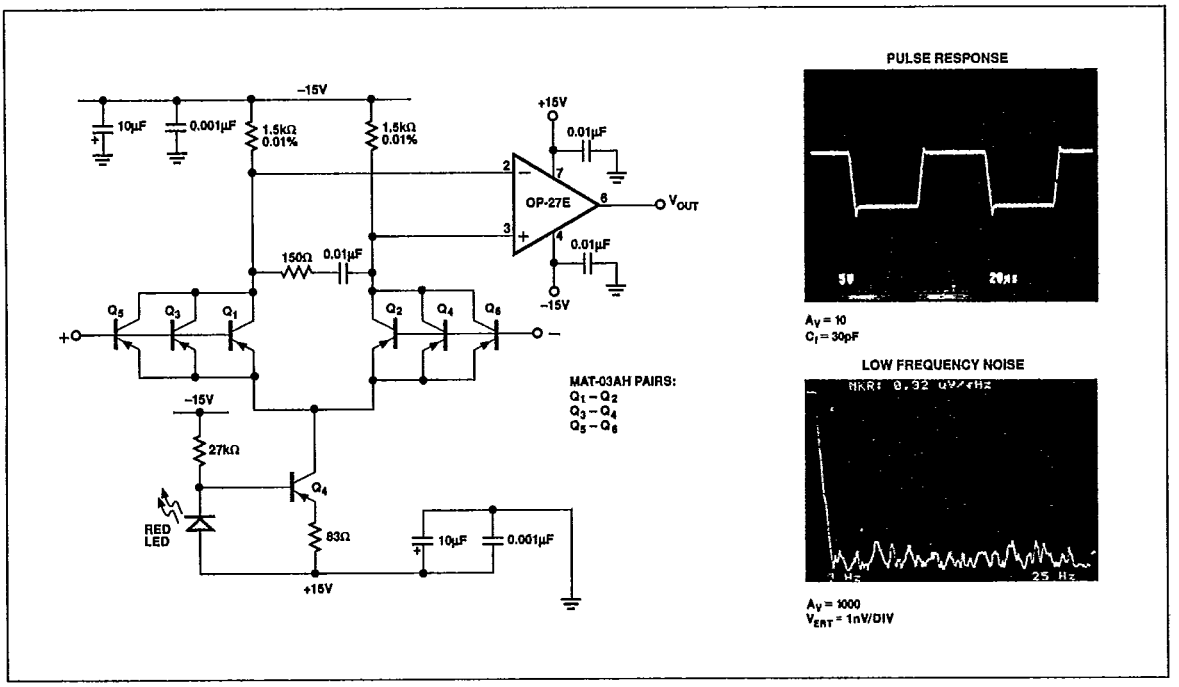

FIGURE 3a: *Super Low Noise Amplifier*

This amplifier exhibits excellent full power AC performance, 0.08% THD into a 600Ω load, making it suitable for exacting audio applications (see Figure 3b).

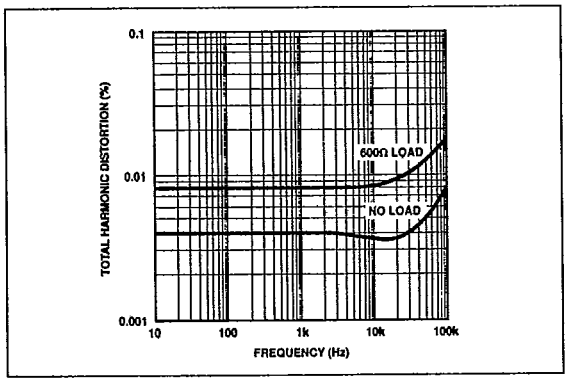

FIGURE 3b: *Super Low Noise Amplifier – Total Harmonic Distortion*

LOW NOISE MICROPHONE PREAMPLIFIER

Figure 4 shows a microphone preamplifier that consists of a MAT-03 and a low noise op amp. The input stage operates at a relatively high quiescent current of 2mA per side, which reduces the MAT-03 transistor's voltage noise. The 1/*f* corner is less than 1Hz. Total harmonic distortion is under 0.005% for a $10V_{p-p}$ signal from 20Hz to 20kHz. The preamp gain is 100, but can be modified by varying R_5 or R_6 ($V_{OUT}/V_{IN} = R_5/R_6 + 1$).

A total input stage emitter current of 4mA is provided by Q_2. The constant current in Q_2 is set by using the forward voltage of a GaAsP LED as a reference. The difference between this voltage and the V_{BE} of a silicon transistor is predictable and constant (to a few percent) over a wide temperature range. The voltage difference, approximately 1V, is dropped across the 250Ω resistor which produces a temperature stabilized emitter current.

CURRENT SOURCES

A fundamental requirement for accurate current mirrors and active load stages is matched transistor components. Due to the excellent V_{BE} matching (the voltage difference between V_{BE}'s required to equalize collector current) and gain matching, the MAT-03 can be used to implement a variety of standard current mirrors that can source current into a load such as an amplifier stage. The advantages of current loads in amplifiers versus resistors is an increase of voltage gain due to higher impedances, larger signal range, and in many applications a wider signal bandwidth.

Figure 5 illustrates a cascode current mirror consisting of two MAT-03 transistor pairs.

The cascode current source has a common base transistor in series with the output which causes an increase in output impedance of the current source since V_{CE} stays relatively constant. High frequency characteristics are improved due to a reduction of Miller capacitance. The small-signal output impedance can be determined by consulting "h_{OF} vs Collector Current" typical graph. Typical output impedance levels approach the performance of a perfect current source.

Considering a typical collector current of 100μA, we have:

$$ro_{Q3} = \frac{1}{1.0\mu MHOS} = 1M\Omega.$$

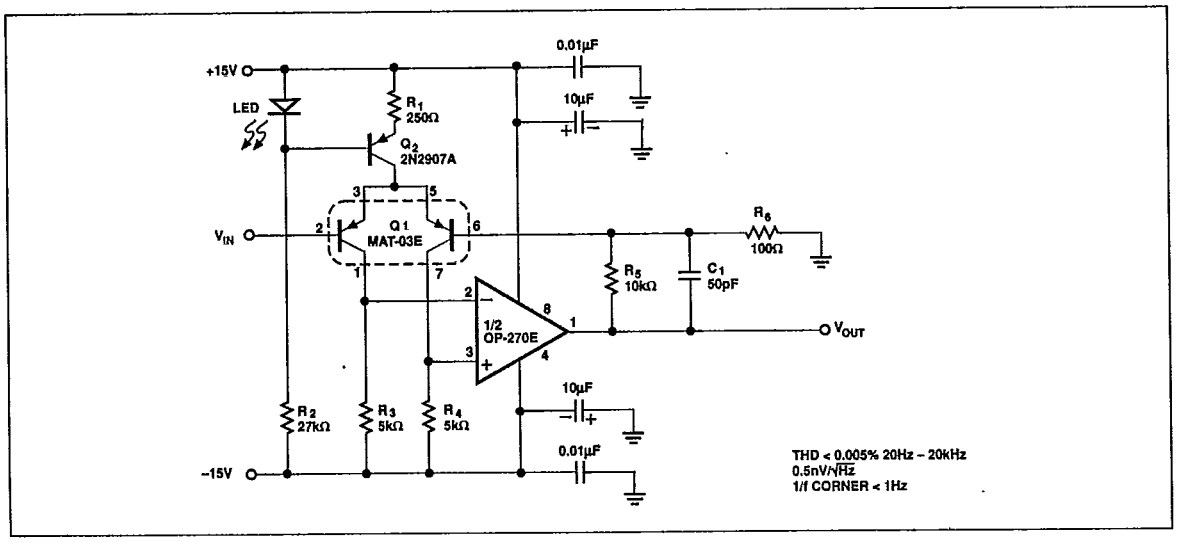

FIGURE 4: *Low Noise Microphone Preamplifier*

Q_2 and Q_3 are in series and operate at the same current level, so the total output impedance is:

$R_O = h_{FE}\, ro_{Q_3} \simeq (160)(1M\Omega) = 160M\Omega$.

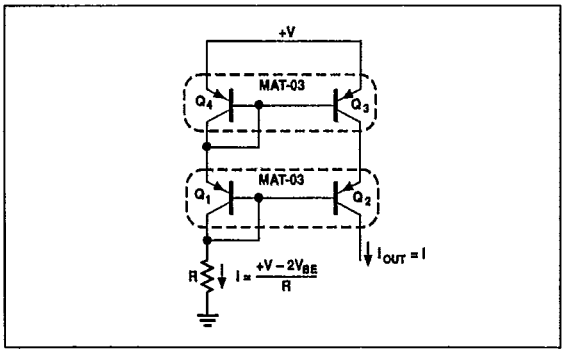

FIGURE 5: *Cascode Current Source*

CURRENT MATCHING

The objective of current source or mirror design is generation of currents that are either matched or must maintain a constant ratio. However, mismatch of base-emitter voltages cause output current errors. Consider the example of Figure 6a. If the resistors and transistors are equal and the collector voltages are the same, the collector currents will match precisely. Investigating the current-matching errors resulting from a non-zero V_{OS}, we define ΔI_C as the current error between the two transistors.

Graph 6b describes the relationship of current matching errors versus offset voltage for a specified average current I_C. Note that since the relative error between the currents is exponentially proportional to the offset voltage, tight matching is required to design high accuracy current sources. For example, if the offset voltage is 5mV at 100μA collector current, the current matching error would be 20%. Additionally, temperature effects such as offset drift (3μV/°C per mV of V_{OS}) will degrade performance if Q_1 and Q_2 are not well matched.

DIGITALLY PROGRAMMABLE BIPOLAR CURRENT PUMP

The circuit of Figure 7 is a digitally programmable current pump. The current pump incorporates a DAC-08, and a fast Wilson current source using the MAT-03. Examining Figure 7, the DAC-08 is set for 2mA full-scale range so that bipolar current operation of ±2mA is achieved. The Wilson current mirror maintains linearity within the LSB range of the 8-bit DAC-08 (±2mA/256 = 15.6μA resolution) as seen in Figure 8. A negative feedback path established by Q_2 regulates the collector current so that it matches the reference current programmed by the DAC-08.

Collector-emitter voltages across both Q_1 and Q_3 are matched by D_1, with Q_3's collector-emitter voltage remaining constant, independent of the voltage across the current source output.

Since Q_2 buffers Q_3, both transistors in the MAT-03, Q_1 and Q_3, maintain the same collector current. D_2 and D_3 form a Baker clamp which prevents Q_2 from turning off, thereby improving the switching speed of the current mirror. The feedback serves to increase the output impedance and improves accuracy by reducing the base-width modulation which occurs with varying collector-emitter voltages. Accuracy and linearity performance of the current pump is summarized in Figure 8.

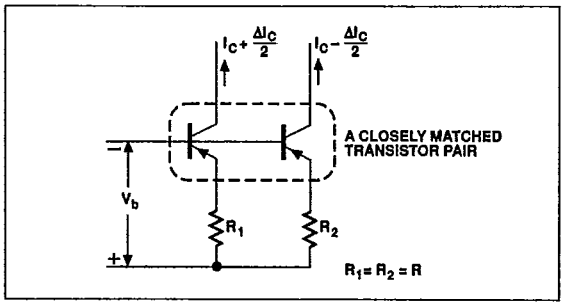

FIGURE 6a: *Current Matching Circuit*

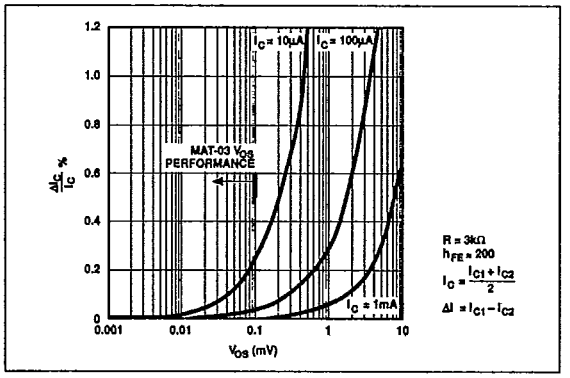

FIGURE 6b: *Current Matching Accuracy % vs Offset Voltage*

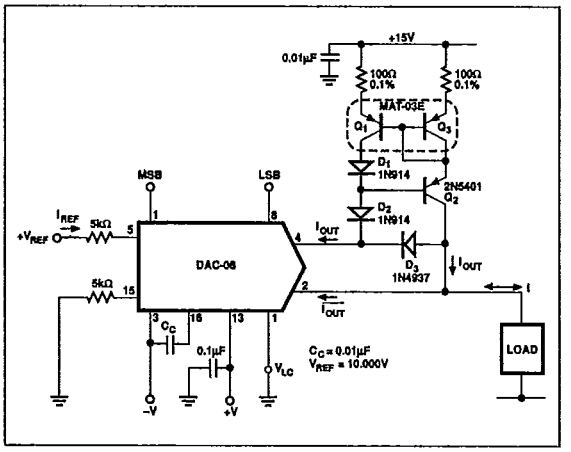

FIGURE 7: *Digitally Programmable Bipolar Current Pump*

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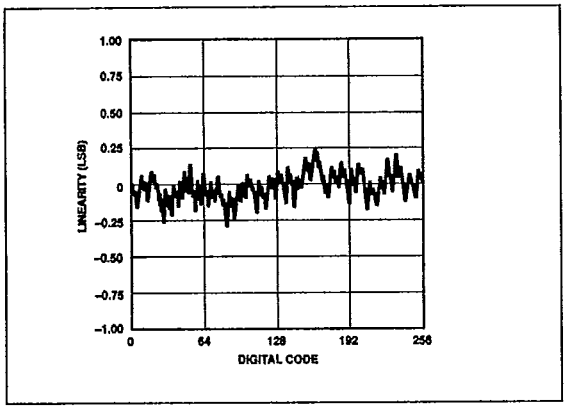

FIGURE 8: *Digitally Programmable Current Pump – INL Error vs Digital Code*

The full scale output of the DAC-08, I_{OUT}, is a linear function of I_{REF}:

$$I_{FR} = \frac{255}{256} \times I_{REF}, \text{ and } I_{OUT} + \overline{I_{OUT}} = I_{REF}\left(\frac{255}{256}\right).$$

The current mirror output is $I_{OUT} - \overline{I_{OUT}} = I$, so that if $I_{REF} = 2mA$:

$$I = 2\, I_{OUT} - 1.992mA$$

$$= 2\left(\frac{\text{Input Code}}{256}\right)(2mA) - 1.992mA.$$

DIGITAL CURRENT PUMP CODING

	DIGITAL INPUT B1 . . . B8	OUTPUT CURRENT
FULL RANGE	1111 1111	I = 1.992mA
HALF-RANGE	1000 0000	I = 0.008mA
ZERO-SCALE	0000 0000	I = -1.992mA