

Am54S/74S174 • Am54S/74S175

Hex / Quadruple D-Type Flip Flops With Clear

Distinctive Characteristics

- 4-Bit and 6-Bit high-speed parallel registers.
- Common clock and common clear.

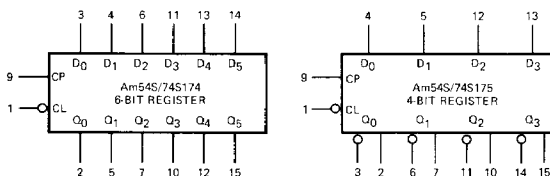
- Positive edge-triggered D flip-flops
- 100% reliability assurance testing in compliance with MIL-STD-883.

FUNCTIONAL DESCRIPTION

The Am54S/74S174 is a six-bit, high-speed register and the Am54S/74S175 is a four-bit, high-speed register built using advanced Schottky technology. The registers consist of D-type flip-flops with a buffered common clock and an asynchronous active LOW buffered clear.

When the clear is LOW, the Q outputs are LOW independent of the other inputs. Information meeting the set-up requirements of the D inputs is transferred to the Q outputs on the positive-going edge of the clock pulse.

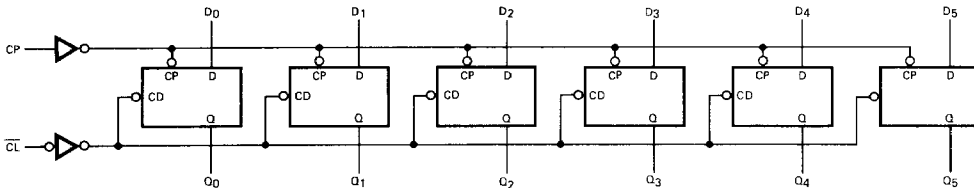
LOGIC SYMBOLS



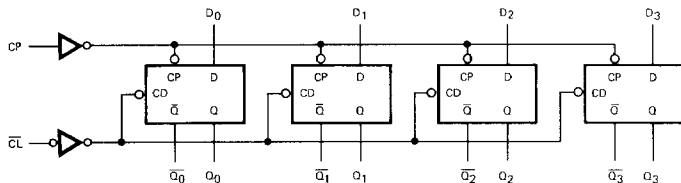
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAMS

Am54S/74S174



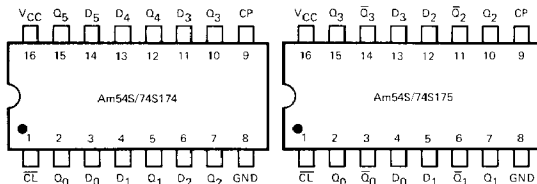
Am54S/74S175



ORDERING INFORMATION

Package Type	Temperature Range	Am54S/74S174 Order Number	Am54S/74S175 Order Number
Molded DIP	0°C to +70°C	SN74S174N	SN74S175N
Hermetic DIP	0°C to +70°C	SN74S174J	SN74S175J
Dice	0°C to +70°C	SN74S174X	SN74S175X
Hermetic DIP	-55°C to +125°C	SN54S174J	SN54S175J
Hermetic Flat Pak	-55°C to +125°C	SN54S174W	SN54S175W
Dice	-55°C to +125°C	SN54S174X	SN54S175X

CONNECTION DIAGRAMS Top Views



Note: Pin 1 is marked for orientation.

MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
Supply Voltage to Ground Potential Continuous	-0.5 V to +7 V
DC Voltage Applied to Outputs for High Output State	-0.5 V to +V _{CC} max.
DC Input Voltage	-0.5 V to +5.5 V
DC Output Current, Into Outputs	30 mA
DC Input Current	-30 mA to +5.0 mA

ELECTRICAL CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (Unless Otherwise Noted)

Am74S174, Am74S175	T _A = 0°C to +70°C	V _{CC} = 5.0 V ±5% (COM'L)	MIN. = 4.75 V	MAX. = 5.25 V
Am54S174, Am54S175	T _A = -55°C to +125°C	V _{CC} = 5.0 V ±10% (MIL)	MIN. = 4.5 V	MAX. = 5.5 V

Parameters	Description	Test Conditions (Note 1)	Min.	Typ. (Note 2)	Max.	Units
V _{OH}	Output HIGH Voltage	V _{CC} = MIN., I _{OH} = -1 mA	74S	2.7	3.4	Volts
		V _{IN} = V _{IH} or V _{IL}	54S	2.5	3.4	
V _{OL}	Output LOW Voltage	V _{CC} = MIN., I _{OL} = 20 mA V _{IN} = V _{IH} or V _{IL}			0.5	Volts
V _{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs	2.0			Volts
V _{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs			0.8	Volts
V _I	Input Clamp Voltage	V _{CC} = MIN., I _{IN} = -18 mA			-1.2	Volts
I _{IL} (Note 3)	Unit Load Input LOW Current	V _{CC} = MAX., V _{IN} = 0.5 V			-2	mA
I _{IH} (Note 3)	Unit Load Input HIGH Current	V _{CC} = MAX., V _{IN} = 2.7 V			50	μA
I _I	Input HIGH Current	V _{CC} = MAX., V _{IN} = 5.5 V			1.0	mA
I _{SC}	Output Short Circuit Current (Note 4)	V _{CC} = MAX., V _{OUT} = 0.0 V		-40	-100	mA
I _{CC}	Power Supply Current (Note 5)	V _{CC} = MAX.	S174	90	144	mA
			S175	60	96	

- Notes: 1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0 V, 25°C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All outputs open and 4.5 V applied to the data and clear inputs. Measured after a momentary ground, then 4.5 V applied to the clock input.

Switching Characteristics (T_A = +25°C)

Parameters	Description	Test Conditions	Min.	Typ.	Max.	Units
t _{PLH}	Clock to Output	V _{CC} = 5.0 V, C _L = 15 pF, R _L = 280 Ω		8	12	ns
t _{PHL}				11.5	17	
t _{PLH}	Clear to Output			10	15	ns
t _{PHL}				13	22	
t _{pw}	Pulse Width		Clock	7		ns
			Clear	10		
t _s	Data Set-up Time			5		ns
t _s	Set-up Time, Clear Recovery (in-active) to Clock			5		ns
t _h	Data Hold Time			3		ns
f _{MAX}	Maximum Clock Frequency		75	110	MHz	

Am54S/74S174 LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
CL	1	1	—	—
Q ₀	2	—	20	10
D ₀	3	1	—	—
D ₁	4	1	—	—
Q ₁	5	—	20	10
D ₂	6	1	—	—
Q ₂	7	—	20	10
GND	8	—	—	—
CP	9	1	—	—
Q ₃	10	—	20	10
D ₃	11	1	—	—
Q ₄	12	—	20	10
D ₄	13	1	—	—
D ₅	14	1	—	—
Q ₅	15	—	20	10
V _{CC}	16	—	—	—

Am54S/74S175 LOADING RULES (In Unit Loads)

Input/Output	Pin No.'s	Input Unit Load	Fan-out	
			Output HIGH	Output LOW
CL	1	1	—	—
Q ₀	2	—	20	10
Q̄ ₀	3	—	20	10
D ₀	4	1	—	—
D ₁	5	1	—	—
Q̄ ₁	6	—	20	10
Q ₁	7	—	20	10
GND	8	—	—	—
CP	9	1	—	—
Q ₂	10	—	20	10
Q̄ ₂	11	—	20	10
D ₂	12	1	—	—
D ₃	13	1	—	—
Q̄ ₃	14	—	20	10
Q ₃	15	—	20	10
V _{CC}	16	—	—	—

FUNCTION TABLE

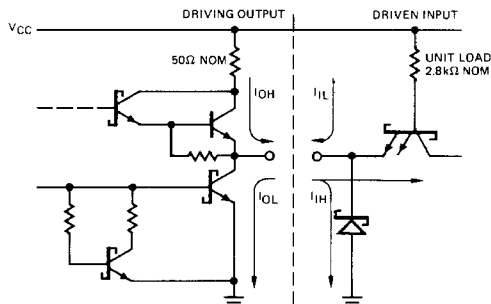
INPUTS			OUTPUTS	
Clear	Clock	D _i	Q _i	Q̄ _i
L	X	X	L	H
H	L	X	NC	NC
H	H	X	NC	NC
H	↑	L	L	H
H	↑	H	H	L

H = HIGH X = Don't Care
 L = LOW NC = No Change
 ↑ = LOW-to-HIGH Transition
 Note: Q̄_i on Am54S/74S175 only

DEFINITION OF FUNCTIONAL TERMS

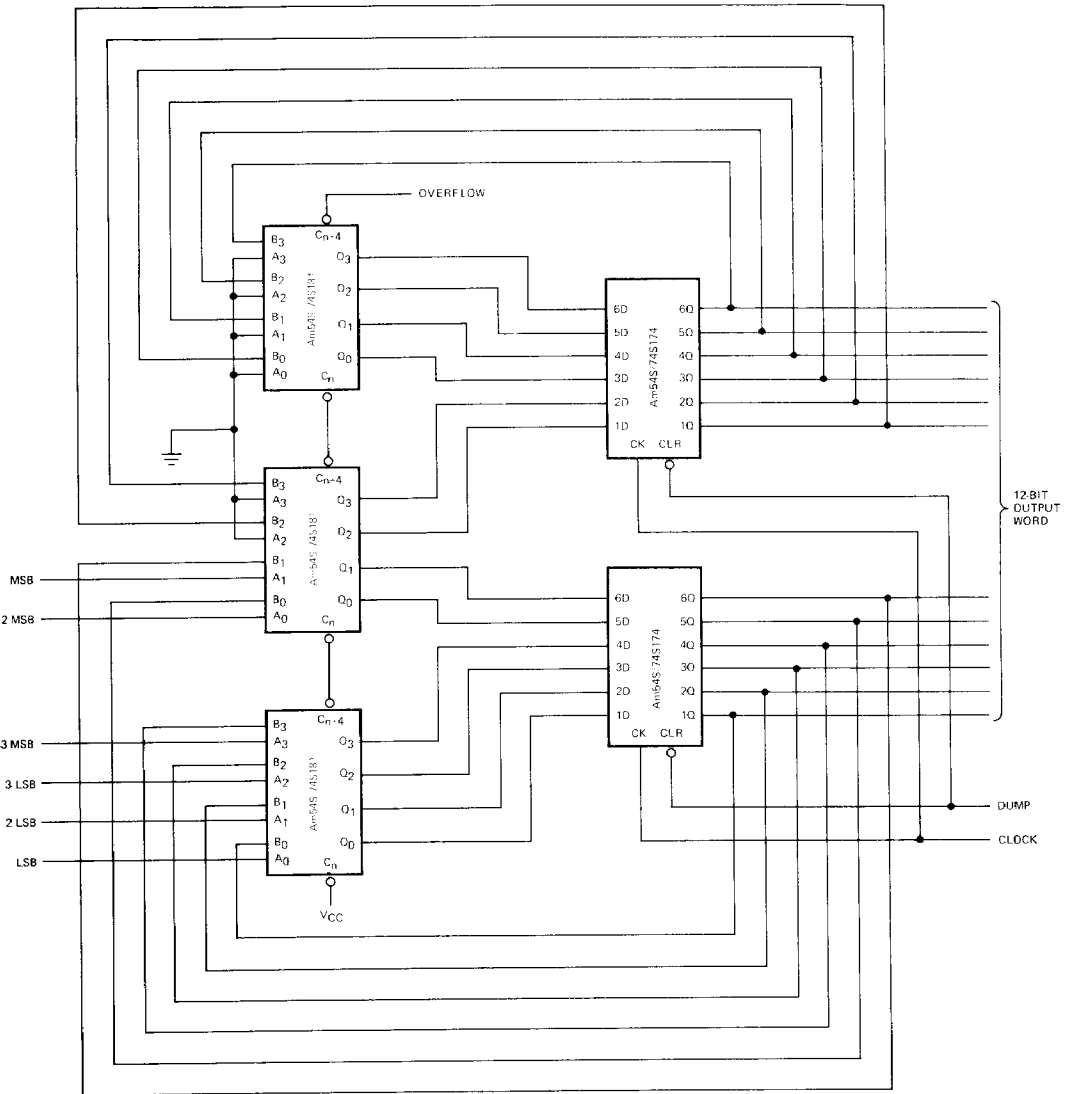
- D_i The D flip-flop data inputs.
- CL Clear. When the clear is LOW, the Q_i outputs are LOW, regardless of the other inputs. When the clear is HIGH, data can be entered in the register.
- CP Clock pulse for the register. Enters data on the positive transition.
- Q_i The TRUE register outputs.
- Q̄_i The complement register outputs.

SCHOTTKY INPUT/OUTPUT CURRENT INTERFACE CONDITIONS



Note: Actual current flow direction shown.

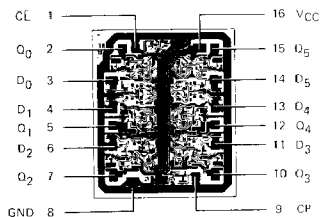
APPLICATION



(Am54S/74S181 in ADD mode)

6-Bit Input, Integrate and Dump for Magnitude-Only Arithmetic (65 samples min. before overflow)

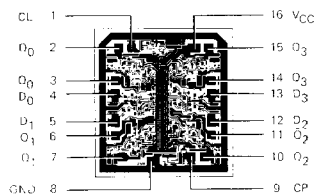
Am54S/74S174



DIE SIZE: 0.070" X 0.083"

Metallization and Pad Layouts

Am54S/74S175



DIE SIZE: 0.067" X 0.073"