National Semiconductor

PRELIMINARY
January 1995

LMX2330/LMX2331/LMX2332 PLLatinum™ Dual Frequency Synthesizer for RF Personal Communications

LMX2330 2.5 GHz/510 MHz
LMX2331 2.0 GHz/510 MHz
LMX2332 1.2 GHz/510 MHz

General Description

The LMX233x family of monolithic, integrated dual frequency synthesizers, including prescalers, is to be used as a local oscillator for RF and first IF of a dual conversion transceiver. It is fabricated using National's ABiC IV silicon BiCMOS process.

The LMX233x contains dual modulus prescalers. A 64/65 or a 128/129 (32/33 or 64/65 in the 2.5 GHz LMX2330) can be selected for the RF synthesizer and a 8/9 or a 16/17 can be selected for the IF synthesizer. Using a digital phase locked loop technique, the LMX233x can generate a very stable, low noise signal for the RF and IF local oscillator. Serial data is transferred into the LMX233x via a three wire interface (Data, Enable, Clock). Supply voltage can range from 2.7V to 5.5V. The LMX233x family features very low current consumption;
LMX2330—15 mA at 3V, LMX2331—14 mA at 3V, LMX2332—8 mA at 3V.

The LMX233x are available in a TSSOP 20-pin surface mount plastic package.

Features

- 2.7V to 5.5V operation
- Low current consumption
- Selectable powerdown mode:
  I_{CC} = 1 μA typical at 3V
- Dual modulus prescaler:

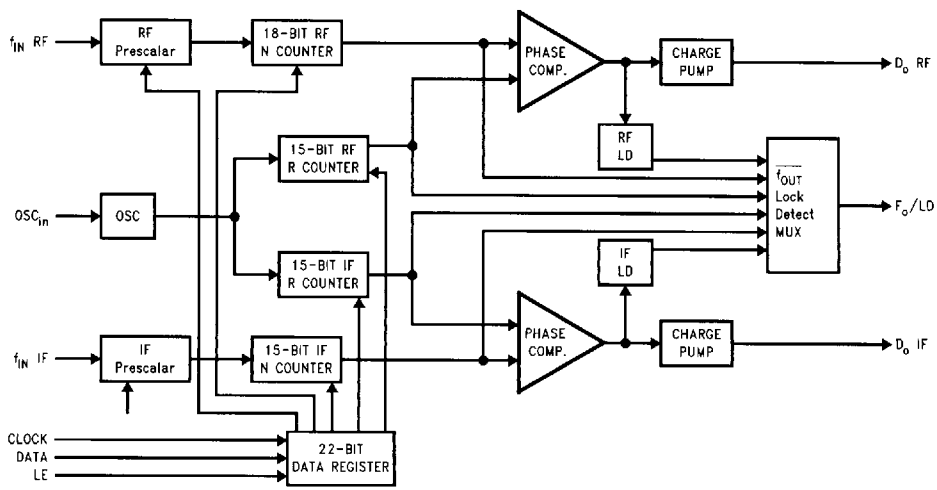
LMX2330	(RF) 32/33 or 64/65
LMX2331/32	(RF) 64/65 or 128/129
LMX2330/31/32	(IF) 8/9 or 16/17

- Selectable charge pump TRI-STATE® mode

Applications

- Portable Wireless Communications (PCS/PCN, cordless)
- Cordless and cellular telephone systems
- Wireless Local Area Networks (WLANs)
- Cable TV tuners (CATV)
- Other wireless communication systems

Functional Block Diagram



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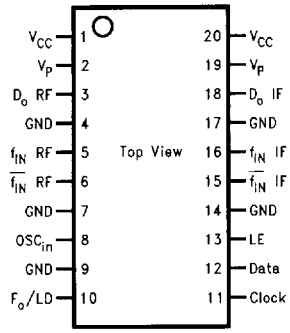
This data sheet contains the design specifications for product development.
Specifications may change in any manner without notice.

Connection Diagram

Thin Shrink Small Outline Package (TM)



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Order Number LMX2330TM, LMX2331TM or LMX2332TM
NS Package Number MTA20

Pin Description

Pin No.	Pin Name	I/O	Description
1	V_{CC}	—	Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	V_P	—	Power Supply for RF charge pump.
3	D_o RF	O	Internal charge pump output. For connection to a loop filter for driving the input of an external VCO.
4	GND	—	Ground.
5	f_{IN} RF	I	RF prescaler input. Small signal input from the VCO.
6	$\overline{f_{IN}}$ RF	I	RF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
7	GND	—	Ground.
8	OSC_{in}	I	Oscillator input. The input has a $V_{CC}/2$ input threshold and can be driven from an external CMOS logic gate.
9	GND	—	Ground.
10	F_o/LD	O	Multiplexed output of the RF/IF programmable or reference dividers and RF/IF lock detect. CMOS output *(see Programmable Modes)*.
11	Clock	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 22-bit shift register.
12	Data	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
13	LE	I	Load enable CMOS input. When LE goes HIGH, data stored in the shift registers is loaded into one of the 4 appropriate latches (control bit dependent).
14	GND	—	Ground.
15	$\overline{f_{IN}}$ IF	I	IF prescaler complimentary input. A bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane. Capacitor is optional with some loss of sensitivity.
16	f_{IN} RF	I	IF prescaler input. Small signal input from the VCO.
17	GND	—	Ground.
18	D_o IF	O	IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
19	V_P	—	Power Supply for IF charge pump.
20	V_{CC}	—	Power supply voltage input. Input may range from 2.7V to 5.5V. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	−0.3V to +6.5V
V_P	−0.3V to +6.5V
Voltage on Any Pin with GND = 0V (V_I)	−0.3V to +6.5V
Storage Temperature Range (T_S)	−65°C to +150°C
Lead Temperature (solder 4 sec.) (T_L)	+260°C

Recommended Operating Conditions

Power Supply Voltage	
V_{CC}	2.7V to 5.5V
V_P	V_{CC} to +5.5V
Operating Temperature (T_A)	−40°C to +85°C

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For guaranteed specifications and test conditions, see the Electrical Characteristics. The guaranteed specifications apply only for the test conditions listed.

Electrical Characteristics V_{CC} = 3.0V, V_P = 3.0V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
I_{CC}	Power Supply Current	LMX2330 RF + IF	V_{CC} = 2.7V to 5.5V		15		mA
		LMX2330 RF Only			12		
		LMX2331 RF + IF			14		
		LMX2331 RF Only			11		
		LMX2332 IF + RF			8		
		LMX2332 RF Only			5		
		LMX233X IF Only			3		
$I_{CC-PWDN}$	Powerdown Current		V_{CC} = 3.0V		1		μA
f_{IN} RF	Operating Frequency	LMX2330		500		2.5	GHz
		LMX2331		200		2.0	
		LMX2332		100		1.2	
f_{IN} IF	Operating Frequency	LMX233X		45		510	MHz
f_{OSC}	Maximum Oscillator Frequency			40			MHz
f_ϕ	Maximum Phase Detector Frequency			10			MHz
Pf_{IN} RF	RF Input Sensitivity		V_{CC} = 3.0V	−15		+4	dBm
			V_{CC} = 5.0V	−10		+4	dBm
Pf_{IN} IF	IF Input Sensitivity		V_{CC} = 2.7V to 5.5V	−10		+4	dBm
V_{OSC}	Oscillator Sensitivity		OSC_{in}	0.5			V_{PP}
V_{IH}	High-Level Input Voltage		*	0.8 V_{CC}			V
V_{IL}	Low-Level Input Voltage		*			0.2 V_{CC}	V
I_{IH}	High-Level Input Current		V_{IH} = V_{CC} = 5.5V*	−1.0		1.0	μA
I_{IL}	Low-Level Input Current		V_{IL} = 0V, V_{CC} = 5.5V*	−1.0		1.0	μA
I_{IH}	Oscillator Input Current		V_{IH} = V_{CC} = 5.5V			100	μA
I_{IL}	Oscillator Input Current		V_{IL} = 0V, V_{CC} = 5.5V	−100			μA
V_{OH}	High-Level Output Voltage		I_{OH} = −500 μA	V_{CC} − 0.4			V
V_{OL}	Low-Level Output Voltage		I_{OL} = 500 μA			0.4	V
t_{CS}	Data to Clock Set Up Time		See Data Input Timing	50			ns
t_{CH}	Data to Clock Hold Time		See Data Input Timing	10			ns
t_{CWH}	Clock Pulse Width High		See Data Input Timing	50			ns
t_{CWL}	Clock Pulse Width Low		See Data Input Timing	50			ns
t_{ES}	Clock to Load Enable Set Up Time		See Data Input Timing	50			ns
t_{EW}	Load Enable Pulse Width		See Data Input Timing	50			ns

*Except f_{IN} RF, f_{IN} IF and OSC_{in}.

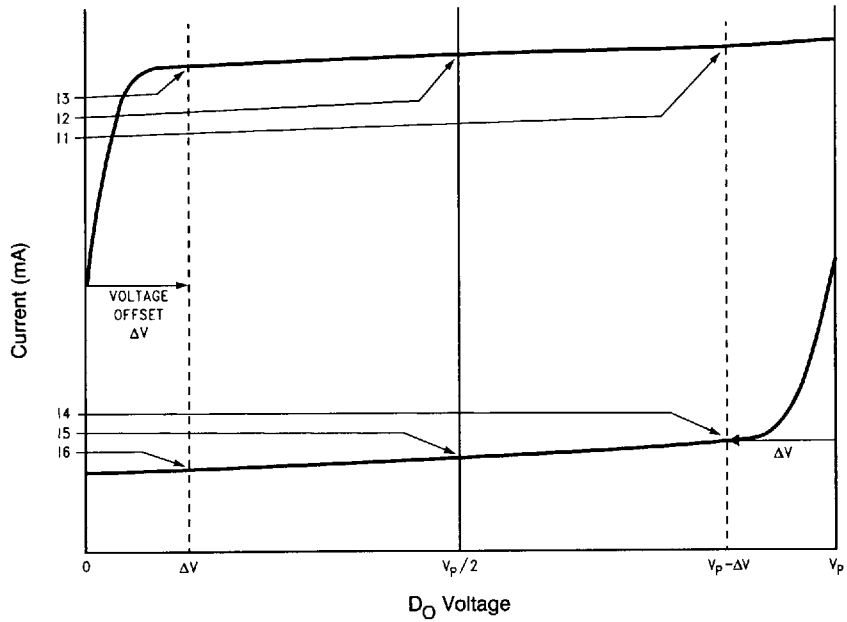
Charge Pump Characteristics V_{CC} = 3.0V, V_P = 3.0V; −40°C < T_A < 85°C, except as specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
I_{D_O}-SOURCE	Charge Pump Output Current	$V_{D_O} = V_P/2$, I_{CP_O} = HIGH**		−2.0		mA
I_{D_O}-SINK		$V_{D_O} = V_P/2$, I_{CP_O} = HIGH**		2.0		mA
I_{D_O}-SOURCE		$V_{D_O} = V_P/2$, I_{CP_O} = LOW**		−0.5		mA
I_{D_O}-SINK		$V_{D_O} = V_P/2$, I_{CP_O} = LOW**		0.5		mA
I_{D_O}-TRI	Charge Pump TRI-STATE Current	$0.5V \le V_{D_O} \le V_P - 0.5V$ −40°C < T < 85°C	−2.5		2.5	nA
I_{D_O}-SINK vs I_{D_O}-SOURCE	CP Sink vs Source Mismatch (Note 1)	$V_{D_O} = V_P/2$ T_A = 25°C		5		%
I_{D_O} vs V_{D_O}	CP Current vs Voltage (Note 2)	$0.5 \le V_{D_O} \le V_P - 0.5V$ T = 25°C		10		%
I_{D_O}vs T	CP Current vs Temperature (Note 3)	$V_{D_O} = V_P/2$ −40°C < T < 85°C		10		%

** See PROGRAMMABLE MODES for I_{CP_O} description.

Notes 1, 2, 3: See charge pump current specification definitions below.

Charge Pump Current Specification Definitions



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I1 = CP sink current at $V_{D_O} = V_P - \Delta V$

I2 = CP sink current at $V_{D_O} = V_P/2$

I3 = CP sink current at $V_{D_O} = \Delta V$

I4 = CP source current at $V_{D_O} = V_P - \Delta V$

I5 = CP source current at $V_{D_O} = V_P/2$

I6 = CP source current at $V_{D_O} = \Delta V$

ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to V_{CC} and ground. Typical values are between 0.5V and 1.0V.

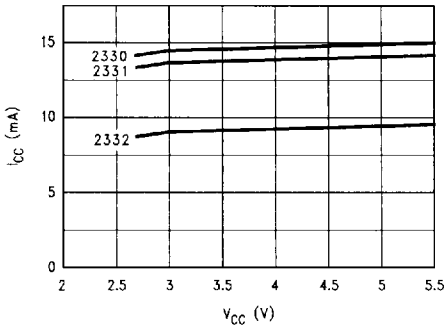
1. I_{D_O} vs V_{D_O} = Charge Pump Output Current magnitude variation vs Voltage =
$[\frac{1}{2} * |I1| - |I3|]/[\frac{1}{2} * (|I1| + |I3|)] * 100\%$ and $[\frac{1}{2} * |I4| - |I6|]/[\frac{1}{2} * (|I4| + |I6|)] * 100\%$

2. $I_{D_{O\text{-sink}}}$ vs $I_{D_{O\text{-source}}}$ = Charge Pump Output Current Sink vs Source Mismatch =
$\{|I2| - |I5|\}/[\frac{1}{2} * (|I2| + |I5|)] * 100\%$

3. I_{D_O} vs T_A = Charge Pump Output Current magnitude variation vs Temperature =
$[|I2 @ temp| - |I2 @ 25°C|]/|I2 @ 25°C| * 100\%$ and $[|I5 @ temp| - |I5 @ 25°C|]/|I5 @ 25°C| * 100\%$

Typical Performance Characteristics

I_{CC} vs V_{CC}



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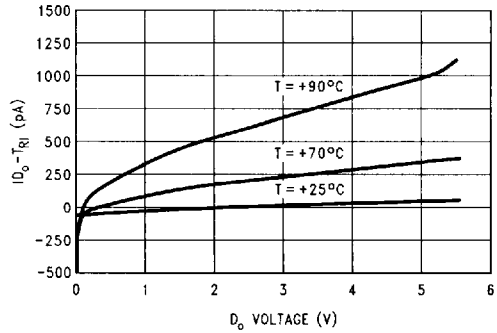
I_{D_O} TRI-STATE vs D_o Voltage



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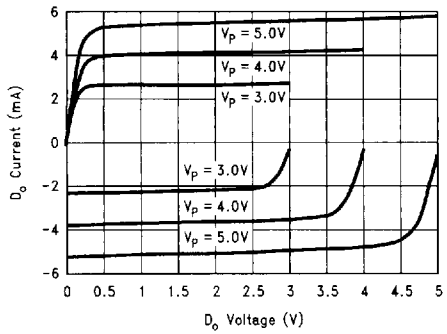
Charge Pump Current vs D_o Voltage
I_{CP} = HIGH



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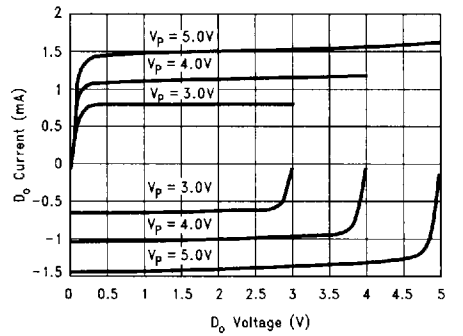
Charge Pump Current vs D_o Voltage
I_{CP} = LOW



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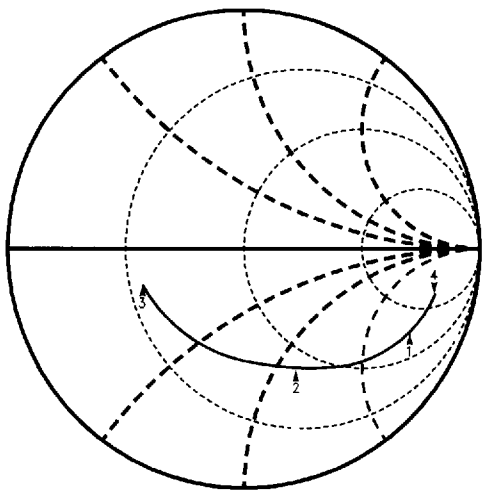
RF Input Impedance
V_{CC} = 2.7V to 5.5V, f_{IN} = 0.5 GHz to 3 GHz



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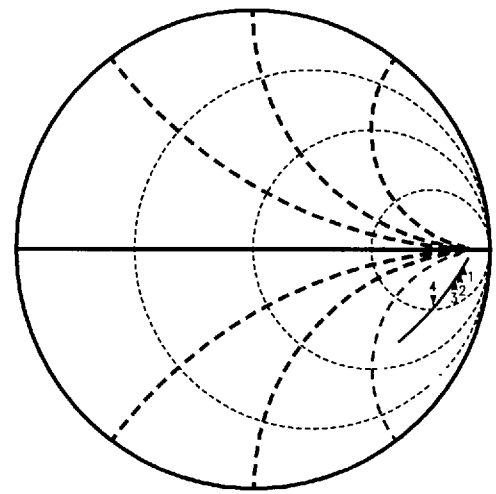
Marker 1 = 1 GHz, Real = 90, Imag. = −158
Marker 2 = 2 GHz, Real = −43, Imag. = −53
Marker 3 = 3 GHz, Real = 18, Imag. = −5
Marker 4 = 500 MHz, Real = 203, Imag. = −284

IF Input Impedance
V_{CC} = 2.7V to 5.5V, f_{IN} = 10 MHz to 1000 MHz



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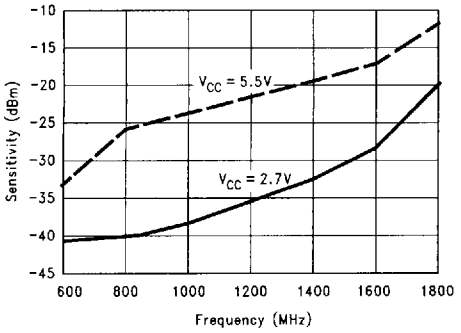
Marker 1 = 100 MHz, Real = 666, Imag. = −411
Marker 2 = 200 MHz, Real = 395, Imag. = −417
Marker 3 = 300 MHz, Real = 265, Imag. = −357
Marker 4 = 500 MHz, Real = 159, Imag. = −253

Typical Performance Characteristics (Continued)

LMX2332 RF Sensitivity vs Frequency



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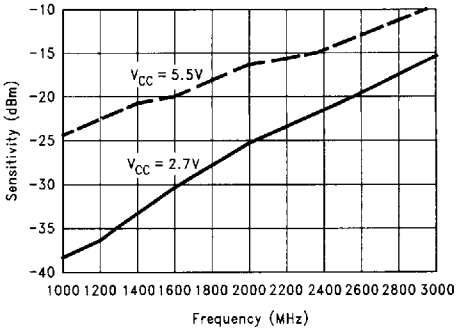
LMX2331 RF Sensitivity vs Frequency



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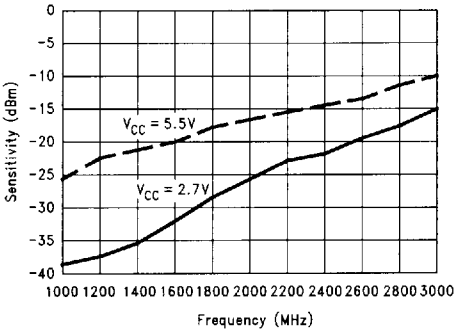
LMX2330 RF Sensitivity vs Frequency



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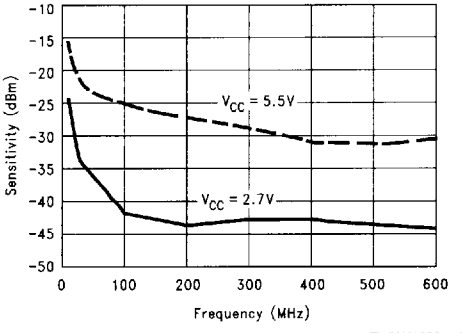
IF Input Sensitivity vs Frequency



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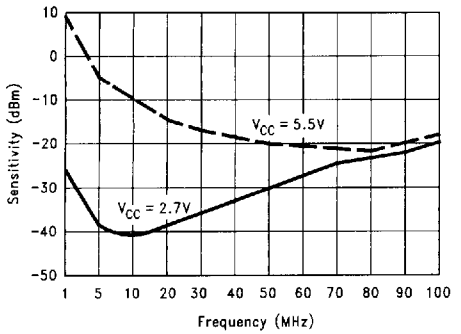
Oscillator Input Sensitivity vs Frequency



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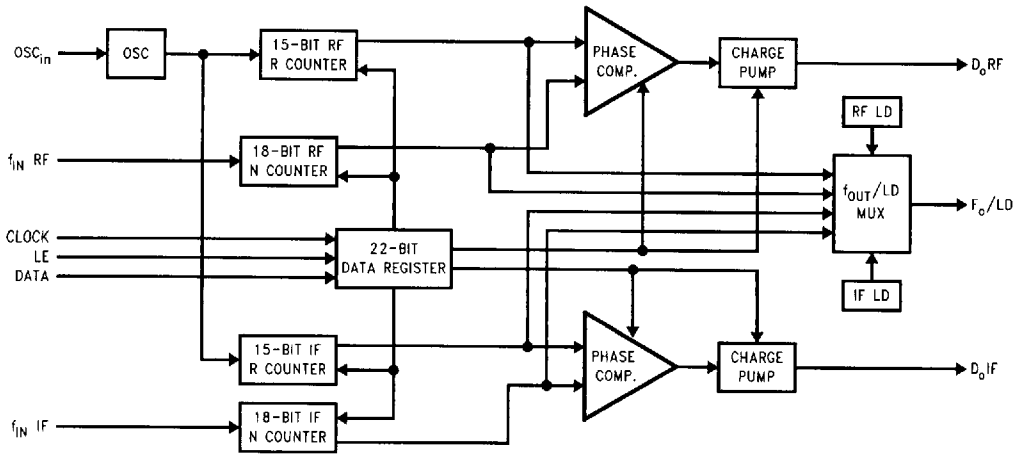
Functional Description

The simplified block diagram below shows the 22-bit data register, two 15-bit R Counters and the 15- and 18-bit N Counters (intermediate latches are not shown). The data stream is clocked (on the rising edge of LE) into the DATA input, MSB first. The last two bits are the Control Bus. The DATA is transferred into the counters as follows:

Control Bits		DATA Location
C1	C2	
0	0	IF R Counter
0	1	RF R Counter
1	0	IF N Counter
1	1	RF N Counter



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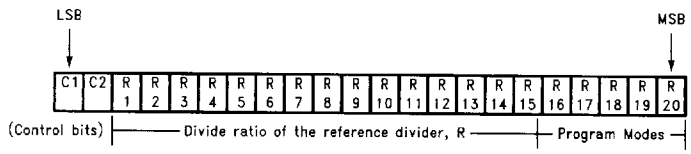
PROGRAMMABLE REFERENCE DIVIDERS (IF AND RF R COUNTERS)

If the Control Bits are 00 or 01 (00 for IF and 01 for RF) data is transferred from the 22-bit shift register into a latch which sets the 15-bit R Counter. Serial data format is shown below.



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15-BIT PROGRAMMABLE REFERENCE DIVIDER RATIO (R COUNTER)

Divide Ratio	R 15	R 14	R 13	R 12	R 11	R 10	R 9	R 8	R 7	R 6	R 5	R 4	R 3	R 2	R 1
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes: Divide ratios less than 3 are prohibited.

Divide ratio: 3 to 32767

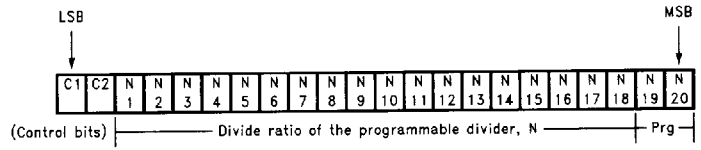
R1 to R15: These bits select the divide ratio of the programmable reference divider.

Data is shifted in MSB first.

Functional Description (Continued)

PROGRAMMABLE DIVIDER (N COUNTER)

The N counter consists of the 7-bit swallow counter (A counter) and the 11-bit programmable counter (B counter). If the Control Bits are 10 or 11 (10 for IF counter and 11 for RF counter) data is transferred from the 22-bit shift register into a 4-bit or 7-bit latch (which sets the Swallow (A) Counter) and an 11-bit latch (which sets the 11-bit programmable (B) Counter), MSB first. Serial data format is shown below. **For the IF N counter bits 5, 6, and 7 are don't care bits.** The RF N counter does not have don't care bits.



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7-BIT SWALLOW COUNTER DIVIDE RATIO (A COUNTER)

RF

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
•	•	•	•	•	•	•	•
127	1	1	1	1	1	1	1

Notes: Divide ratio: 0 to 127
B ≥ A

IF

Divide Ratio A	N 7	N 6	N 5	N 4	N 3	N 2	N 1
0	X	X	X	0	0	0	0
1	X	X	X	0	0	0	1
•	•	•	•	•	•	•	•
15	X	X	X	1	1	1	1

X = DON'T CARE condition

11-BIT PROGRAMMABLE COUNTER DIVIDE RATIO (B COUNTER)

Divide Ratio B	N 18	N 17	N 16	N 15	N 14	N 13	N 12	N 11	N 10	N 9	N 8
3	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Note: Divide ratio: 3 to 2047 (Divide ratios less than 3 are prohibited)
B ≥ A

PULSE SWALLOW FUNCTION

$f_{VCO} = [(P \times B) + A] \times f_{OSC}/R$

f_{VCO}: Output frequency of external voltage controlled oscillator (VCO)

B: Preset divide ratio of binary 11-bit programmable counter (3 to 2047)

A: Preset divide ratio of binary 7-bit swallow counter
(0 ≤ A ≤ 127 {RF}, 0 ≤ A ≤ 15 {IF}, A ≤ B)

f_{OSC}: Output frequency of the external reference frequency oscillator

R: Preset divide ratio of binary 15-bit programmable reference counter (3 to 32767)

P: Preset modulus of dual modulus prescaler (for **IF**; P = 8 or 16;
for **RF**; LMX2330: P = 32 or 64 LMX2331/32: P = 64 or 128

Functional Description (Continued)

PROGRAMMABLE MODES

Several modes of operation can be programmed with bits R16–R19 including the phase detector polarity, charge pump TRI-STATE and the output of the F_o/LD pin. The prescaler and powerdown modes are selected with bits N19 and N20. The programmable modes are shown in Table I. Truth table for the programmable modes and F_o/LD output are shown in Table II and Table III.

TABLE I. Programmable Modes

C1	C2	R16	R17	R18	R19	R20
0	0	IF Phase Detector Polarity	IF I_{CP_o}	IF D_o TRI-STATE	IF LD	IF F_o
0	1	RF Phase Detector Polarity	RF I_{CP_o}	RF D_o TRI-STATE	RF LD	RF F_o

C1	C2	N19	N20
1	0	IF Prescaler	Pwdn IF
1	1	RF Prescaler	Pwdn RF

TABLE II. Mode Select Truth Table

	ΦD Polarity	D_o TRI-STATE	I_{CP_o} (Note 1)	IF Prescaler	2330 RF Prescaler	2331/2 RF Prescaler	Pwdn (Note 2)
0	Negative	Normal Operation	LOW	8/9	32/33	64/65	Pwrd Up
1	Positive	TRI-STATE	HIGH	16/17	64/65	128/129	Pwrd Dn

Note 1: I_{CP_o} (Charge Pump current magnitude) is dependent on V_P. The I_{CP_o} LOW current state = 1/4 × I_{CP_o} HIGH current.

Note 2: Activation of the IF PLL or RF PLL powerdown modes result in the disabling of the respective N counter divider and debiasing of its respective f_{IN} inputs (to a high impedance state). Powerdown forces the respective charge pump and phase comparator logic to a TRI-STATE condition. The R counter functionality does not become disabled until *both* IF and RF powerdown bits are activated. The OSC_{in} pin reverts to a high impedance state when this condition exists. The MICROWIRE™ control register remains active amd capable of loading and latching in data during all of the powerdown modes.

TABLE III. The F_o/LD (Pin 10) Output Truth Table

RF R[19] (RF LD)	IF R[19] (IF LD)	RF R[20] (RF F_o)	IF R[20] (IF F_o)	F_o Output State
0	0	0	0	Disabled
0	1	0	0	IF Lock Detect
1	0	0	0	RF Lock Detect
1	1	0	0	RF/IF Lock Detect
X	0	0	1	IF Reference Divider Output
X	0	1	0	RF Reference Divider Output
X	1	0	1	IF Programmable Divider Output
X	1	1	0	RF Programmable Divider Output
0	1	1	1	For Internal Use Only
1	0	1	1	For Internal Use Only
1	1	1	1	For Internal Use Only

X = don't care condition

Lock Detect Output Characteristics

Output provided to indicate when the VCO frequency is in "lock." When the loop is locked and a lock detect mode is selected, the pins output is HIGH, with narrow pulses LOW. In the RF/IF lock detect mode a locked condition is indicated when IF and RF are both locked. When the F_o/LD output is disabled it is actively pulled to a low logic state.

Functional Description (Continued)

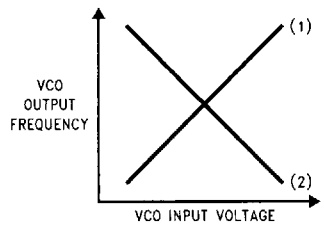
PHASE DETECTOR POLARITY

Depending upon VCO characteristics, R16 bit should be set accordingly: (see figure right)

When VCO characteristics are positive like (1), R16 should be set HIGH;

When VCO characteristics are negative like (2), R16 should be set LOW.

VCO Characteristics



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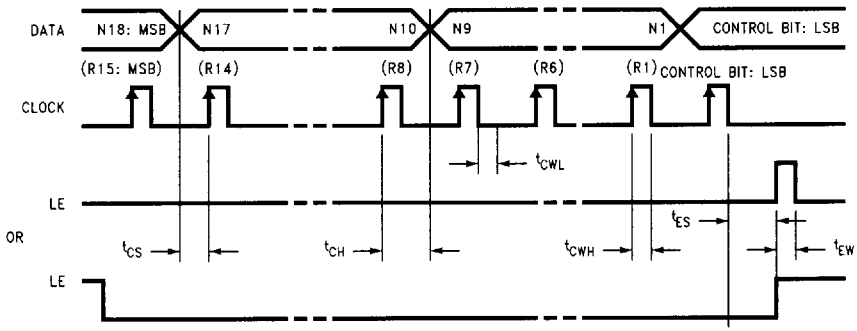
SERIAL DATA INPUT TIMING



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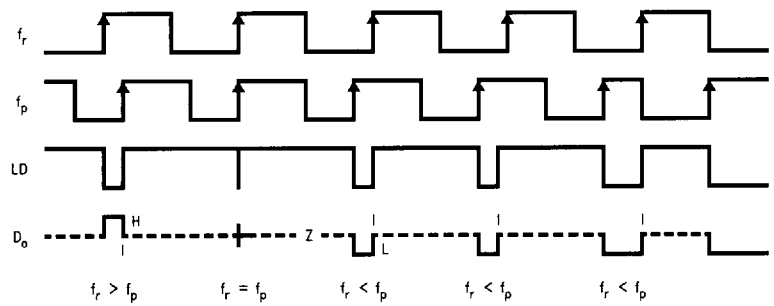
Notes: Parenthesis data indicates programmable reference divider data.

Data shifted into register on clock rising edge.

Data is shifted in MSB first.

Test Conditions: The Serial Data Input Timing is tested using a symmetrical waveform around $V_{CC}/2$. The test waveform has an edge rate of 0.6V/ns with amplitudes of 2.2V @ V_{CC} = 2.7V and 2.6V @ V_{CC} = 5.5V.

PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS



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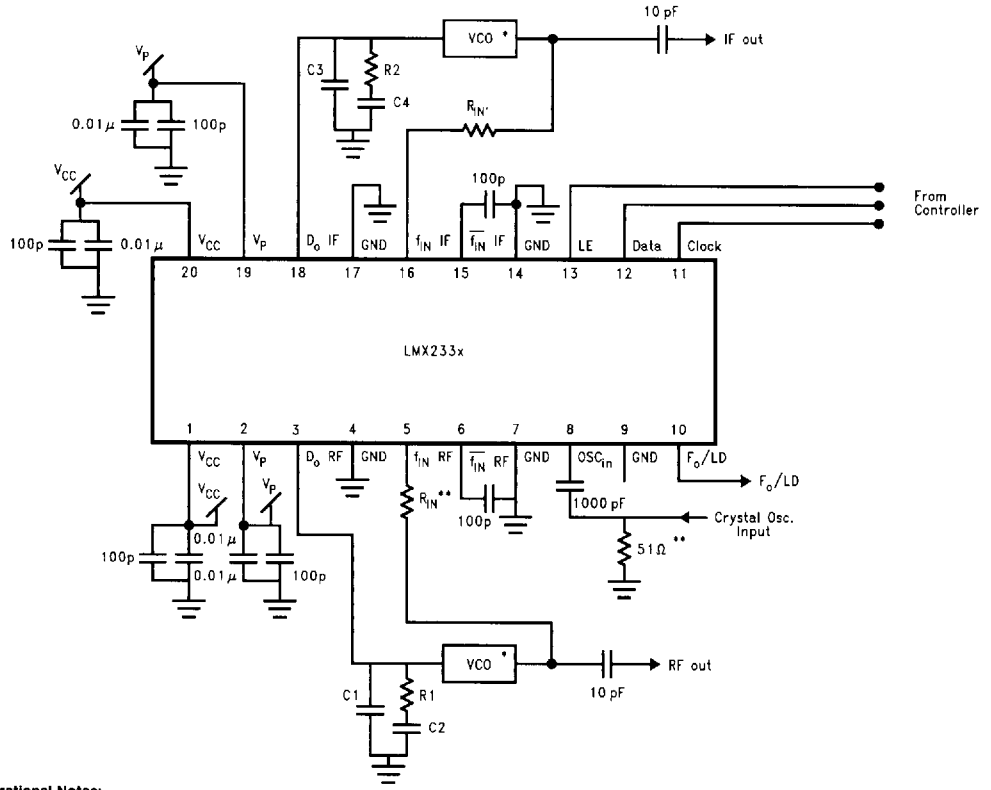
Notes: Phase difference detection range: -2π to $+2\pi$

The minimum width pump up and pump down current pulses occur at the D_o pin when the loop is locked.

R16 = HIGH

Typical Application Example



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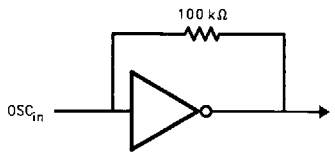
Operational Notes:

* VCO is assumed AC coupled.

** R_{IN} increases impedance so that VCO output power is provided to the load rather than the PLL. Typical values are 10Ω to 200Ω depending on the VCO power level. f_{IN} RF impedance ranges from 40Ω to 100Ω. f_{IN} IF impedances are higher.

*** 50Ω termination is often used on test boards to allow use of external reference oscillator. For most typical products a CMOS clock is used and no terminating resistor is required. OSC_{in} may be AC or DC coupled. AC coupling is recommended because the input circuit provides its own bias. (See *Figure* below)



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Proper use of grounds and bypass capacitors is essential to achieve a high level of performance. Crosstalk between pins can be reduced by careful board layout.

This is a static sensitive device. It should be handled only at static free work stations.

Application Information

LOOP FILTER DESIGN

A block diagram of the basic phase locked loop is shown.

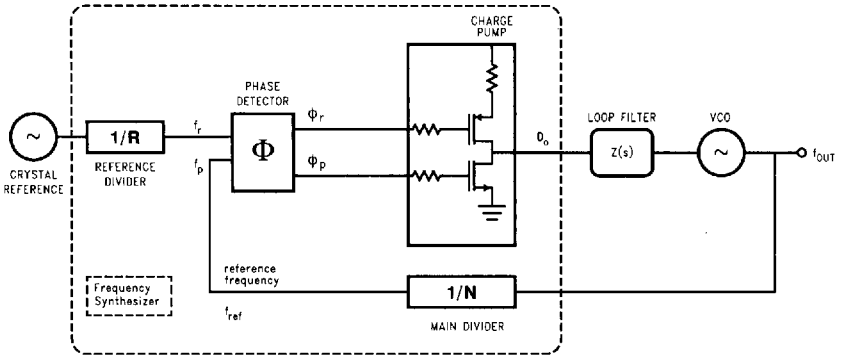

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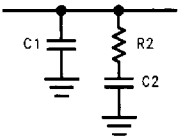
FIGURE 1. Basic Charge Pump Phase Locked Loop

An example of a passive loop filter configuration, including the transfer function of the loop filter, is shown in *Figure 2*.



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$$Z(s) = \frac{s\,(C2 \bullet R2) + 1}{s^2\,(C1 \bullet C2 \bullet R2) + sC1 + sC2}$$

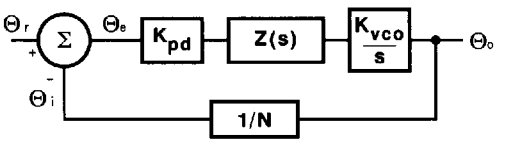
FIGURE 2. 2nd Order Passive Filter

Define the time constants which determine the pole and zero frequencies of the filter transfer function by letting

$$T2 = R2 \bullet C2 \qquad (1a)$$

and

$$T1 = R2 \bullet \frac{C1 \bullet C2}{C1 + C2} \qquad (1b)$$



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Open Loop Gain $= \theta_i/\theta_e = H(s)\,G(s) = K_{PD}\,Z(s)\,K_{VCO}/Ns$

Closed Loop Gain $= \theta_o/\theta_i = G(s)/[1 + H(s)\,G(s)]$

The PLL linear model control circuit is shown along with the open loop transfer function in *Figure 3*. Using the phase detector and VCO gain constants [$K\phi$ and K_{VCO}] and the loop filter transfer function [Z(s)], the open loop Bode plot can be calculated. The loop bandwidth is shown on the Bode plot (ωp) as the point of unity gain. The phase margin is shown to be the difference between the phase at the unity gain point and $-180°$.

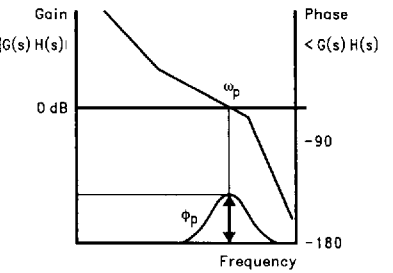

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FIGURE 3. Open Loop Transfer Function

Application Information (Continued)

Thus we can calculate the 3rd order PLL Open Loop Gain in terms of frequency

$$G(s) \bullet H(s)|_{s = j \bullet \omega} = \frac{-K\phi \bullet K_{VCO}\,(1 + j\omega \bullet T2)}{\omega^2 C1 \bullet N(1 + j\omega \bullet T1)} \bullet \frac{T1}{T2} \quad (2)$$

From equation 2 we can see that the phase term will be dependent on the single pole and zero such that

$$\phi(\omega) = \tan^{-1}(\omega \bullet T2) - \tan^{-1}(\omega \bullet T1) + 180^\circ \quad (3)$$

By setting

$$\frac{d\phi}{d\omega} = \frac{T2}{1 + (\omega \bullet T2)^2} - \frac{T1}{1 + (\omega \bullet T1)^2} = 0 \quad (4)$$

we find the frequency point corresponding to the phase inflection point in terms of the filter time constants T1 and T2. This relationship is given in equation 5.

$$\omega_p = 1/\sqrt{T2 \bullet T1} \quad (5)$$

For the loop to be stable the unity gain point must occur before the phase reaches -180°. We therefore want the phase margin to be at a maximum when the magnitude of the open loop gain equals 1. Equation 2 then gives

$$C1 = \frac{K\phi \bullet K_{VCO} \bullet T1}{\omega_p^2 \bullet N \bullet T2} \left\| \frac{(1 + j\omega_p \bullet T2)}{(1 + j\omega_p \bullet T1)} \right\| \quad (6)$$

Therefore, if we specify the loop bandwidth, ω_p, and the phase margin, ϕ_p, equations 1 through 6 allow us to calculate the two time constants, T1 and T2, as shown in equations 7 and 8. A common rule of thumb is to begin your design with a 45° phase margin.

$$T1 = \frac{\sec\phi_p - \tan\phi_p}{\omega_p} \quad (7)$$

$$T2 = \frac{1}{\omega_p^2 \bullet T1} \quad (8)$$

From the time constants T1, and T2, and the loop bandwidth, ω_p, the values for C1, R2, and C2 are obtained in equations 9 to 11.

$$C1 = \frac{T1}{T2} \bullet \frac{K\phi \bullet K_{VCO}}{\omega_p^2 \bullet N} \sqrt{\frac{1 + (\omega_p \bullet T2)^2}{1 + (\omega_p \bullet T1)^2}} \quad (9)$$

$$C2 = C1 \bullet \left(\frac{T2}{T1} - 1\right) \quad (10)$$

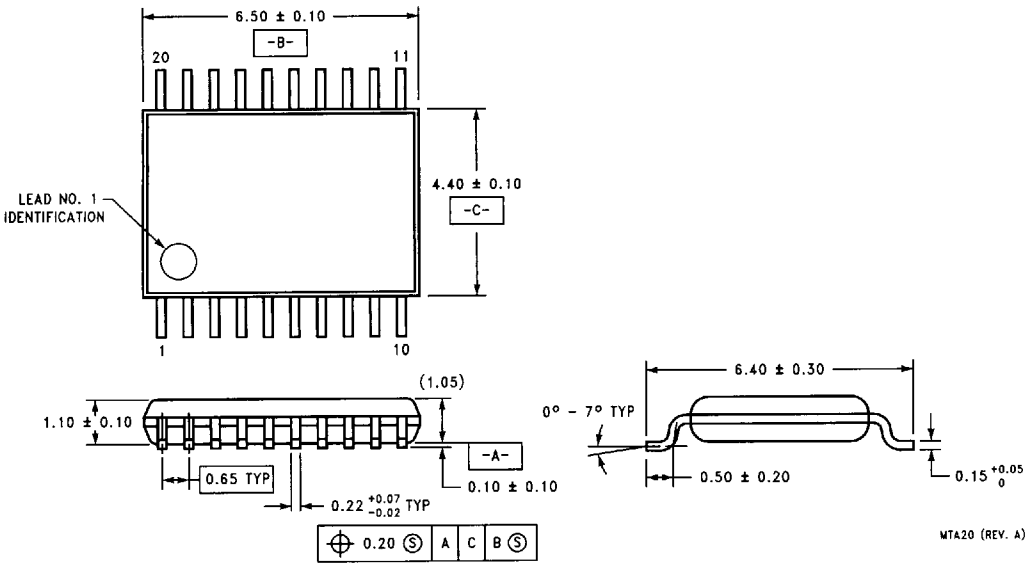
$$R2 = \frac{T2}{C2} \quad (11)$$

K_{VCO} (MHz/V)	Voltage Controlled Oscillator (VCO) Tuning Voltage constant. The frequency vs voltage tuning ratio.
$K\phi$ (mA/2πrad)	Phase detector/charge pump constant. The ratio of the current output to the input phase differential.
N	Main divider ratio. Equal to RF_{opt}/f_{ref}.
RF_{opt} (MHz)	Radio Frequency output of the VCO at which the loop filter is optimized.
f_{ref} (kHz)	Frequency of the phase detector inputs. Usually equivalent to the RF channel spacing.

In choosing the loop filter components a tradeoff must be made between lock time, noise, stability, and reference spurs. The greater the loop bandwidth the faster the lock time will be, but a large loop bandwidth could result in higher reference spurs. The reference spurs can be reduced by reducing the loop bandwidth or by adding more low pass filter stages but the lock time will increase and stability will decrease as a result. Wider loop bandwidths generally improve close in phase noise but may increase integrated phase noise depending on the reference input, VCO and division ratios used.

Lit. # 108545-001

Physical Dimensions (millimeters)



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