MOTOROLA

MC54F/74F259

Advance Information

8-BIT ADDRESSABLE LATCH

DESCRIPTION — The MC54F/74F259 is a high-speed 8-bit addressable latch designed for general purpose storage applications in digital systems. It is a multifunctional device capable of storing single line data in eight addressable latches, and also a 1-of-8 decoder and demultiplexer with active HIGH outputs. The device also incorporates an active LOW Common Clear for resetting all latches, as well as an active LOW Enable. It is functionally identical to the 9334 and 93L34 8-bit addressable latch.

- **Serial-to-Parallel Conversion**
- **Eight Bits of Storage with Output of Each Bit Available**
- **Random (Addressable) Data Entry**
- **Active High Demultiplexing or Decoding Capability**
- **Easily Expandable**
- **Common Clear**

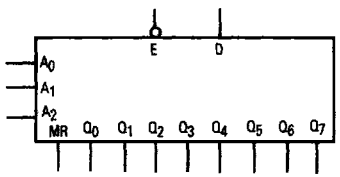
FUNCTIONAL DESCRIPTION — The MC54F/74F259 has four modes of operation as shown in the Mode Selection Table. In the addressable latch mode, data on the Data line (D) is written into the addressed latch. The addressed latch will follow the data input with all non-addressed latches remaining in their previous states in the memory mode. All latches remain in their previous state and are unaffected by the Data or Address inputs.

In the one-of-eight decoding or demultiplexing mode, the addressed output will follow the state of the D input with all other outputs in the LOW state. In the clear mode all outputs are LOW and unaffected by the address and data inputs. When operating the MC54F/74F259 as an addressable latch, changing more than one bit of the address could impose a transient wrong address. Therefore, this should only be done while in the memory mode. The Truth Table below summarizes the operations of the MC54F/74F259.

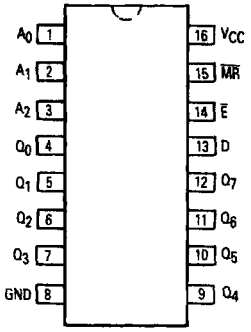
8-BIT ADDRESSABLE LATCH

FAST™ SCHOTTKY TTL

LOGIC SYMBOL



CONNECTION DIAGRAM



PIN ASSIGNMENT

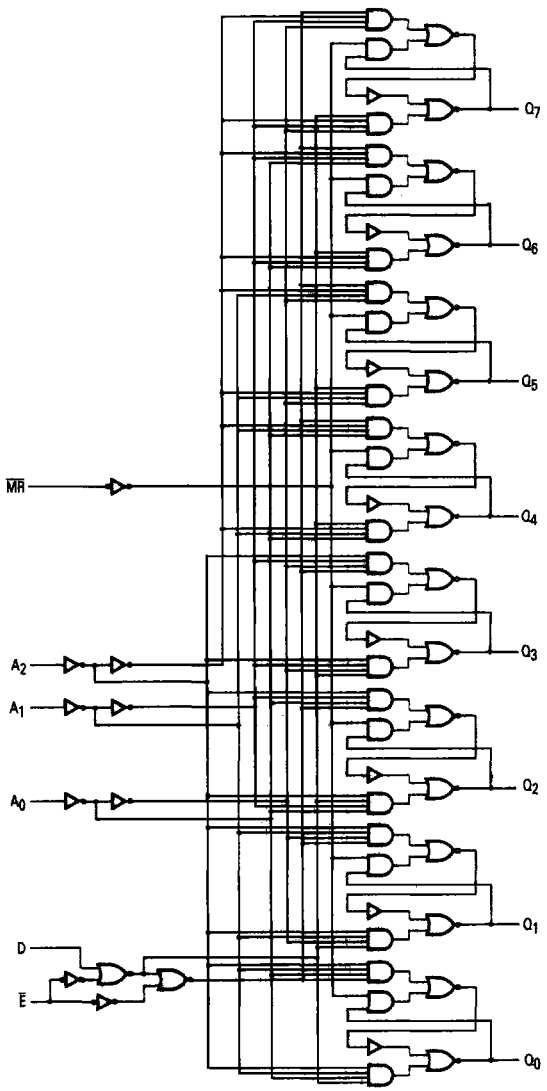
TOP VIEW

J SUFFIX — CASE 620-09 (CERAMIC DIP)
N SUFFIX — CASE 648-08 (PLASTIC DIP)
D SUFFIX — CASE 751B-03 (SOIC)

GUARANTEED OPERATING RANGES

SYMBOL	PARAMETER		MIN	TYP	MAX	UNIT
V_{CC}	Supply Voltage	54, 74	4.5	5.0	5.5	V
T_A	Operating Ambient Temperature Range	54	−55	25	125	°C
		74	0	25	70	
I_{OH}	Output Current — High	54, 74			−1.0	mA
I_{OL}	Output Current — Low	54, 74			20	mA

This document contains information on a new product. Specifications and information herein are subject to change without notice.



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

MODE SELECT TABLE

$\overline{E}$	$\overline{MR}$	Mode
L	H	Addressable Latch
H	H	Memory
L	L	Active HIGH 8-Channel Demultiplexer
H	L	Clear

H = HIGH Voltage Level
L = LOW Voltage Level

MODE SELECT-FUNCTION TABLE

Operating Mode	Inputs						Q_0	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Q_7
	$\overline{MR}$	E	D	A_0	A_1	A_2								
Master Reset	L	H	X	X	X	X	L	L	L	L	L	L	L	L
Demultiplex (Active HIGH Decoder when D=H)	L	L	d	L	L	L	Q=d	L	L	L	L	L	L	L
	L	L	d	H	L	L	L	Q=d	L	L	L	L	L	L
	L	L	d	L	H	L	L	L	Q=d	L	L	L	L	L
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	L	L	d	H	H	H	L	L	L	L	L	L	L	Q=d
Store (Do Nothing)	H	H	X	X	X	X	q_0	q_1	q_2	q_3	q_4	q_5	q_6	q_7
Addressable Latch	H	L	d	L	L	L	Q=d	q_1	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	H	L	L	q_0	Q=d	q_2	q_3	q_4	q_5	q_6	q_7
	H	L	d	L	H	L	q_0	q_1	Q=d	q_3	q_4	q_5	q_6	q_7
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	•	•	•	•	•	•	•	•	•	•	•	•	•	•
	H	L	d	H	H	H	q_0	q_1	q_2	q_3	q_4	q_5	q_6	Q=d

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
d = HIGH or LOW Data one setup time prior to the LOW-to-HIGH Enable transition
q = Lower case letters indicate the state of the referenced output established during the last cycle in which it was addressed or cleared.

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS	
V_{IH}	Input HIGH Voltage		2.0			V	Guaranteed Input HIGH Voltage	
V_{IL}	Input LOW Voltage				0.8	V	Guaranteed Input LOW Voltage	
V_{IK}	Input Clamp Diode Voltage				−1.2	V	V_{CC} = MIN, I_{IN} = −18 mA	
V_{OH}	Output HIGH Voltage	54, 74	2.5			V	I_{OL} = −1.0 mA	V_{CC} = MIN
		74	2.7			V	I_{OL} = −1.0 mA	V_{CC} = 4.75 V
V_{OL}	Output LOW Voltage				0.5	V	I_{OL} = 20 mA	V_{CC} = MIN
I_{IH}	Input HIGH Current				20	μA	V_{CC} = MAX, V_{IN} = 2.7 V	
					0.1	mA	V_{CC} = MAX, V_{IN} = 7.0 V	
I_{IL}	Input LOW Current				−0.6	mA	V_{CC} = MAX, V_{IN} = 0.5 V	
I_{OS}	Output Short Circuit Current (Note 2)		−60		−150	mA	V_{CC} = MAX, V_{OUT} = 0 V	
I_{CC}	Power Supply Current Total, Output HIGH				2.8	mA	V_{CC} = MAX, V_{IN} = GND	
	Total, Output LOW				10.2	mA	V_{CC} = MAX, V_{IN} = Open	

NOTES:
1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
2. Not more than one output should be shorted at a time, nor for more than 1 second.

AC CHARACTERISTICS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$, $V_{CC} = +5.0$ V, $C_L = 50$ pF		54F $T_A = -55$ to $+125°C$, $V_{CC} = 5.0$ V ± 10%, $C_L = 50$ pF		74F $T_A = 0$ to $+70°C$, $V_{CC} = 5.0$ V ± 10%, $C_L = 50$ pF		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_n	4.0 3.0	10.5 7.0	4.0 3.0	13 8.5	4.0 3.0	12 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay D_n to Q_n	3.5 3.0	9.0 6.5	3.5 2.5	11.5 8.5	3.5 2.5	10 7.0	ns
t_{PLH} t_{PHL}	Propagation Delay A_n to Q_n	3.5 4.0	13 9.0	3.5 4.0	15.5 11	3.5 4.0	14.5 9.5	ns
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n	5.0	9.0	4.5	11.5	4.5	10	ns

AC OPERATING REQUIREMENTS

SYMBOL	PARAMETER	54/74F $T_A = +25°C$, $V_{CC} = +5.0$ V		54F $T_A = -55$ to $+125°C$, $V_{CC} = 5.0$ V ± 10%		74F $T_A = 0$ to $+70°C$, $V_{CC} = 5.0$ V ± 10%		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW D_n to $\overline{E}$	4.0 4.0		5.0 5.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW D_n to $\overline{E}$	2.0 2.0		2.0 2.0		2.0 2.0		ns
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW A to $\overline{E}$[a]	4.0 4.0		4.0 4.0		4.0 4.0		ns
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW A to $\overline{E}$[b]	0 0		0 0		0 0		ns
t_W	$\overline{E}$ Pulse Width	4.0		4.0		4.0		ns
t_W	$\overline{MR}$ Pulse Width	4.0		4.0		4.0		ns

a. The Address to Enable setup time is the time before the HIGH-to-LOW Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

b. The Address to Enable hold time is the time after the LOW-to-HIGH Enable transition that the Address must be stable so that the correct latch is addressed and the other latches are not affected.

AC TEST CONDITIONS

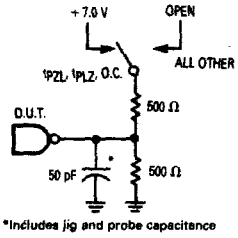
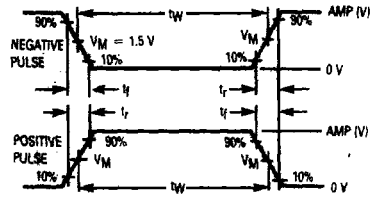


FIGURE 1 — TEST LOAD



Amplitude	Rep. Rate	Pulse Width	t_r	t_f
3.0 V	1.0 MHz	500 ns	2.5 ns	2.5 ns

FIGURE 2 — INPUT PULSE DEFINITION

AC WAVEFORMS

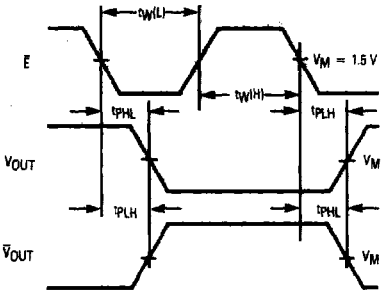


FIGURE 1 — PROPAGATION DELAY ENABLE TO OUTPUT AND ENABLE PULSE WIDTH

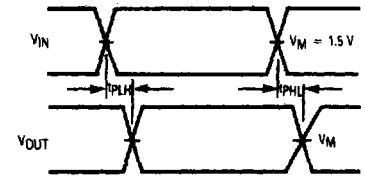


FIGURE 3 — PROPAGATION DELAY DATA TO OUTPUT

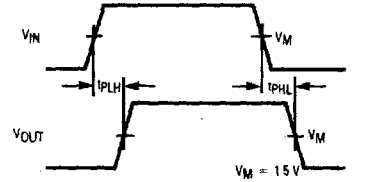


FIGURE 2 — PROPAGATION DELAY DATA TO OUTPUT

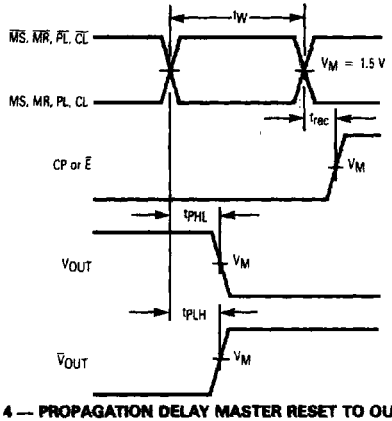


FIGURE 4 — PROPAGATION DELAY MASTER RESET TO OUTPUT AND MASTER RESET PULSE WIDTH

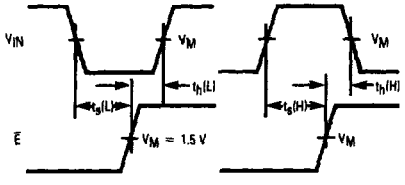


FIGURE 5 — SETUP AND HOLD TIME DATA TO ENABLE

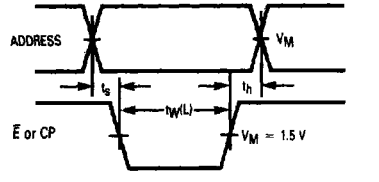


FIGURE 6 — SETUP AND HOLD TIME ADDRESS TO ENABLE