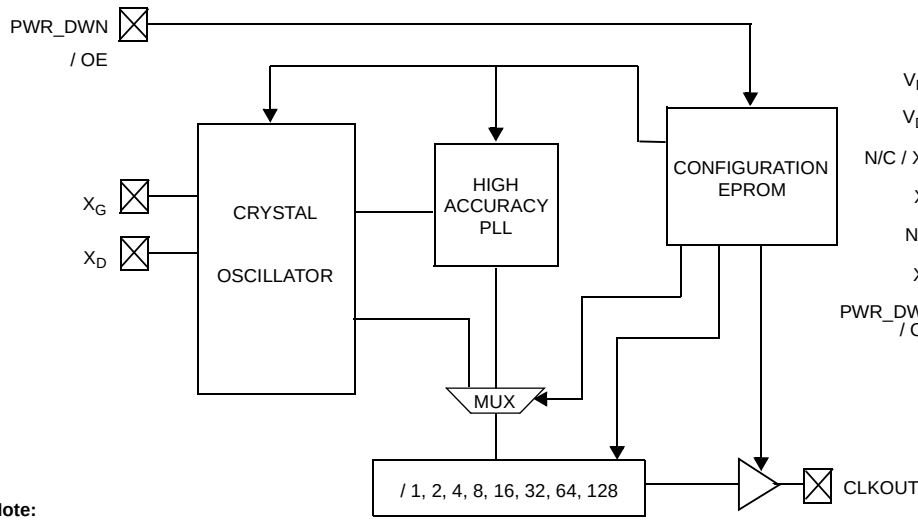
CY5037A

High-accuracy EPROM-programmable PLL Die for Crystal Oscillators

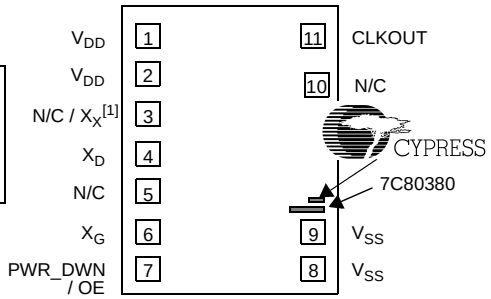
Features	Benefits
• **EPROM-programmable die for in-package programming of crystal oscillators**	Enables quick turnaround of custom oscillators Lowers inventory costs through stocking of blank parts
• **High-resolution phase-locked loop (PLL) with 12-bit multiplier and 10-bit divider**	Enables synthesis of highly accurate and stable output clock frequencies with zero or low PPM
• **EPROM-programmable capacitor tuning array with Shadow register**	Enables fine-tuning of output clock frequency by adjusting C_{Load} of the crystal
• **Twice-programmable die**	Enables reprogramming of programmed part, to correct errors, and control excess inventory
• **Simple four-wire programming interface**	Enables programming of output frequency after packaging
• **On-chip oscillator runs from 20–30 MHz fundamental tuned crystal**	Lowers cost of oscillator as PLL can be programmed to a high frequency using a low-frequency, low-cost crystal
• **EPROM-selectable TTL or CMOS duty cycle levels**	Duty cycle centered at 1.4V or $V_{DD}/2$ Provides flexibility to service most TTL or CMOS applications
• **Operating frequency** **— 1–125 MHz at 5V** **— 1–90 MHz at 3.3V** **— 1–66.6 MHz at 2.7V**	Services most PC, networking, and consumer applications
• **Sixteen selectable post-divide options, using either PLL or reference oscillator output**	Provides flexibility in output configurations and testing
• **Programmable PWR_DWN or OE pin**	Enables low-power operation or output enable function
• **Programmable asynchronous or synchronous OE and PWR_DWN modes**	Provides flexibility for system applications through selectable instantaneous or synchronous change in outputs
• **Low jitter outputs typically** **— < ± 125 ps (pk-pk) at 5V and f > 33 MHz** **— < ± 200 ps (pk-pk) at 3.3V and f > 33 MHz**	Suitable for most PC, consumer, and networking applications
• **3.3V or 5V operation**	Lowers inventory cost as same die services both applications
• **Small die**	Enables encapsulation in small-size, surface mount packages
• **Controlled rise and fall times and output slew rate**	Has lower EMI than oscillators

Logic Block Diagram



Die Configuration

Top View



Note:

1. For customers not bonding X_D or X_G pad to external pins, an alternative bonding option would be shorting the X_X pad to the X_D pad.

Functional Description

The CY5037 is an EPROM-programmable, high-accuracy, PLL-based die designed for the crystal oscillator market. The die attaches directly to a low-cost 10–30 MHz crystal and can be packaged into four-pin through-hole or surface-mount packages. The oscillator devices can be stocked as blank parts and custom frequencies programmed in-package at the last stage before shipping. This enables fast-turn manufacture of custom and standard crystal oscillators without the need for dedicated, expensive crystals.

The CY5037 contains an on-chip oscillator and an unique oscillator tuning circuit for fine-tuning the output frequency. The crystal C_{load} can be selectively adjusted by programming a set of seven EPROM bits. This feature can be used to compensate for crystal variations or to obtain a more accurate synthesized frequency.

The CY5037 uses EPROM programming with a simple two-wire, four-pin interface that includes V_{SS} and V_{DD}. Clock outputs can be generated up to 133 MHz at 5V or up to 90 MHz at 3.3V. The entire configuration can be reprogrammed one time, allowing programmed inventory to be altered or reused.

The CY5037 PLL die has been designed for very high resolution. It has a 12-bit feedback counter multiplier and a 10 bit reference counter divider. This enables the synthesis of highly accurate and stable output clock frequencies with zero or low PPM error. The clock can be further modified by eight output divider options of 1, 2, 4, 8, 16, 32, 64 and 128. The divider input can be selected as either the PLL or crystal oscillator output providing a total of sixteen separate output options. For further flexibility, the ouput is selectable between TTL and CMOS duty cycle levels.

The CY5037 also contains flexible-power management controls. These parts include both PWR_DWN and OE features with integrated pull-up resistors. The PWR_DWN and OE modes have an additional setting to determine timing (asynchronous or synchronous) with respect to the output signal. When PWR_DWN or OE modes are enabled, CLKOUT is pulled LOW by a weak pull-down. The weak pull-down is easily overdriven by another active CLKOUT for applications that require multiple CLKOUTs on a single signal path.

Controlled rise and fall times, unique output driver circuits, and innovative circuit layout techniques enable the CY5037 to have low jitter and accurate outputs making it suitable for most PC, networking, and consumer applications.

EPROM Configuration Block

Table 1 summarizes the features that are configurable by EPROM. Please refer to the "*7C8038X/7C8034X Programming Specification*" for further details. The specification can be obtained from your Cypress factory representative.

Table 1. EPROM Adjustable Features

Adjust Frequency	Feedback counter value (P)
	Reference counter value (Q)
	Output divider selection
Oscillator Tuning (load capacitance values)	
Duty cycle levels (TTL or CMOS)	
Power management mode (OE or PWR_DWN)	
Power management timing (synchronous or asynchronous)	

PLL Output Frequency

The CY5037 contains a high-resolution PLL with 12-bit multiplier and 10-bit divider.The output frequency of the PLL is determined by the following formula:

$$F_{PLL} = \frac{2 \bullet (P + 5)}{(Q + 2)} \bullet F_{REF}$$

where P is the feedback counter value and Q is the reference counter value. P and Q are EPROM-programmable values.

Power-management Features

The CY5037 contains EPROM-programmable PWR_DWN and OE functions. If power-down is selected, all active circuitry on the chip is shut down when the control pin goes LOW. The oscillator and PLL circuits must re-lock when the part leaves power-down mode. If output enable mode is selected, the output is three-stated and weakly pulled LOW when the control pin goes LOW. In this mode the oscillator and PLL circuits continue to operate, allowing a rapid return to normal operation when the control input is deasserted.

In addition, the PWR_DWN and OE modes can be programmed to occur synchronously or asynchronously with respect to the output signal. When the asynchronous setting is used, the power-down or output disable occurs immediately (allowing for logic delays) regardless of position in the clock cycle. However, when the synchronous setting is used, the part waits for a falling edge at the output before power-down or output enable signal is initiated, thus preventing output glitches. In either asynchronous or synchronous setting, the output is always enabled synchronously by waiting for the next falling edge of the output.

Crystal Oscillator Tuning Circuit

The CY5037 contains a unique tuning circuit to fine-tune the output frequency of the device. The tuning circuit consists of an array of eleven load capacitors on both sides of the oscillator drive inverter. The capacitor load values are EPROM programmable and can be increased in small increments. As the capacitor load is increased the circuit is fine-tuned to a lower frequency. The capacitor load values vary from 0.17 pF to 8 pF for a 100:1 total control ratio. The tuning increments are shown in the table below. Please refer to the "*7C8038X/7C8034X Programming Specification*" for further details.

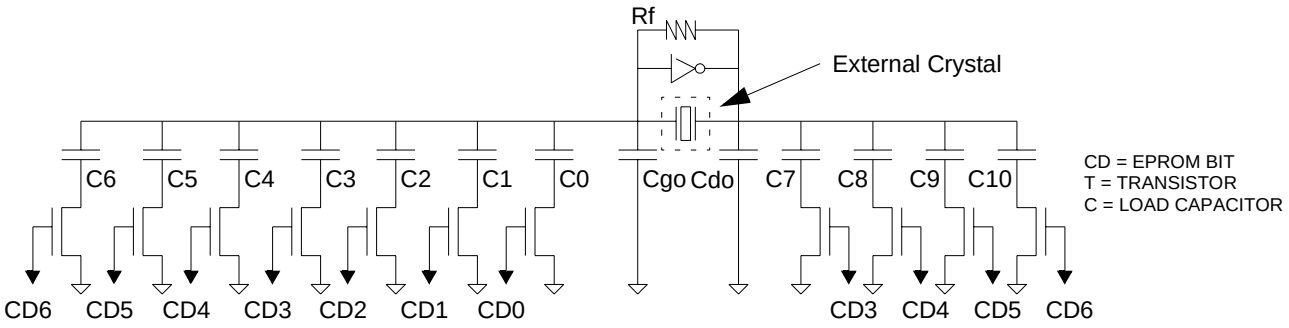
Die Pad Summary

Name	Die Pad	Description
V_{DD}	1, 2	Voltage supply
V_{SS}	8,9	Ground
X_D	4	Crystal connection (drain pin).
X_X	3	No connect. (For customers not bonding X_D or X_G pad to external pins, an alternative bonding option would be shorting this pad to X_D pad.)
X_G	6	Crystal connection (gate pin).
PWR_DWN/OE	7	EPROM programmable power down or output enable pad. Serves as V_{PP} in programming mode for all devices.
CLKOUT	11	Clock output. Also serves as three-state input during programming.
N/C	5, 10	No connect. (Do not bond to these pads.)

Device Functionality: Output Frequencies

Parameter	Description	Condition	Min.	Max.	Unit
Fo	Output Frequency	V_{DD} = 4.5 – 5.5V	1	125	MHz
		V_{DD} = 3.0 – 3.6V	1	90	MHz
		V_{DD} = 2.7 – 3.0V	1	66.6	MHz

Crystal Oscillator Tuning Circuit



Parameter	Description	Min.	Typ.	Max.	Unit
R_f	Feedback resistor, V_{DD} = 4.5 – 5.5V Feedback resistor, V_{DD} = 2.7 – 3.6V	0.5 1.0	2 4	3.5 9.0	MΩ MΩ
	Capacitors have ± 20% tolerance				
C_g	Gate capacitor		13		pF
C_d	Drain capacitor56		9		pF
C_0	Series cap		0.27		pF
C_1	Series cap		0.52		pF
C_2	Series cap		1.00		pF
C_3	Series cap		0.7		pF
C_4	Series cap		1.4		pF
C_5	Series cap		2.6		pF
C_6	Series cap		5.0		pF
C_7	Series cap		0.45		pF
C_8	Series cap		0.85		pF
C_9	Series cap		1.7		pF
C_{10}	Series cap		3.3		pF

Absolute Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage .....–0.5 to +7.0V

Input and Output Voltage .....–0.5V to V_{DD} +0.5

Input Current ..... –1 mA to 1 mA

Storage Temperature (Non-condensing) .... –55°C to +150°C

Junction Temperature. ..... –40°C to +100°C

Static Discharge Voltage .....> 2000V
(per MIL-STD-883, Method 3015)

Output Current with absolute
max output voltage ..... –10 mA to 10 mA

Operating Conditions

Parameter	Description	Min.	Max.	Unit
V_{DD}	Supply Voltage (3.3V) Supply Voltage (5.0V)	2.7 4.5	3.6 5.5	V V
T_{AJ} [2]	Operating Temperature, Junction	–10	+100	°C
C_{TTL}	Max. Capacitive Load on outputs for TTL levels V_{DD} = 4.5–5.5V, Output frequency = 1 – 66.6 MHz V_{DD} = 4.5–5.5V, Output frequency = 66.6 – 125 MHz		 50 25	 pF pF
C_{CMOS}	Max. Capacitive Load on outputs for CMOS levels V_{DD} = 4.5–5.5V, Output frequency = 1 – 66.6 MHz V_{DD} = 4.5–5.5V, Output frequency = 66.6 – 125 MHz V_{DD} = 3.0–3.6V, Output frequency = 1 – 40 MHz V_{DD} = 3.0–3.6V, Output frequency = 40 – 90 MHz V_{DD} = 2.7–3.0V, Output frequency = 1 – 66.6 MHz		 50 25 30 15 15	 pF pF pF pF pF
X_{REF}	Reference frequency, input crystal. Fundamental tuned crystals only.	20	30	MHz

Electrical Characteristics Over the Operating Range (part was characterized in a 20-pin SOIC package with external crystal; electrical characteristics may change with other package types)

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level Input Voltage	V_{DD} = 4.5–5.5V V_{DD} = 2.7–3.6V			0.8 $0.2V_{DD}$	V V
V_{IH}	High-level Input Voltage	V_{DD} = 4.5–5.5V V_{DD} = 2.7–3.6V	2.0 $0.7V_{DD}$			V V
V_{OL}	Low-level Output Voltage	V_{DD} = 4.5–5.5V, I_{OL}= 16 mA V_{DD} = 2.7–3.6V, I_{OL}= 8 mA			0.4 0.4	V V
V_{OHC}	High-level Output Voltage, CMOS levels	V_{DD} = 4.5–5.5V, I_{OH}= –16 mA V_{DD} = 2.7–3.6V, I_{OH}= –8 mA	V_{DD} – 0.4 V_{DD} – 0.4			V V
V_{OHT}	High-level Output Voltage, TTL levels	V_{DD} = 4.5–5.5V, I_{OH}= –8 mA	2.4			V
I_{IL}	Input Low Current	V_{IN} = 0V	–10			µA
I_{IH}	Input High Current	V_{IN} = V_{DD}			5	µA
I_{OP}	Power Supply Current, Unloaded	V_{DD} = 4.5– 5.5V, Output frequency <= 125 MHz V_{DD} = 2.7–3.6V, Output frequency <= 90 MHz			45 25	mA mA
I_{PD} [3]	Stand-by current	V_{DD} = 2.7–3.6V		10	50	µA
I_{OZ}	Output leakage current (OE enabled)	VDD = 2.7–5.5V, with output disabled[4]		1	50	µA
R_{UP}	Input Pull-Up Resistor	V_{DD} = 4.5–5.5V, V_{IN} = 0V V_{DD} = 4.5–5.5V, V_{IN} = 0.7 V_{DD}	1.1 50	3.0 100	8.0 200	MΩ kΩ

Notes:

2. This product is sold in die form so operating conditions are specified for the die, or junction temperature.
3. If external reference is used, it is required to stop the reference (set reference to LOW) during power down.
4. When PD is enabled, output is driven LOW. See V_{OL} spec.

Output Clock Switching Characteristics Over the Operating Range[5]

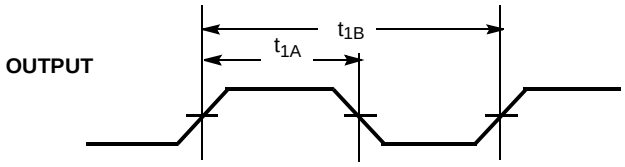
Parameter	Description	Test Conditions	Min.	Typ.	Max.	Unit
dt5	Output Duty Cycle at 1.4V, V_{DD} = 4.5–5.5V dt5 = $t_{1A} \div t_{1B}$	1–27 MHz, C_L <= 50 pF 1-50MHz, C_L <= 25 pF 27–66.6 MHz, C_L <= 50 pF 50–125 MHz, C_L <= 25 pF 66.6–125 MHz, C_L <= 15 pF 1–80MHz, C_L <= 15 pF	45 45 40 35 40 45		55 55 60 60 60 55	%
dc5	Output Duty Cycle at V_{DD}/2, V_{DD} = 4.5–5.5V dc5 = $t_{1A} \div t_{1B}$	1–40 MHz, C_L <= 50 pF 1–66.6MHz, C_L <= 50 pF 1–66.6 MHz, C_L <= 25 pF 66-125 MHz, C_L <= 25 pF	45 40 45 40		55 60 55 60	%
dc3	Output Duty Cycle at V_{DD}/2, V_{DD} = 3.0–3.6 dc3 = $t_{1A} \div t_{1B}$	1–40 MHz, C_L <= 30 pF 40–90 MHz, C_L <= 15 pF	45 40		55 60	%
d3	Output Duty Cycle at V_{DD}/2, V_{DD} = 2.7–3.0 d3 = $t_{1A} \div t_{1B}$	1–40 MHz, C_L <= 15 pF	40		60	%
tr1	Output Clock Rise time	Between 0.8 –2.0V, V_{DD} = 4.5V–5.5V			2.0	ns
tr2	Output Clock Rise time	Between 0.2V_{DD}– 0.8V_{DD}, V_{DD}= 4.5V–5.5V Between 0.2V_{DD}– 0.8V_{DD}, V_{DD}= 2.7V–3.6V			4.0 4.0	ns
tf1	Output Clock Fall time	Between 2.0 –0.8V, V_{DD} = 4.5V–5.5V			2.0	ns
tf2	Output Clock Fall time	Between 0.8V_{DD}– 0.2V_{DD}, V_{DD}= 4.5V–5.5V Between 0.8V_{DD}– 0.2V_{DD}, V_{DD}= 2.7V–3.6V			4.0 4.0	ns
t_3	Start-up time out of power-down	PWR_DWN or OE pin LOW to HIGH[4]		1	5	ms
t_{4a}	Power-down delay time (synchronous setting)	PWR_DWN pin LOW to output LOW (T = period of Output CLK)		T/2	T+25	ns
t_{4b}	Power-down delay time (asynchronous setting)	PWR_DWN pin LOW to output LOW		10	25	ns
t_5	Power-up time	From power-on[6]		1	5	ms
t_{6a}	Output disable time (synchronous setting)	OE pin LOW to output High-Z (T = period of Output CLK)		T/2	T + 25	ns
t_{6b}	Output disable time (asynchronous setting)	OE pin LOW to output High-Z		10	25	ns
t_7	Output enable time (always synchronous enable)	PWR_DWN or OE pin LOW to HIGH (T = period of Output CLK)		T	1.5T + 25	ns
t_j	Peak-to-Peak Period Jitter	V_{DD}= 4.5–5.5V, C_L=15 pF, Fo>33 MHz, VCO > 100 MHz V_{DD}= 3.0–3.6V, C_L=15 pF, Fo>33 MHz, VCO > 100 MHz V_{DD}= 3.0–5.5V, C_L=15 pF,16 MHz < Fo < 33 MHz V_{DD}= 3.0–5.5V, C_L=15 pF,1 MHz < Fo < 16 MHz		±75 ±100	± 125 ± 200 ± 300 ± 500	ps
F_{VCO}	VCO frequency	V_{DD}= 4.5–5.5V V_{DD}= 3.0–3.6V V_{DD}= 2.7–3.0V	50 50 50		250 180 135	MHz

Notes:

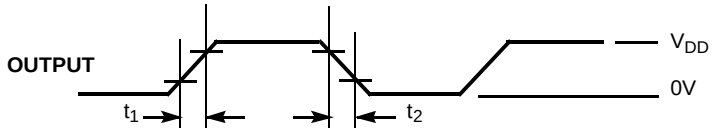
5. Oscillator start time cannot be guaranteed for all crystal types. This specification is for operation with AT cut crystals with ESR < 70Ω.
6. Not all parameters measured in production testing.

Switching Waveforms

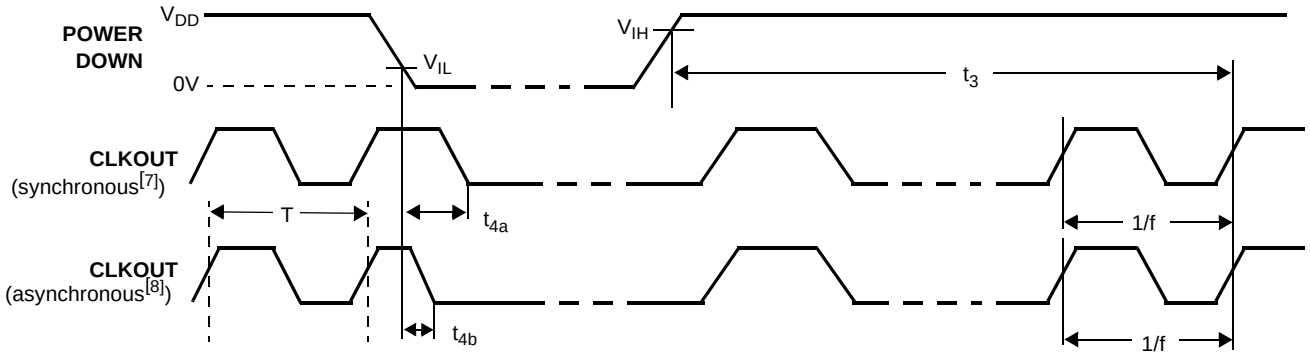
Duty Cycle Timing (dt5, dc5, dc3, d3)



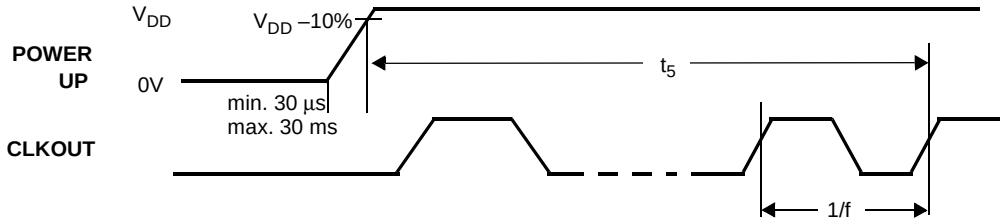
Output Rise/Fall Time



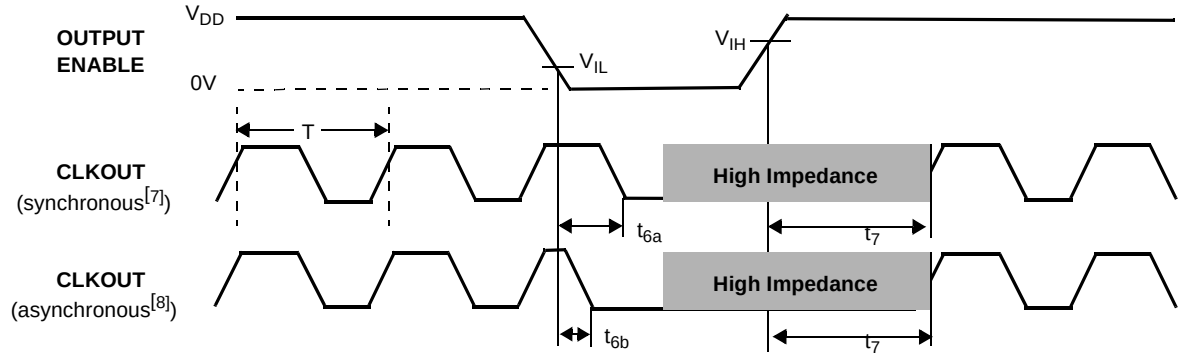
Power-down Timing (synchronous and asynchronous modes)



Power-up Timing



Output Enable Timing (synchronous and asynchronous modes)



Notes:

7. In synchronous mode the powerdown or output three-state is not initiated until the next falling edge of the output clock.
8. In asynchronous mode the powerdown or output three-state occurs within 25 ns regardless of position in the ouput clock cycle.

Ordering Information*

Ordering Code	Type	Operating Range
CY5037AWAF	Wafer	–10°C to 100°C

Die Information

Wafer Thickness	14 ± 0.5 mils

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Document Number: 38-07208

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	111726	12/02/01	DSG	Change from Spec number: 38-01132 to 38-07208
*A	113700	05/02/02	CKN	Added “and Output” to Absolute Max. Ratings on p. 5 Added I_{OH} and I_{OL} rows to Electrical Characteristics table on p. 5 Removed 10 in the Max. column of the I_{IL} row and added -10 in the Min. column