NOTICE
SEE ORDER OF DATA FOR ERRATA INFORMATION

T-46-23-14

Integrated Device Technology, Inc.

CMOS STATIC RAM 256K (32K x 8-BIT)

IDT71256S
IDT71256L

FEATURES:

- Optimized for fast RISC processors including the IDT79R3000
- High-speed address/chip select time
  - — Military: 25/30/35/45/55/70/85/100/120/150ns (max.)
  - — Commercial: 20/25/30/35/45ns (max.)
- Low-power operation
- Battery Backup operation — 2V data retention
- Produced with advanced high-performance CEMOS™ technology
- Single 5V(±10%) power supply
- Input and output directly TTL-compatible
- Static operation: no clocks or refresh required
- Available in standard 28-pin (600 mil) CERDIP, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebraze DIP, 28-pin (330 mil) SOIC and (300 mil) SOJ, 28-pin CERPACK, 32-pin LCC or PLCC, 28-pin LCC
- Military product compliant to MIL-STD-883, Class B
- This function is listed as Standard Military Drawing #5962-88552 (L-Power) and #5962-88662 (S-Power)

DESCRIPTION:

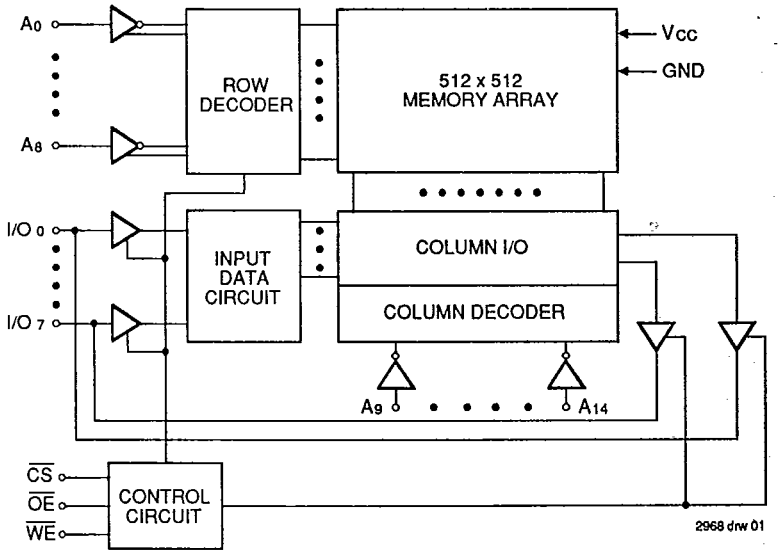
The IDT71256 is a 262,144-bit high-speed static RAM organized as 32K x 8. It is fabricated using IDT's high-performance, high-reliability CEMOS technology. This state-of-the-art technology, combined with innovative circuit design techniques, provides a cost effective alternative to bipolar and fast NMOS memories. Timing parameters have been specified to meet the speed demands of the fastest IDT79R3000 RISC processors.

Address access times as fast as 20ns are available with power consumption of only 350mW (typ.). The circuit also offers a reduced power standby mode. When $\overline{CS}$ goes high, the circuit will automatically go to, and remain in, a low-power standby mode as long as $\overline{CS}$ remains high. In the full standby mode, the low-power device consumes less than 15µW, typically. This capability provides significant system level power and cooling savings. The low power (L) version also offers a battery backup data retention capability where the circuit typically consumes only 5µW when operating off a 2V battery.

The IDT71256 is packaged in a 28-pin (330 mil) gull-wing or (300 or 350 mil) J-bend SOIC, a 28-pin 600 mil CERDIP, 28-pin (300 or 600 mil) plastic DIP, 28-pin (300 mil) ceramic sidebraze DIP, 28-pin CERPACK, 32-pin LCC or PLCC, 28-pin LCC, providing high board-level packing densities.

The IDT71256 military RAM is manufactured in compliance with the latest revision of MIL-STD-883, Class B, making it ideally suited to military temperature applications demanding the highest level of performance and reliability.

FUNCTIONAL BLOCK DIAGRAM



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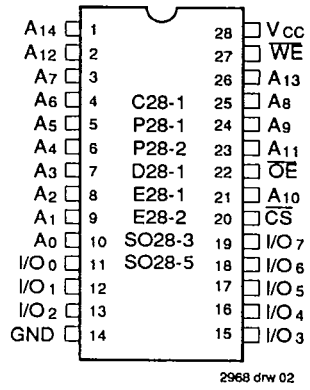
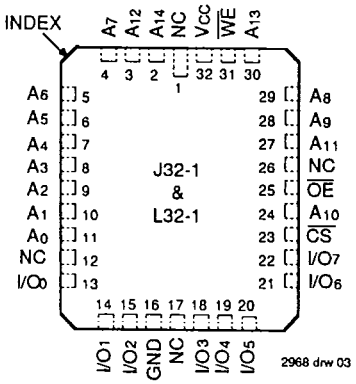
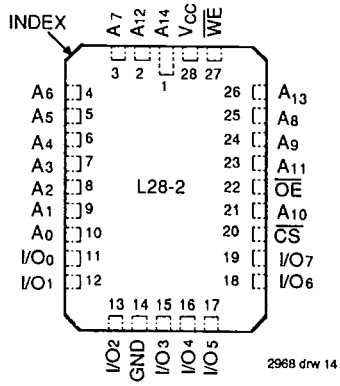
PIN CONFIGURATIONS



DIP/SOJ/SOIC
TOP VIEW



32-Pin LCC/PLCC
TOP VIEW



28-Pin LCC
TOP VIEW

PIN DESCRIPTIONS

Name	Description
A_0–A_{14}	Addresses
I/O_0–I/O_7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
GND	Ground
VCC	Power

2968 tbl 01

TRUTH TABLE(1)

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
X	H	X	High-Z	Standby (I_{SB})
X	V_{HC}	X	High-Z	Standby (I_{SB1})
H	L	H	High-Z	Output Disable
H	L	L	D_{OUT}	Read
L	L	X	D_{IN}	Write

NOTE:
1. H = V_{IH}, L = V_{IL}, X = Don't Care

2968 tbl 02

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Com'l.	Mil.	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to +7.0	-0.5 to +7.0	V
T_A	Operating Temperature	0 to +70	-55 to +125	°C
T_{BIAS}	Temperature Under Bias	-55 to +125	-65 to +135	°C
T_{STG}	Storage Temperature	-55 to +125	-65 to +150	°C
P_T	Power Dissipation	1.0	1.0	W
I_{OUT}	DC Output Current	50	50	mA

NOTE:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2968 tbl 03

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V	11	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	11	pF

NOTE:
1. This parameter is determined by device characterization, but is not production tested.

2968 tbl 04

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Temperature	GND	Vcc
Military	-55°C to +125°C	0V	5.0V ± 10%
Commercial	0°C to +70°C	0V	5.0V ± 10%

2968 tbl 05

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
Vcc	Supply Voltage	4.5	5.0	5.5	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.2	—	6.0	V
V_{IL}	Input Low Voltage	-0.5[1]	—	0.8	V

NOTE:
1. V_{IL} (min.) = -3.0V for pulse width less than 20ns.

2968 tbl 06

DC ELECTRICAL CHARACTERISTICS[1, 2]

(V_{CC} = 5.0V ± 10%, V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V)

Symbol	Parameter	Power	71256x20		71256x25		71256x30		71256x35		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[3]	S	155	—	145	150	170	180	155	165	mA
		L	135	—	115	130	145	160	130	145	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	—	20	20	20	20	20	20	mA
		L	3	—	3	3	3	3	3	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{LC} \ge V_{IN} \ge V_{HC}$, f = 0	S	15	—	15	20	15	20	15	20	mA
		L	0.4	—	0.4	1.5	0.4	1.5	0.4	1.5	

Symbol	Parameter	Power	71256x45		71256x55		71256x70		71256x85[5]		71256x100		Unit
			Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	Com'l.	Mil.	
I_{CC}	Dynamic Operating Current $\overline{CS} \le V_{IL}$, Outputs Open V_{CC} = Max., f = f_{MAX}[3]	S	140	150	—	150	—	150	—	150	—	150	mA
		L	120	135	—	125	—	125	—	125	—	125	
I_{SB}	Standby Power Supply Current (TTL Level) $\overline{CS} \ge V_{IH}$, V_{CC} = Max., Outputs Open, f = f_{MAX}[3]	S	20	20	—	20	—	20	—	20	—	20	mA
		L	3	3	—	3	—	3	—	3	—	3	
I_{SB1}	Full Standby Power Supply Current (CMOS Level) $\overline{CS} \ge V_{HC}$, V_{CC} = Max., $V_{LC} \ge V_{IN} \ge V_{HC}$, f = 0	S	15	20	—	20	—	20	—	20	—	20	mA
		L	0.4	1.5	—	1.5	—	1.5	—	1.5	—	1.5	

NOTES:
1. All values are maximum guaranteed values.
2. An "x" in part numbers indicate power rating (S or L).
3. f_{MAX} = 1/t_{RC}.
4. Standby current mode not available at 20ns.
5. Also available: 120 and 150 ns military devices.

2968 tbl 07

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 and 2

2968 tbl 08

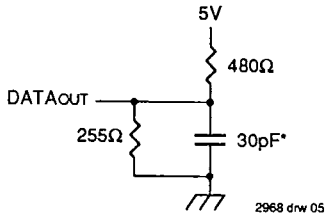


Figure 1. Output Load

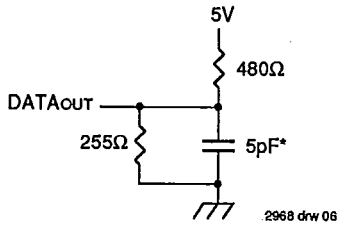


Figure 2. Output Load
(for t_{CLZ}, t_{OLZ}, t_{CHZ}, t_{OHZ}, t_{OW}, t_{WHZ})

*Includes scope and jig capacitances

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DC ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%

Symbol	Parameter	Test Condition		IDT71256S Min.	IDT71256S Typ.	IDT71256S Max.	IDT71256L Min.	IDT71256L Typ.	IDT71256L Max.	Unit
$\|I_{LI}\|$	Input Leakage Current	V_{CC} = Max., V_{IN} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
$\|I_{LO}\|$	Output Leakage Current	V_{CC} = Max., $\overline{CS}$ = V_{IH}, V_{OUT} = GND to V_{CC}	MIL.	—	—	10	—	—	5	µA
			COM'L.	—	—	5	—	—	2	
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.			—	0.4	—	—	0.4	V
		I_{OL} = 10mA, V_{CC} = Min.		—	—	0.5	—	—	0.5	
V_{OH}	Output High Voltage	I_{OH} = -4mA, V_{CC} = Min.		2.4	—	—	2.4	—	—	V

2968 tbl 09

DATA RETENTION CHARACTERISTICS OVER ALL TEMPERATURE RANGES

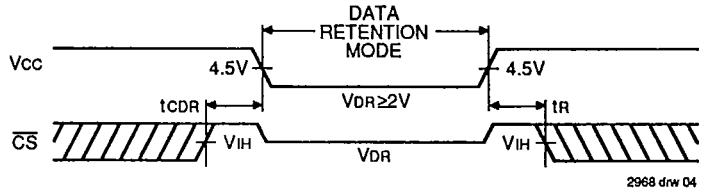
(L Version Only) V_{LC} = 0.2V, V_{HC} = V_{CC} - 0.2V

Symbol	Parameter	Test Condition		Min.	Typ.(1) Vcc @ 2.0v	Typ.(1) Vcc @ 3.0V	Max. Vcc @ 2.0V	Max. Vcc @ 3.0V	Unit
V_{DR}	Vcc for Data Retention	—		2.0	—	—	—	—	V
I_{CCDR}	Data Retention Current		MIL.	—	—	—	200	800	µA
			COM'L.	—	—	—	120	200	
t_{CDR}	Chip Deselect to Data Retention Time	$\overline{CS} \geq V_{HC}$ $V_{IN} \geq V_{HC}$ or $\leq V_{LC}$		0	—	—	—	—	ns
t_R(3)	Operation Recovery Time			t_{RC}(2)	—	—	—	—	ns

NOTES:
1. T_A = +25°C.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed, but not tested.

2968 tbl 10

LOW Vcc DATA RETENTION WAVEFORM



2968 drw 04

T-46-23-14

AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S20[1] 71256L20[1] Min.	Max.	71256S25 71256L25 Min.	Max.	71256S30 71256L30 Min.	Max.	71256S35 71256L35 Min.	Max.	71256S45 71256L45 Min.	Max.	Unit
Read Cycle												
tRC	Read Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tAA	Address Access Time	—	20	—	25	—	30	—	35	—	45	ns
tACS	Chip Select Access Time	—	20	—	25	—	30	—	35	—	45	ns
tCLZ	Chip Select to Output in Low Z[2]	5	—	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	10	—	11	—	13	—	15	—	20	ns
tOLZ	Output Enable to Output in Low Z[2]	2	—	2	—	2	—	2	—	0	—	ns
tCHZ	Chip Select to Output in High Z[2]	—	10	—	11	—	15	—	15	—	20	ns
tOHZ	Output Disable to Output in High Z[2]	2	8	2	10	2	12	2	15	—	20	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	5	—	ns
Write Cycle												
tWC	Write Cycle Time	20	—	25	—	30	—	35	—	45	—	ns
tCW	Chip Select to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAW	Address Valid to End of Write	15	—	20	—	25	—	30	—	40	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	15	—	20	—	25	—	30	—	35	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z[2]	—	10	—	11	—	15	—	15	—	20	ns
tDW	Data to Write Time Overlap	11	—	13	—	14[3]	—	15[3]	—	20	—	ns
tDH1	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time ($\overline{CS}$)	3	—	3	—	3	—	3	—	3	—	ns
tOW	Output Active from End of Write[2]	5	—	5	—	5	—	5	—	5	—	ns

2968 tbl 11

NOTES:
1. 0° to +70°C temperature range only.
2. This parameter guaranteed but not tested.
3. For the 0°C to +70°C temperature range,
   30ns speed grade, tOW = 14ns.
   35ns speed grade, tOW = 15ns.
   For the -55°C to +125°C temperature range,
   30ns speed grade, tOW = 17ns.
   35ns speed grade, tOW = 18ns.

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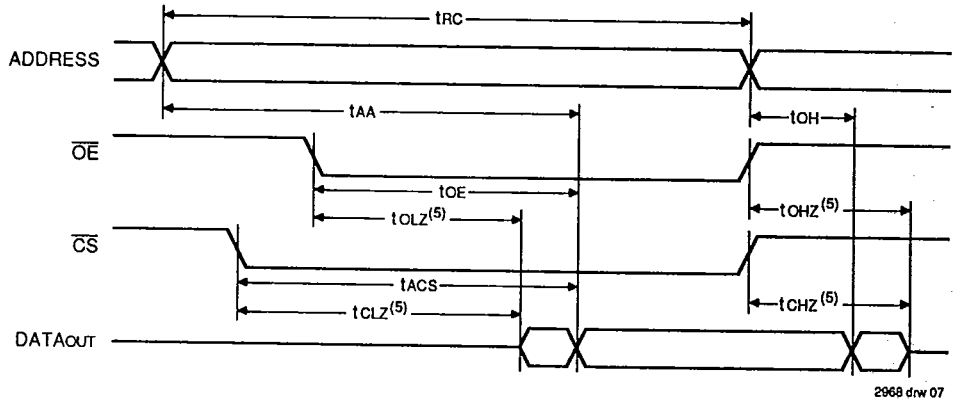
AC ELECTRICAL CHARACTERISTICS (Vcc = 5.0V ± 10%, All Temperature Ranges)

Symbol	Parameter	71256S55[1] 71256L55[1] Min.	Max.	71256S70[1] 71256L70[1] Min.	Max.	71256S85[1] 71256L85[1] Min.	Max.	71256S100[3] 71256L100[3] Min.	Max.	Unit
Read Cycle										
tRC	Read Cycle Time	55	—	70	—	85	—	100	—	ns
tAA	Address Access Time	—	55	—	70	—	85	—	100	ns
tACS	Chip Select Access Time	—	55	—	70	—	85	—	100	ns
tCLZ	Chip Select to Output in Low Z[2]	5	—	5	—	5	—	5	—	ns
tOE	Output Enable to Output Valid	—	25	—	30	—	35	—	40	ns
tOLZ	Output Enable to Output in Low Z[2]	0	—	0	—	0	—	0	—	ns
tCHZ	Chip Select to Output in High Z[2]	—	25	—	30	—	35	—	40	ns
tOHZ	Output Disable to Output in High Z[2]	0	25	0	30	—	35	—	40	ns
tOH	Output Hold from Address Change	5	—	5	—	5	—	5	—	ns
Write Cycle										
tWC	Write Cycle Time	55	—	70	—	85	—	100	—	ns
tCW	Chip Select to End of Write	50	—	60	—	70	—	80	—	ns
tAW	Address Valid to End of Write	50	—	60	—	70	—	80	—	ns
tAS	Address Set-up Time	0	—	0	—	0	—	0	—	ns
tWP	Write Pulse Width	40	—	45	—	50	—	55	—	ns
tWR	Write Recovery Time	0	—	0	—	0	—	0	—	ns
tWHZ	Write Enable to Output in High Z[2]	—	25	—	30	—	35	—	40	ns
tDW	Data to Write Time Overlap	25	—	30	—	35	—	40	—	ns
tDH1	Data Hold from Write Time ($\overline{WE}$)	0	—	0	—	0	—	0	—	ns
tDH2	Data Hold from Write Time ($\overline{CS}$)	3	—	3	—	3	—	3	—	ns
tOW	Output Active from End of Write[2]	5	—	5	—	5	—	5	—	ns

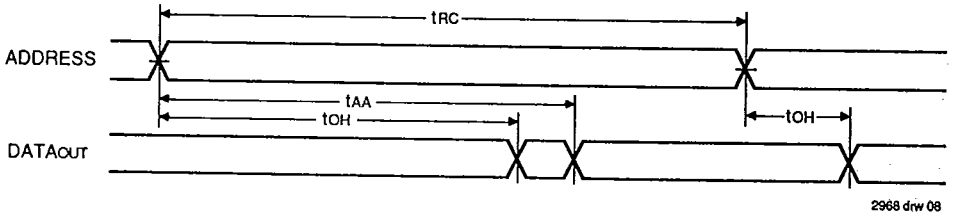
2968 tbl 11

NOTES:
1. -55°C to +125°C temperature range only.
2. This parameter guaranteed but not tested.
3. 0° to +70°C temperature range only.
4. Also available: 120 and 150 ns military devices.
5. For the 0°C to +70°C temperature range,
   30ns speed grade, tOW = 14ns.
   35ns speed grade, tOW = 15ns.
   For the -55°C to +125°C temperature range,
   30ns speed grade, tOW = 17ns.
   35ns speed grade, tOW = 18ns.

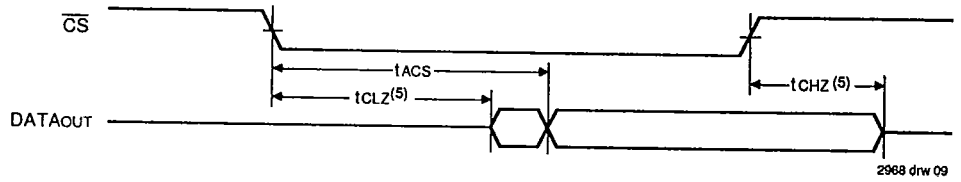
TIMING WAVEFORM OF READ CYCLE NO. 1(1)



TIMING WAVEFORM OF READ CYCLE NO. 2(1, 2, 4)

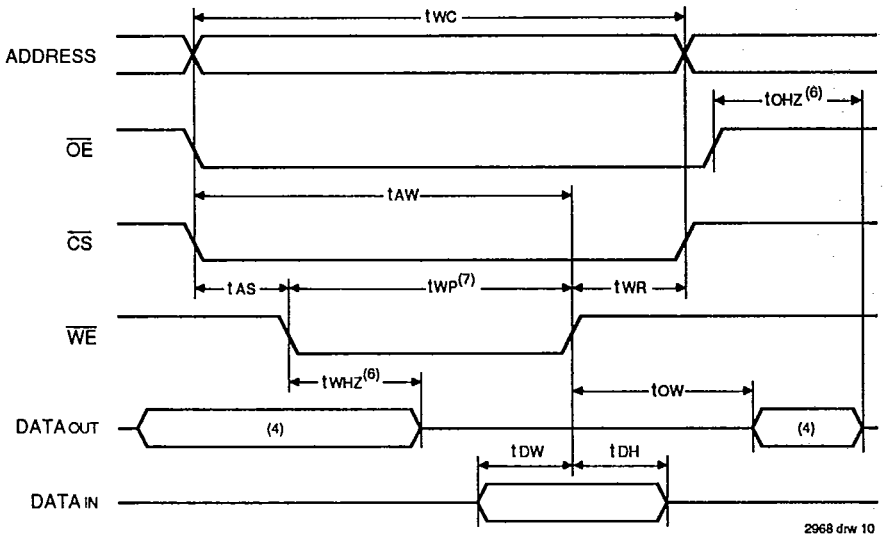


TIMING WAVEFORM OF READ CYCLE NO. 3(1, 3, 4)

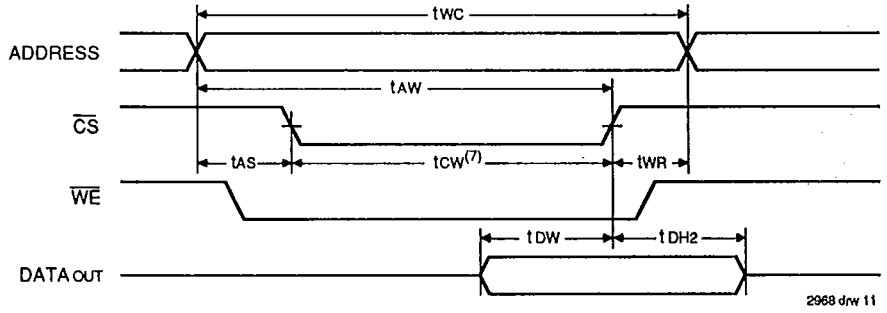


NOTES:
1. $\overline{WE}$ is high for read cycle.
2. Device is continuously selected, $\overline{CS}$ = V_{IL}.
3. Address valid prior to or coincident with $\overline{CS}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±200mV from steady state with 5pF load (including scope and jig).

TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{WE}$ CONTROLLED TIMING)(1, 2, 3, 5, 7)



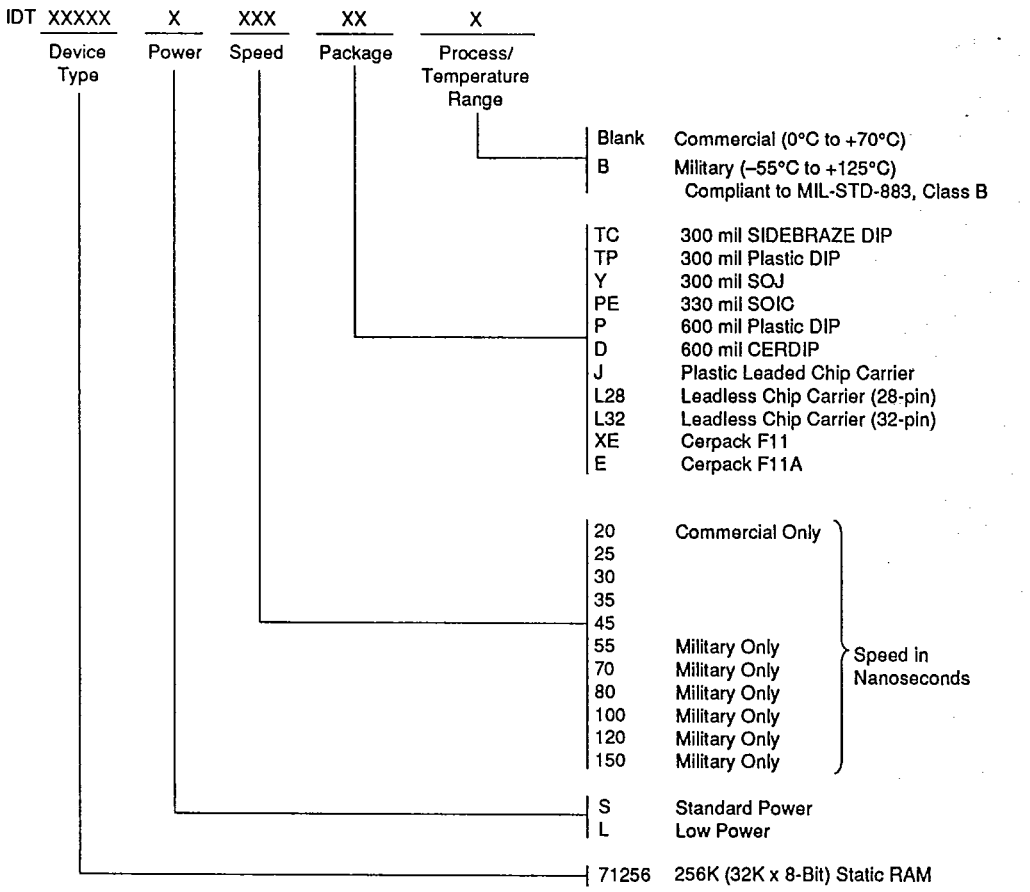
TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{CS}$ CONTROLLED TIMING)(1, 2, 3, 5)



NOTES:
1. $\overline{WE}$ or $\overline{CS}$ must be high during all address transitions.
2. A write occurs during the overlap (tCW or tWP) of a low $\overline{CS}$ and a low $\overline{WE}$.
3. tWR is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of the write cycle.
4. During this period, I/O pins are in the output state so that the input signals must not be applied.
5. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the outputs remain in a high impedance state.
6. Transition is measured ±200mV from steady state with a 5pF load (including scope and jig).
7. If $\overline{OE}$ is low during a $\overline{WE}$ controlled write cycle, the write pulse width must be the larger of tWP or (tWHZ + tDW) to allow the I/O drivers to turn off and data to be placed on the bus for the required tDW. If $\overline{OE}$ is high during a $\overline{WE}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified tWP.

ORDERING INFORMATION

T-46-23-14



2968 drw 12

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