mosaic

Mosaic Semiconductor Inc

32K x 8 SRAM

MSM832-45/55/70

Issue 2.2 : October 1993

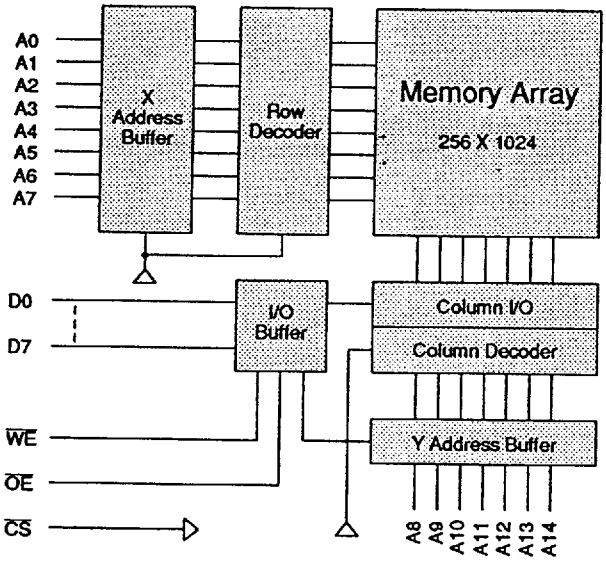
PRELIMINARY

32,768 x 8 CMOS High Speed Static RAM

Features

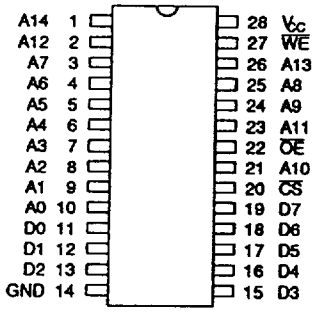
Access Times of 45/55/70 ns
Standard 28 pin DIL footprint.
Available in 28 pin VIL™ and FlatPack packages.
Operating Power 715 mW (max)
Standby Power 2.2mW (max)
Completely Static Operation.
Battery back-up capability.
Directly TTL compatible.
Common Data Inputs and Outputs.
May be Processed to MIL-STD-883, Method 5004, non-compliant.

Block Diagram

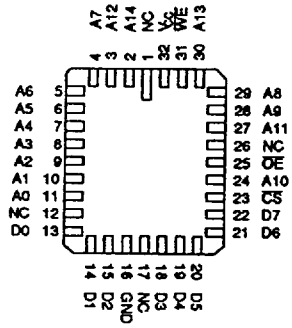


Pin Definition

Package Type: 'G', 'S', 'T', 'V'



Package Type: 'W', 'J'



Pin Functions

A0-A14	Address inputs
D0-7	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
V_{cc}	Power(+5V)
GND	Ground

Package Details Package dimensions and outlines are displayed on pages 8 & 9.

Pin Count	Description	Package Type	Material	Pin Out
28	0.6" Dual-in-Line (DIP)	S	Ceramic	JEDEC
28	0.3" Dual-in-Line (DIP)	T	Ceramic	JEDEC
28	0.1" Vertical-in-Line (VIL™)	V	Ceramic	JEDEC
28	Bottom Brazed Flat Pack	G	Ceramic	JEDEC
32	Leadless Chip Carrier (LCC)	W	Ceramic	JEDEC
32	J-Leaded Chip Carrier (JLCC)	J	Ceramic	JEDEC

VIL™ is a Trademark of Mosaic Semiconductor Inc., (U.S. Patent Des. 316251)

Absolute Maximum Ratings (1)

Voltage on any pin relative to V_{SS} (2)	V_T	-1.0V to +7	V
Power Dissipation	P_T	1	W
Storage Temperature	T_{STG}	-65 to +150	°C

Notes : (1) Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
(2) Pulse width:- 3.5V for less than 10ns.

Recommended Operating Conditions

		min	*typ*	*max*	
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Voltage	V_{IH}	2.2	-	V_{CC}+1.0	V
Input Low Voltage	V_{IL}	-0.5	-	0.8	V
Operating Temperature	T_A	0	-	70	°C
	T_{AL}	-40	-	85	°C (832I)
	T_{AM}	-55	-	125	°C (832M,832MB)

DC Electrical Characteristics (V_{CC} = 5.0V±10%, T_A=-55°C to +125°C)

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
Input Leakage Current	I_{LI}	V_{IN}=0V to V_{CC}	-5	-	5	µA
Output Leakage Current	I_{LO}	$\overline{CS}$=V_{IH} or $\overline{OE}$=V_{IH}, $V_{I/O}$=GND to V_{CC}	-5	-	5	µA
Average Supply Current	I_{CC1}	$\overline{CS}$=V_{IL}, $I_{I/O}$=0mA, Min. Cycle, Duty=100%	-	-	130	mA
Standby Supply Current	I_{SB}	$\overline{CS}$=V_{IH}, I/P's static	-	-	30	mA
	I_{SB1}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	-	20	mA
L-Version	I_{SB2}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	-	3	mA
P-Version	I_{SB3}	$\overline{CS}$≥V_{CC}-0.2V, 0.2V≥V_{IN}≥V_{CC}-0.2V	-	-	400	µA
Output Voltage	V_{OL}	I_{OL}=8.0mA	-	-	0.4	V
	V_{OH}	I_{OH}=-4.0mA	2.4	-	-	V

Typical values are at V_{CC}=5.0V, T_A=25°C and specified loading.

Capacitance (V_{CC}=5V±10%, T_A=25°C)

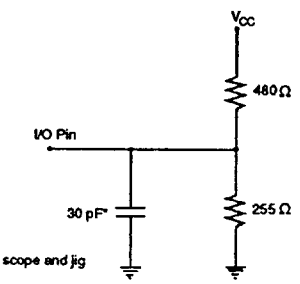
Parameter	*Symbol*	*Test Condition*	*typ*	*max*	*Unit*
Input Capacitance:	C_{IN}	V_{IN} = 0V	-	8	pF
I/O Capacitance:	$C_{I/O}$	$V_{I/O}$= 0V	-	10	pF

Note: This parameter is sampled and not 100% tested.

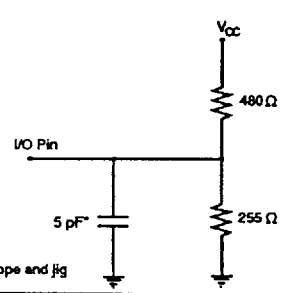
AC Test Conditions

* Input pulse levels: 0V to 3.0V
* Input rise and fall times: 3ns
* Input and Output timing reference levels: 1.5V
* Output load: see diagram
* V_{CC}=5V±10%

Output Load A



Output Load B

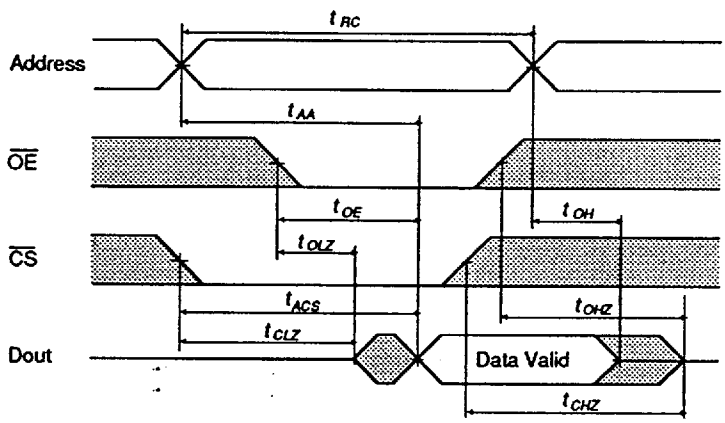


Electrical Characteristics & Recommended AC Operating Conditions

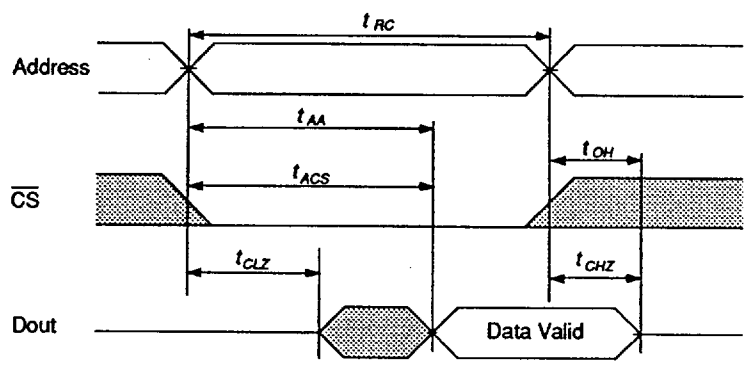
Read Cycle

Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Unit	Notes
Read Cycle Time	t_{RC}	45	-	55	-	70	-	ns	
Address Access Time	t_{AA}	-	45	-	55	-	70	ns	
Chip Select Access Time	t_{ACS}	-	45	-	55	-	70	ns	
Output Enable to Output Valid	t_{OE}	-	20	-	25	-	30	ns	
Output Hold from Address Change	t_{OH}	3	-	3	-	3	-	ns	
Chip Selection to Output in Low Z	t_{CLZ}	3	-	3	-	3	-	ns	5,6
Output Enable to Output in Low Z	t_{OLZ}	0	-	0	-	0	-	ns	5,6
Chip Deselection to Output in High Z	t_{CHZ}	0	20	-	25	-	30	ns	5,6
Output Disable to Output in High Z	t_{OHZ}	0	20	-	25	-	30	ns	5,6

Read Cycle 1 Timing Waveform[1,5] ($\overline{OE}$ Controlled)



Read Cycle 2 Timing Waveform [1,2,3,4,5] ($\overline{CS}$ Controlled)

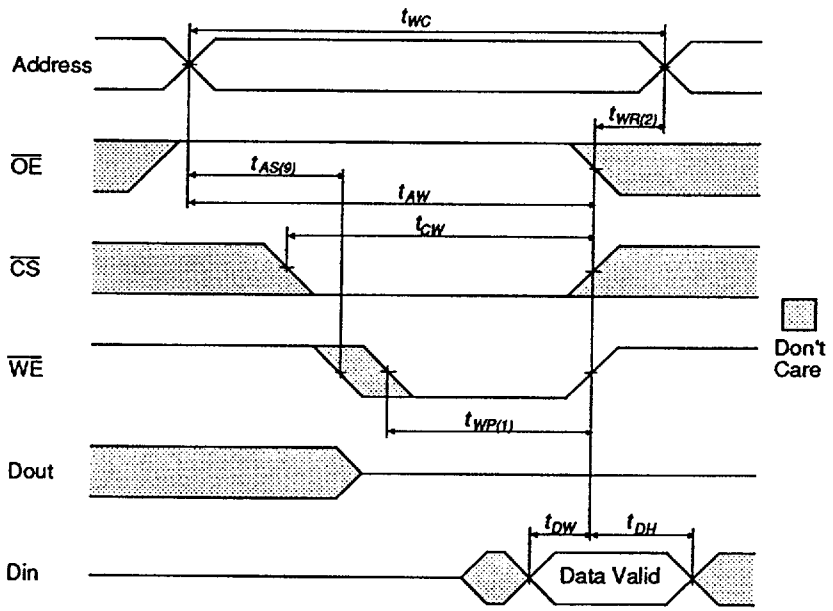


Notes: (1) $\overline{WE}$ is V_{IH} (High) for Read Cycle.
(2) Device may be continually selected, ($\overline{CS}$=V_{IL}).
(3) $\overline{OE}$ is V_{IL} (Low) for Read Cycle.
(4) If address is valid prior to or coincident with $\overline{CS}$ access is controlled by $\overline{CS}$, otherwise address transition controls timing.
(5) t_{CHZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referenced to output voltage levels. These parameters are sampled and not 100% tested.
(6) Transition is measured ±200mV from steady voltage with load B shown on page 2.

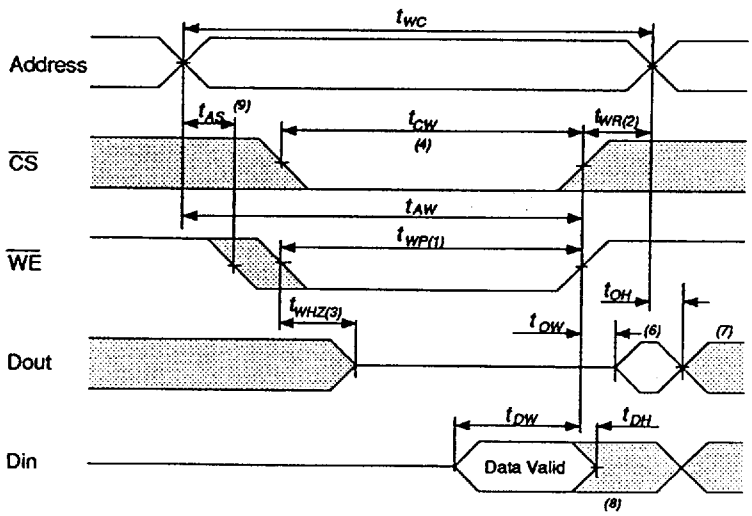
Write Cycle

Parameter	Symbol	-45 min	-45 max	-55 min	-55 max	-70 min	-70 max	Unit	Notes
Write Cycle Time	t_{WC}	45	-	55	-	70	-	ns	
Chip Selection to End of Write	t_{CW}	40	-	40	-	45	-	ns	
Address Valid to End of Write	t_{AW}	40	-	40	-	45	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Write Pulse Width	t_{WP}	25	-	25	-	25	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	0	-	ns	
Write to Output in High Z	t_{WHZ}	0	20	0	20	0	20	ns	9,10
Data to Write Time Overlap	t_{DW}	20	-	20	-	20	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
Output Active from End of Write	t_{OW}	3	-	3	-	3	-	ns	

Write Cycle 1 Timing Waveform ($\overline{OE}$ Clock)



Write Cycle 2 Timing Waveform ($\overline{OE}$ Low Fixed)



AC Write Characteristics Notes

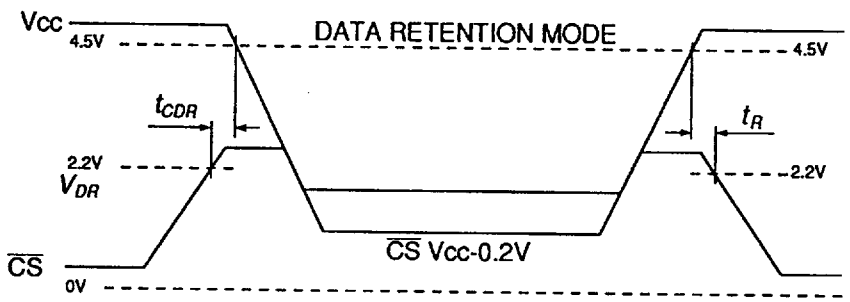
(1) A write occurs during the overlap (t_{WP}) of a low $\overline{CS}$ and a low $\overline{WE}$.
(2) t_{WR} is measured from the earlier of $\overline{CS}$ or $\overline{WE}$ going high to the end of write cycle.
(3) During this period, I/O pins are in the output state. Input signals out of phase must not be applied.
(4) If the $\overline{CS}$ low transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ low transition, outputs remain in a high impedance state.
(5) $\overline{OE}$ is continuously low. ($\overline{OE}$=V_{IL})
(6) Dout is in the same phase as written data of this write cycle.
(7) Dout is the read data of next address.
(8) If $\overline{CS}$ is low during this period, I/O pins are in the output state. Input signals out of phase must not be applied to I/O pins.
(9) $\overline{WE}$ must be high during all address transitions except when the device is deselected with $\overline{CS}$.
(10) Transition is measured ±200mV from steady voltage with load B. This parameter is sampled and is not 100% tested.

Low V_{CC} Data Retention Characteristics - L & P Version Only

Parameter	*Symbol*	*Test Condition*	*min*	*typ*	*max*	*Unit*
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC}$-0.2V	2.0	-	-	V
Data Retention Current		$\overline{CS} \geq V_{CC}$-0.2V, $V_{IN} \geq V_{CC}$-0.2V or ≤ 0.2V				
L-Version	I_{CCDR1}	V_{CC} = 3V	-	-	800	µA
P-Version	I_{CCDR2}	V_{CC} = 3V	-	1	200	µA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R	See Retention Waveform	t_{RC} (1)	-	-	ns

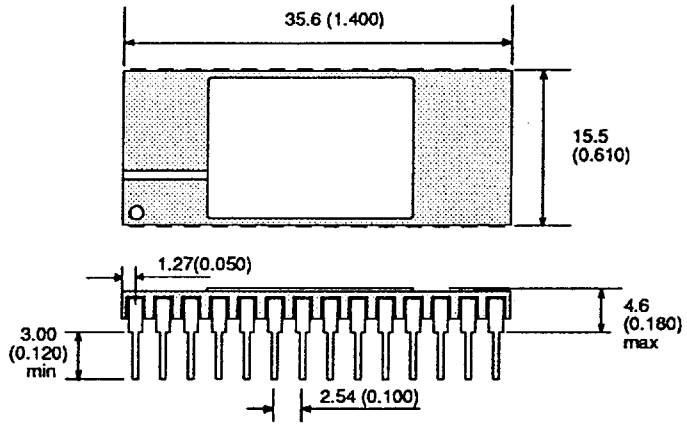
Notes (1) t_{RC}=Read Cycle Time

Data Retention Waveform

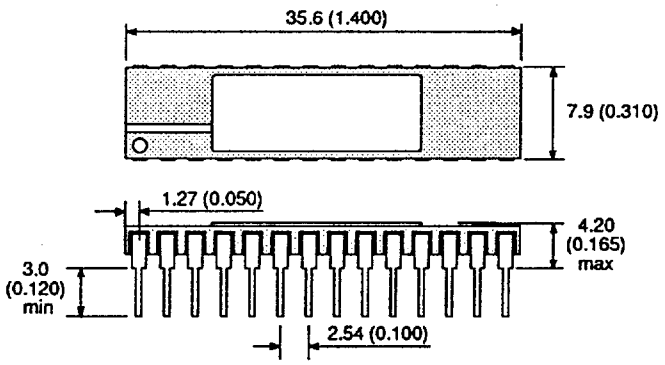


Package Details Dimensions in mm (inches). Tolerance on all dimensions ± 0.254 (0.01)

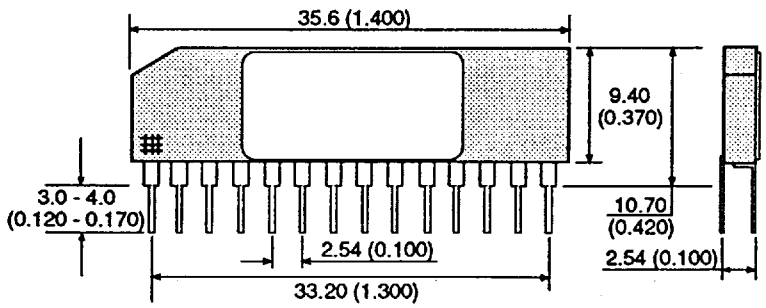
28 pin 0.6" Dual-In-Line (DIL) - 'S' Package



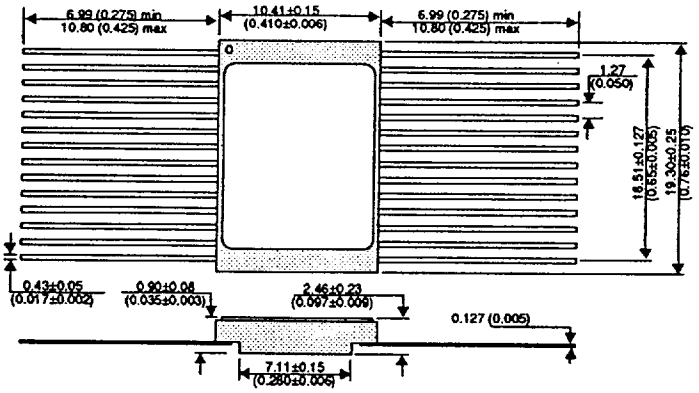
28 pin 0.3" Dual-In-Line (DIL) - 'T' Package



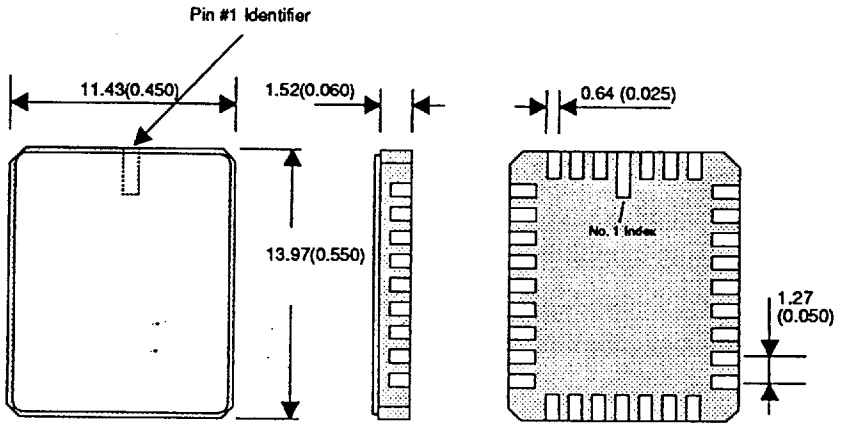
28 pin 0.1" Vertical-In-Line (VIL) - 'V' Package



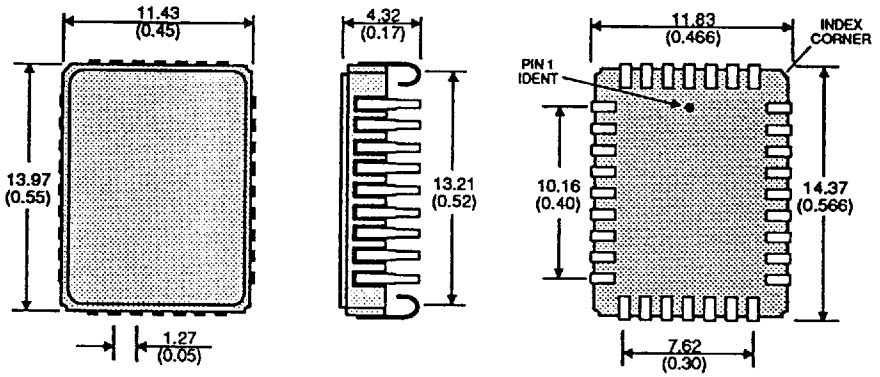
28 pin Cereamic Flatpack - 'G' Package



32 pad Leadless Chip Carrier (LCC) - 'W' Package

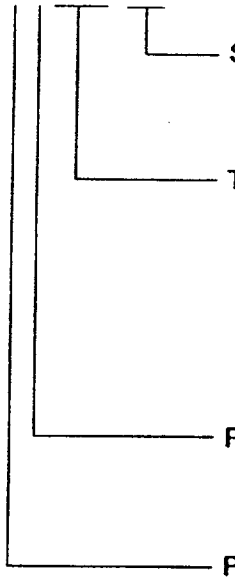


32 pad 'J' Leaded Chi p Carrier (JLCC) - 'J' Package



Ordering Information

MSM832SPMB-45



Speed	45	= 45 ns
	55	= 55 ns
	70	= 70 ns
Temp. range/screening	Blank	= Commercial
	I	= Industrial
	M	= Military
	MB	= Processed to MIL-STD-883 Method 5004, non-compliant
	MC	= MIL-STD-883, compliant (under development)
Power	Blank	= Standard Power
	L	= Low Power
	P	= Super Low Power
Package	G	= 28 pin Ceramic Flatpack
	S	= 28 pin 0.6" DIL
	T	= 28 pin 0.3" DIL
	V	= 28 pin 0.1" VIL
	W	= 32 pad LCC
	J	= 32 JLCC

Note: For more information regarding screening levels, contact Mosaic Semiconductor Inc. for a 'Screening Level Applications Note.'

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Mosaic Semiconductor Inc.
7420 Carroll Road
San Diego, CA 92121
Tel: (619) 271 4565
FAX: (619) 271 6058