F10186 • F10586

HEX D FLIP-FLOP WITH RESET

F10K VOLTAGE COMPENSATED ECL

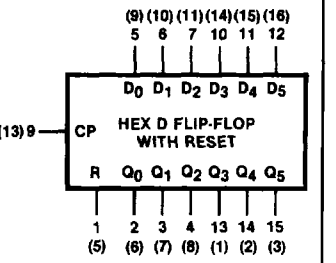
DESCRIPTION — The F10186 and F10586 contain six high-speed master/slave D-type flip-flops which have a common clock. Data is entered into the master when the Clock is LOW. Data transfer takes place on the positive-going clock transition. A change in the information present at the Data input will not affect the output information. The common reset functions only when the Clock is LOW.

- **VOLTAGE COMPENSATED—NOISE MARGIN INSENSITIVE TO POWER SUPPLY VARIATIONS AND TRANSIENTS.**
- **OPEN EMITTER-FOLLOWER OUTPUTS.**
- **50 Ω DRIVE AND WIRED-OR CAPABILITY.**
- **INTERNAL 50 kΩ INPUT PULL-DOWN RESISTORS.**

PIN NAMES

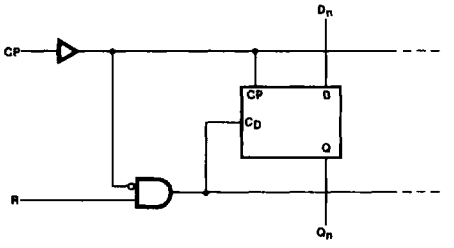
D_n	Data Inputs
CP	Clock
R	Common Reset
Q_n	Outputs

LOGIC SYMBOL



( ) = Flatpak
V_{CC} = Pin 16 (4)
V_{EE} = Pin 8 (12)

LOGIC DIAGRAM (One Flip-flop)

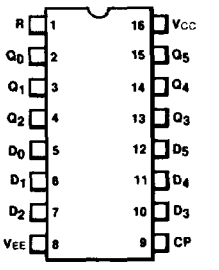


CLOCKED TRUTH TABLE

R	CP	D	Q_{t+1}
L	L	X	Q_t
L	⎍	L	L
L	⎍	H	H
H	L	X	L

X = Don't Care
H = HIGH Voltage Level
L = LOW Voltage Level
t, t + 1 = Time before and after CP positive transition

CONNECTION DIAGRAM
DIP (TOP VIEW)



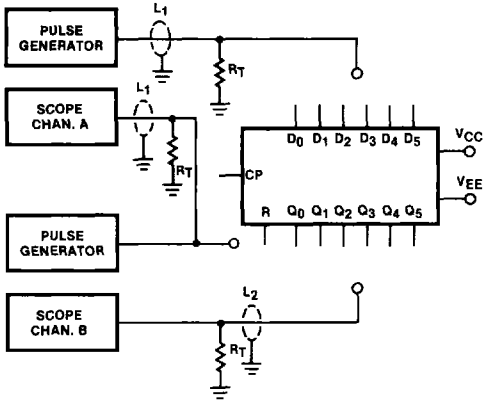
DC CHARACTERISTICS: $V_{EE} = -5.2$ V, $V_{CC} = GND$

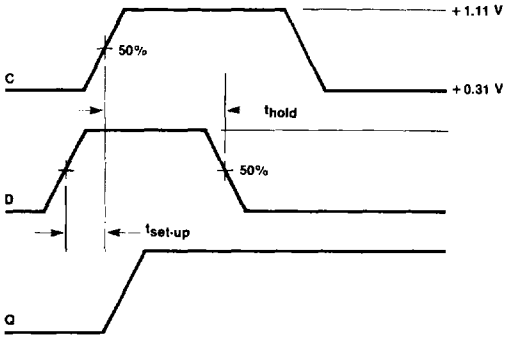
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	T_A	CONDITIONS
		B	TYP	A			
I_{IH}	Input Current HIGH				μA	25°C	$V_{IN} = V_{IHA}$
	Data			220			
	Clock			310			
	Reset			575			
I_{EE}	Supply Current	−110	−88		mA	25°C	Inputs and Outputs Open

AC CHARACTERISTICS: $V_{EE} = -5.2$ V, $T_A = 25°C$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
	Propagation Delay,				ns	
t_{PLH},	Reset to Q	1.5	2.5	4.0		
t_{PHL}	Clock to Q	1.5	3.5	4.5		
t_{TLH},	Transition Time	1.5	1.8	3.5	ns	See Figure 1
t_{THL}	20% to 80%, 80% to 20%					
t_s	Set-Up Time	2.5			ns	
t_h	Hold Time	1.5			ns	

AC TEST CIRCUIT AND WAVEFORMS





L_1 and L_2 = equal length 50 Ω impedance lines
R_T = 50 Ω termination of scope
C_L = Jig and stray capacitance <5.0 pF
Decoupling 0.1 μF from gnd to V_{EE} and V_{CC}
V_{CC} = 2.0 V
V_{EE} = −3.2 V

$t_{set\text{-}up}$ is the minimum time before the transition of the clock pulse (C) that information must be present at the data input (D).

t_{hold} is the minimum time after the positive transition of the clock pulse (C) that information must remain unchanged at the data input (D). Note that t_{hold} may be a negative number.

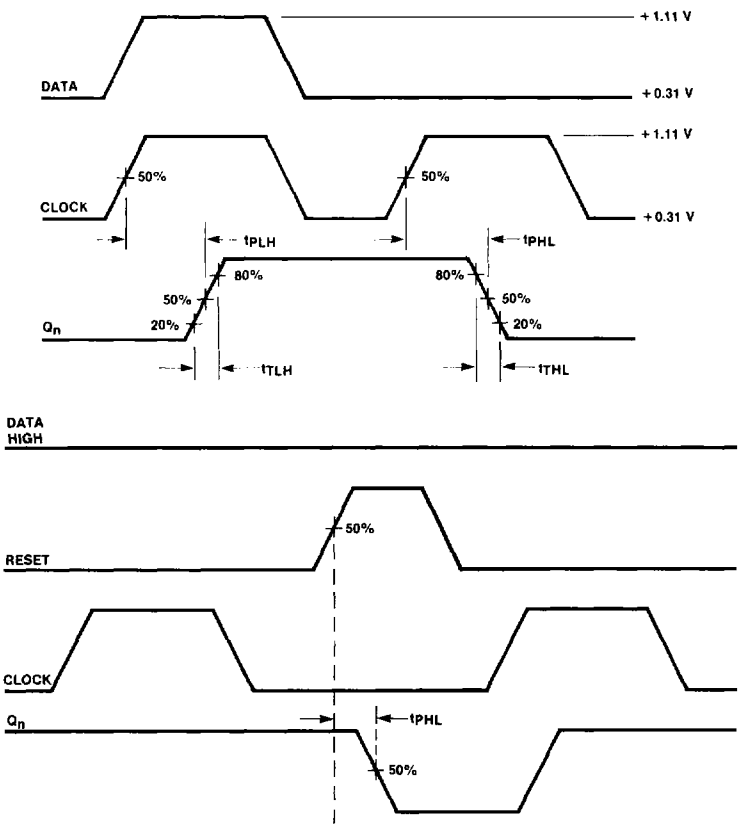


Fig. 1