54F/74F160A • 54F/74F162A

Synchronous Presettable BCD Decade Counter

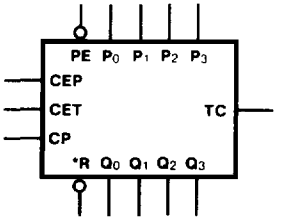
Description

The 'F160A and 'F162A are high-speed synchronous decade counters operating in the BCD (8421) sequence. They are synchronously presettable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The 'F160A has an asynchronous Master Reset input that overrides all other inputs and forces the outputs LOW. The 'F162A has a Synchronous Reset input that overrides counting and parallel loading and allows all outputs to be simultaneously reset on the rising edge of the clock. The 'F160A and 'F162A are high speed versions of the 'F160 and 'F162.

- **Synchronous Counting and Loading**
- **High-Speed Synchronous Expansion**
- **Typical Count Rate of 120 MHz**

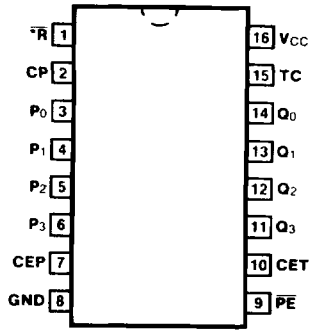
Ordering Code: See Section 5

Logic Symbol

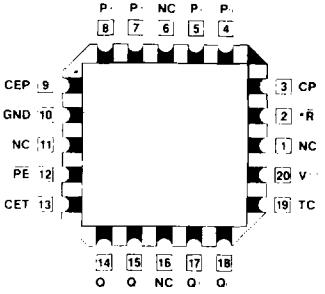


* $\overline{MR}$ for 'F160A
* $\overline{SR}$ for 'F162A

Connection Diagrams



Pin Assignment for DIP and SOIC



Pin Assignment for LCC and PCC

* $\overline{MR}$ for 'F160A
* $\overline{SR}$ for 'F162A

Input Loading/Fan-Out: See Section 3 for U.L. definitions

Pin Names	Description	54F/74F(U.L.) HIGH/LOW
CEP	Count Enable Parallel Input	0.5/0.375
CET	Count Enable Trickle Input	0.5/0.75
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.375
$\overline{MR}$ ('F160A)	Asynchronous Master Reset Input (Active LOW)	0.5/0.375
$\overline{SR}$ ('F162A)	Synchronous Reset Input (Active LOW)	0.5/0.75
P_0-P_3	Parallel Data Inputs	0.5/0.375
$\overline{PE}$	Parallel Enable Input (Active LOW)	0.5/0.75
Q_0-Q_3	Flip-Flop Outputs	25/12.5
TC	Terminal Count Output	25/12.5

Functional Description

The 'F160A and 'F162A count modulo-10 in the BCD (8421) sequence. From state 9 (HLLH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the ('F160A) occur as a result of, and synchronous with, the LOW-to-HIGH transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset ('F160A), synchronous reset ('F162A), parallel load, count-up and hold. Five control inputs—Master Reset ($\overline{MR}$, 'F160A), Synchronous Reset ($\overline{SR}$, 'F162A), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET)—determine the mode of operation, as shown in the Mode Select Table. A LOW signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs LOW. A LOW signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go LOW on the next rising edge of CP. A LOW signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ ('F160A) or $\overline{SR}$ ('F162A) HIGH, CEP and CET permit counting when both are HIGH. Conversely, a LOW signal on either CEP or CET inhibits counting.

The 'F160A and 'F162A use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed.

The Terminal Count (TC) output is HIGH when CET is HIGH and counter is in state 9. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. Please refer to the 'F568 data sheet. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers. In the 'F160A and 'F162A decade counters, the TC output is fully decoded and can only be HIGH in state 9. If a decade counter is preset to an illegal state, or assumes an illegal state when power is applied, it will return to the normal sequence within two counts, as shown in the State Diagram.

Logic Equations: Count Enable = $CEP \bullet CET \bullet \overline{PE}$

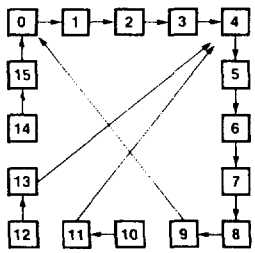
$TC = Q_0 \bullet \overline{Q}_1 \bullet \overline{Q}_2 \bullet Q_3 \bullet CET$

Mode Select Table

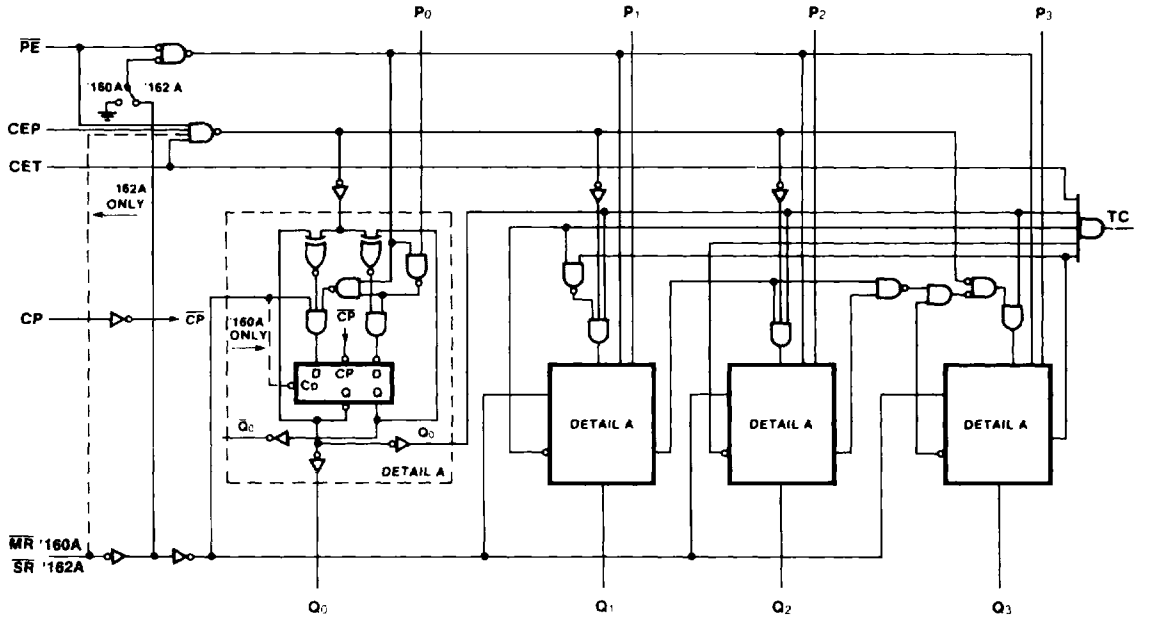
*$\overline{SR}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge (⌐)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No Change (Hold)
H	H	X	L	No Change (Hold)

*For 'F162A only
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

State Diagram



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	54F/74F			Units	Conditions
		Min	Typ	Max		
I_{CC}	Power Supply Current		37	55	mA	V_{CC} = Max

AC Characteristics: See Section 3 for waveforms and load configurations

Symbol	Parameter	54F/74F $T_A = +25°C$, $V_{CC} = +5.0\ V$, $C_L = 50\ pF$			54F T_A, V_{CC} = Mil, $C_L = 50\ pF$		74F T_A, V_{CC} = Com, $C_L = 50\ pF$		Units	Fig. No.
		Min	Typ	Max	Min	Max	Min	Max		
f_{max}	Maximum Count Frequency	100	120		75		90		MHz	3-1
t_{PLH} t_{PHL}	Propagation Delay, Count CP to Q_n ($\overline{PE}$ Input HIGH)	3.5 3.5	5.5 7.5	7.5 10.0	3.5 3.5	9.0 11.5	3.5 3.5	8.5 11.0	ns	3-1, 3-7
t_{PLH} t_{PHL}	Propagation Delay, Load CP to Q_n ($\overline{PE}$ Input LOW)	4.0 4.0	6.0 6.0	8.5 8.5	4.0 4.0	10.0 10.0	4.0 4.0	9.5 9.5		
t_{PLH} t_{PHL}	Propagation Delay CP to TC	5.0 5.0	10.0 10.0	14.0 14.0	5.0 5.0	16.5 15.5	5.0 5.0	15.0 15.0	ns	3-1 3-7
t_{PLH} t_{PHL}	Propagation Delay CET to TC	2.5 2.5	4.5 4.5	7.5 7.5	2.5 2.5	9.0 9.0	2.5 2.5	8.5 8.5	ns	3-1 3-4
t_{PHL}	Propagation Delay $\overline{MR}$ to Q_n ('F160A)	5.5	9.0	12.0	5.5	14.0	5.5	13.0	ns	3-1 3-11
t_{PHL}	Propagation Delay $\overline{MR}$ to TC ('F160A)	4.5	8.0	10.5	4.5	12.5	4.5	11.5	ns	3-1 3-11

AC Operating Requirements: See Section 3 for waveforms

Symbol	Parameter	54F/74F	54F	74F	Units	Fig. No.
		$T_A = +25°C$ $V_{CC} = +5.0\ V$	T_A, V_{CC} = Mil	T_A, V_{CC} = Com		
		Min Typ Max	Min Max	Min Max		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW P_n to CP	5.0 5.0	5.5 5.5	5.0 5.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW P_n to CP	2.0 2.0	2.5 2.5	2.0 2.0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	11.0 8.5	13.5 10.5	11.5 9.5	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW $\overline{PE}$ or $\overline{SR}$ to CP	2.0 0	2.0 0	2.0 0		
$t_s(H)$ $t_s(L)$	Setup Time, HIGH or LOW CEP or CET to CP	11.0 5.0	13.0 6.0	11.5 5.0	ns	3-5
$t_h(H)$ $t_h(L)$	Hold Time, HIGH or LOW CEP or CET to CP	0 0	0 0	0 0		
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Load) HIGH or LOW	5.0 5.0	5.0 5.0	5.0 5.0	ns	3-7
$t_w(H)$ $t_w(L)$	Clock Pulse Width (Count) HIGH or LOW	4.0 6.0	5.0 8.0	4.0 7.0	ns	3-7
$t_w(L)$	$\overline{MR}$ Pulse Width, LOW ('F160A)	5.0	5.0	5.0	ns	3-11
t_{rec}	Recovery Time $\overline{MR}$ to CP ('F160A)	6.0	6.0	6.0		