

# CD74HCU04

## High Speed CMOS Logic Hex Inverter

### Features

- **Typical Propagation Delay: 6ns at  $V_{CC} = 5V$ ,  $C_L = 15pF$ ,  $T_A = 25^\circ C$ , Fastest Part in QMOS Line**
- **Wide Operating Temperature Range . . .  $-55^\circ C$  to  $125^\circ C$**
- **Balanced Propagation Delay and Transition Times**
- **Significant Power Reduction Compared to LSTTL Logic ICs**
- **HCU Types**
  - 2V to 6V Operation
  - High Noise Immunity:  $N_{IL} = 20\%$ ,  $N_{IH} = 30\%$  of  $V_{CC}$  at  $V_{CC} = 5V$
- **CMOS Input Compatibility,  $I_I \leq 1\mu A$  at  $V_{OL}$ ,  $V_{OH}$**

### Description

The Harris CD74HCU04 unbuffered hex inverter utilizes silicon-gate CMOS technology to achieve operation speeds similar to LSTTL gates with the low power consumption of standard CMOS integrated circuits. These devices are especially useful in crystal oscillator and analog applications. Figures 10 and 11 are supplied as design information for the above applications.

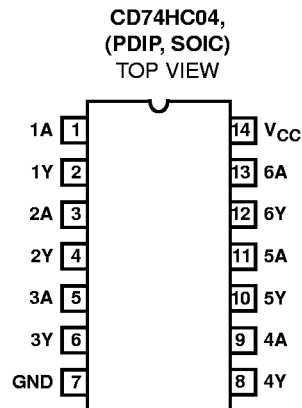
### Ordering Information

PART NUMBER	TEMP. RANGE ( $^\circ C$ )	PACKAGE	PKG. NO.
CD74HCU04E	-55 to 125	14 Ld PDIP	E14.3
CD74HCU04M	-55 to 125	14 Ld SOIC	M14.15

#### NOTES:

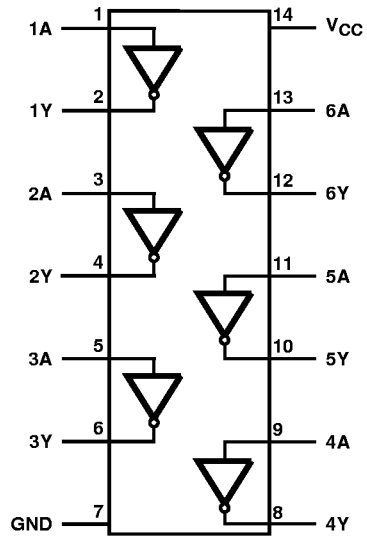
1. When ordering, use the entire part number. Add the suffix 96 to obtain the variant in the tape and reel.
2. Wafer or die for this part number is available which meets all electrical specifications. Please contact your local sales office or Harris customer service for ordering information.

### Pinout



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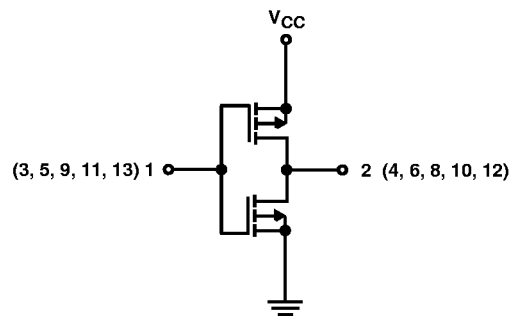
## Functional Diagram



## Logic Symbol



## Schematic Diagram



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## Absolute Maximum Ratings

DC Supply Voltage, $V_{CC}$	
Voltages Referenced to Ground	-0.5V to +7V
DC Input Diode Current, $I_{IK}$	
For $V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$	$\pm 20mA$
DC Output Diode Current, $I_{OK}$	
For $V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$	$\pm 20mA$
DC Drain Current, per Output, $I_O$	
For $V_O > -0.5V$ or $V_O < V_{CC} + 0.5V$	$\pm 25mA$
DC $V_{CC}$ or Ground Current, $I_{CC}$	$\pm 50mA$

## Thermal Information

Thermal Resistance (Typical, Note 3)	$\theta_{JA}$ ( $^{\circ}C/W$ )
PDIP Package	100
SOIC Package	180
Maximum Junction Temperature (Hermetic Package or Die)	175 $^{\circ}C$
Maximum Junction Temperature (Plastic Package)	150 $^{\circ}C$
Maximum Storage Temperature Range	-65 $^{\circ}C$ to 150 $^{\circ}C$
Maximum Lead Temperature (Soldering 10s)	300 $^{\circ}C$
(SOIC - Lead Tips Only)	

## Operating Conditions

Temperature Range $T_A$	-55 $^{\circ}C$ to 125 $^{\circ}C$
Supply Voltage Range, $V_{CC}$	.2V to 6V
DC Input or Output Voltage, $V_I$ , $V_O$	0V to $V_{CC}$
Input Rise and Fall Time	
2V	1000ns (Max)
4.5V	500ns (Max)
6V	400ns (Max)

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

### NOTE:

- $\theta_{JA}$  is measured with the component mounted on an evaluation PC board in free air.

## DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		$V_{CC}$ (V)	25 $^{\circ}C$		-40 $^{\circ}C$ TO +85 $^{\circ}C$		-55 $^{\circ}C$ TO 125 $^{\circ}C$		UNITS
		$V_I$ (V)	$I_O$ (mA)		MIN	MAX	MIN	MAX	MIN	MAX	
High Level Input Voltage	$V_{IH}$	-	-	2	1.7	-	1.7	-	1.7	-	V
				4.5	3.6	-	3.6	-	3.6	-	V
				6	4.8	-	4.8	-	4.8	-	V
Low Level Input Voltage	$V_{IL}$	-	-	2	-	0.3	-	0.3	-	0.3	V
				4.5	-	0.8	-	0.8	-	0.8	V
				6	-	1.1	-	1.1	-	1.1	V
High Level Output Voltage CMOS Loads	$V_{OH}$	$V_{IH}$ or $V_{IL}$	-0.02	2	1.8	-	1.8	-	1.8	-	V
			-0.02	4.5	4	-	4	-	4	-	V
			-0.02	6	5.5	-	5.5	-	5.5	-	V
High Level Output Voltage TTL Loads	$V_{OH}$	$V_{CC}$ or GND	-4	4.5	3.98	-	3.84	-	3.7	-	V
			-5.2	6	5.48	-	5.34	-	5.2	-	V
Low Level Output Voltage CMOS Loads	$V_{OL}$	$V_{IH}$ or $V_{IL}$	0.02	2	-	0.2	-	0.2	-	0.2	V
			0.02	4.5	-	0.5	-	0.5	-	0.5	V
			0.02	6	-	0.5	-	0.5	-	0.5	V
Low Level Output Voltage TTL Loads	$V_{OL}$	$V_{CC}$ or GND	4	4.5	-	0.26	-	0.33	-	0.4	V
			5.2	6	-	0.26	-	0.33	-	0.4	V
Input Leakage Current	$I_I$	$V_{CC}$ or GND	-	6	-	$\pm 0.1$	-	$\pm 1$	-	$\pm 1$	$\mu A$
Quiescent Device Current	$I_{CC}$	$V_{CC}$ or GND	0	6	-	2	-	20	-	40	$\mu A$

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## Switching Specifications Input $t_r, t_f = 6\text{ns}$

PARAMETER	SYMBOL	TEST CONDITIONS	$V_{CC}$ (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Propagation Delay, Input to Output Y (Figure 1)	$t_{PLH}, t_{PHL}$	$C_L = 50\text{pF}$	2	-	-	70	-	90	-	105	ns
		$C_L = 50\text{pF}$	4.5	-	-	14	-	18	-	21	ns
		$C_L = 15\text{pF}$	5	-	5	-	-	-	-	-	ns
		$C_L = 50\text{pF}$	6	-	-	12	-	15	-	18	ns
Transition Times (Figure 1)	$t_{TLH}, t_{THL}$	$C_L = 50\text{pF}$	2	-	-	75	-	95	18	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
Input Capacitance	$C_I$	-	See Figure 3							pF	
Power Dissipation Capacitance (Notes 4, 5)	$C_{PD}$	-	5	-	14	-	-	-	-	-	pF

**NOTES:**

4.  $C_{PD}$  is used to determine the dynamic power consumption, per inverter.
5.  $P_D = V_{CC}^2 f_i (C_{PD} + C_L)$  where  $f_i$  = input frequency,  $C_L$  = output load capacitance,  $V_{CC}$  = supply voltage.

## Test Circuits and Waveforms

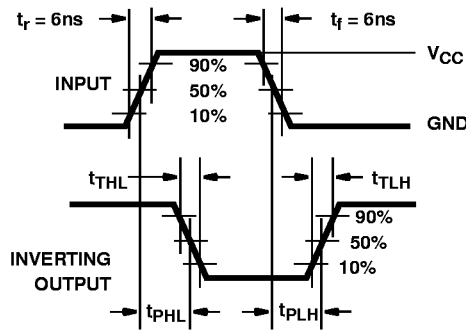


FIGURE 1. HC AND HCU TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

## Typical Performance Curves

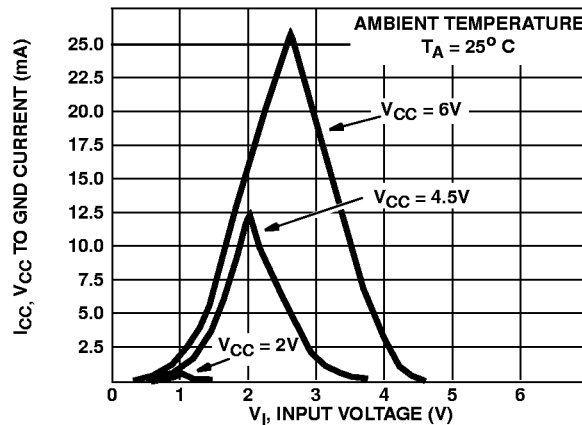


FIGURE 2. TYPICAL INVERTER SUPPLY CURRENT AS FUNCTION OF INPUT VOLTAGE

Typical Performance Curves (Continued)

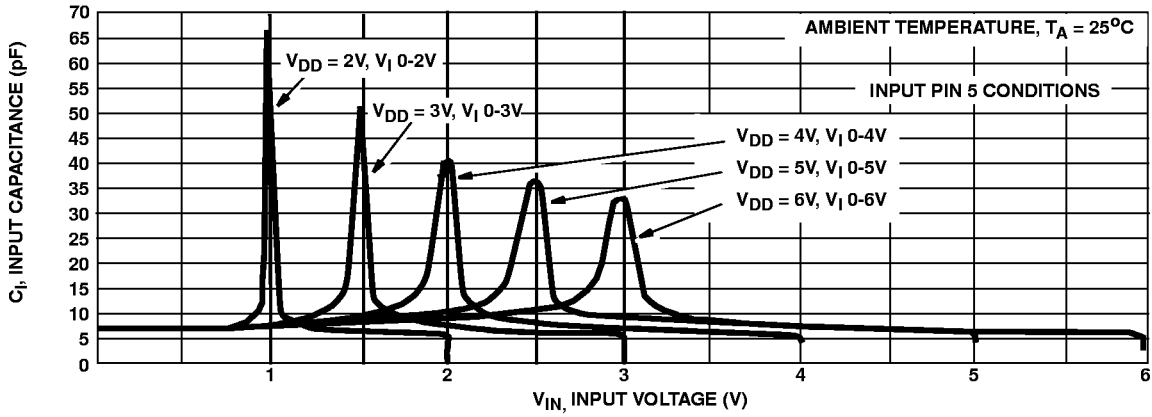


FIGURE 3. INPUT CAPACITANCE AS A FUNCTION OF INPUT VOLTAGE