REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device type 02. Add I_{OH} and I_{OL} tests. Add Schmitt trigger threshold tests for device type 02. Change table IB. Editorial changes throughout. - JAK	96-11-19	Monica L. Poelking
B	Changes in accordance with NOR 5962-R259-97. - CFS	97-04-22	Monica L. Poelking
C	Add die appendix. Update boilerplate. - CFS	00-07-12	Monica L. Poelking
D	Add limit for linear energy threshold (LET) with no latch-up in section 1.5. Update the boilerplate to the requirements of MIL-PRF-38535. Editorial changes throughout. - TVN	07-04-25	Thomas M. Hess
E	Update boilerplate paragraphs and radiation paragraphs 4.4.4.1 – 4.4.4.4 to the current MIL-PRF-38535 requirements. Delete class M requirement throughout. - LTG	14-01-28	Thomas M. Hess
F	Update quiescent supply current (I_{DDQ}) limit to table IA. - MAA	17-10-30	Thomas M. Hess

REV																				
SHEET																				
REV	F	F	F	F	F	F	F	F	F	F	F									
SHEET	15	16	17	18	19	20	21	22	23	24	25									

REV STATUS	REV	F	F	F	F	F	F	F	F	F	F	F	F	F
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

CHECKED BY
Thanh V. Nguyen

APPROVED BY
Monica L. Poelking

DRAWING APPROVAL DATE
96-05-30

REVISION LEVEL
F

MICROCIRCUIT, DIGITAL, RADIATION HARDENED, ADVANCED CMOS, OCTAL BUS TRANSCEIVER WITH THREE-STATE OUTPUTS, MONOLITHIC SILICON

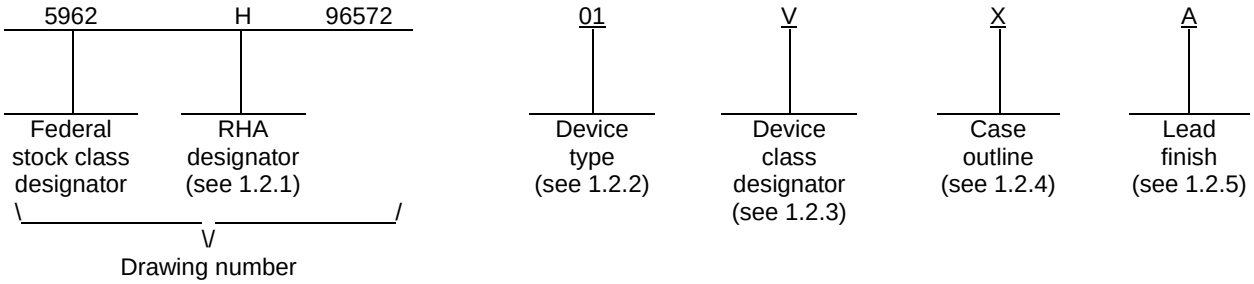
SIZE	CAGE CODE	
A	**67268**	**5962-96572**

SHEET 1 OF 25

1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device class Q) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS245	Radiation hardened, octal bus transceiver with three-state outputs
02	54ACS245S	Radiation hardened, Schmitt octal bus transceiver with three-state outputs

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
R	GDIP1-T20 or CDIP2-T20	20	Dual-in-line
X	CDFP4-F20	20	Flat pack

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V.

1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range (V_{DD})	-0.3 V dc to +7.0 V dc
DC input voltage range (V_{IN})	-0.3 V dc to V_{DD} + 0.3 V dc
DC output voltage range (V_{OUT})	-0.3 V dc to V_{DD} + 0.3 V dc
DC input current, any one input (I_{IN})	±10 mA
Latch-up immunity current (I_{LU})	±150 mA
Storage temperature range (T_{STG})	-65°C to +150°C
Lead temperature (soldering, 5 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Junction temperature (T_J)	+175°C
Maximum power dissipation (P_D)	1.0 W

1.4 Recommended operating conditions. 2/ 3/

Supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Input voltage range (V_{IN})	0.0 V dc to V_{DD}
Output voltage range (V_{OUT})	0.0 V dc to V_{DD}
Maximum input rise or fall time at V_{DD} = 4.5 V (t_r, t_f)	1 ns/V 4/
Case operating temperature range (T_C)	-55°C to +125°C

1.5 Radiation features. 5/

Maximum total dose available (dose rate = 50 – 300 Rad (Si)/s)	1M Rad (Si)
Single event phenomenon (SEP):	
Effective linear energy transfer (LET), no upsets (see 4.4.4.4)	≤ 80 MeV/(mg/cm^2) 6/
Effective linear energy transfer (LET), no latch-up (see 4.4.4.4)	≤ 120 MeV/(mg/cm^2) 6/
Dose rate upset (20 ns pulse)	1 x 10^9 Rad (Si)/s
Latch-up	None
Dose rate survivability	1 x 10^{12} Rad (Si)/s

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ Unless otherwise noted, all voltages are referenced to V_{SS}.
3/ The limits for the parameters specified herein shall apply over the full specified V_{DD} range and case temperature range of -55°C to +125°C unless otherwise noted.
4/ Derate system propagation delays by difference in rise time to switch point for t_r or t_f > 1 ns/V.
5/ Radiation testing is performed on the standard evaluation circuit.
6/ Limits obtained during technology characterization/qualification, guaranteed by design or process, but not production tested unless specified by the customer through the purchase order or contract.

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARDS

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-1835 - Interface Standard Electronic Component Case Outlines.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

2.2 Non-Government publications. The following document(s) form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents cited in the solicitation or contract.

ASTM INTERNATIONAL (ASTM)

ASTM F1192 - Standard Guide for the Measurement of Single Event Phenomena (SEP) Induced by Heavy Ion Irradiation of Semiconductor Devices.

(Copies of this document is available online at http://www.astm.org/ or from ASTM International, 100 Barr Harbor Drive, P. O. Box C700, West Conshohocken, PA 19428-2959).

2.3 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 as specified herein, or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

3.1.1 Microcircuit die. For the requirements of microcircuit die, see appendix A to this document.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V.

3.2.1 Case outlines. The case outlines shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table. The truth table shall be as specified on figure 2.

3.2.4 Logic diagram. The logic diagram shall be as specified on figure 3.

3.2.5 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 4.

3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing and acquiring activity upon request.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table IA and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table IIA. The electrical tests for each subgroup are defined in table IA.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). The certificate of compliance submitted to DLA Land and Maritime-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuits delivered to this drawing.

TABLE IA. Electrical performance characteristics.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/		Unit
						Min	Max	
High level input voltage	V_{IH}		01	4.5 V	1, 2, 3	3.15		V
		M, D, P, L, R, F, G, H 3/	01		1	3.15		
			01	5.5 V	1, 2, 3	3.85		
		M, D, P, L, R, F, G, H 3/	01		1	3.85		
Low level input voltage	V_{IL}		01	4.5 V	1, 2, 3		1.35	V
		M, D, P, L, R, F, G, H 3/	01		1		1.35	
			01	5.5 V	1, 2, 3		1.65	
		M, D, P, L, R, F, G, H 3/	01		1		1.65	
Schmitt trigger, positive-going threshold	V_{T+}		02	4.5 V	1, 2, 3		3.15	V
		M, D, P, L, R, F, G, H 3/	02		1		3.15	
			02	5.5 V	1, 2, 3		3.85	
		M, D, P, L, R, F, G, H 3/	02		1		3.85	
Schmitt trigger, negative-going threshold	V_{T-}		02	4.5 V	1, 2, 3	1.35		V
		M, D, P, L, R, F, G, H 3/	02		1	1.35		
			02	5.5 V	1, 2, 3	1.65		
		M, D, P, L, R, F, G, H 3/	02		1	1.65		
Schmitt trigger, range of hysteresis	V_H		02	4.5 V	1, 2, 3	0.6	1.5	V
		M, D, P, L, R, F, G, H 3/	02		1	0.6	1.5	
High level output voltage	V_{OH}	For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} $I_{OH} = -100\ \mu A$	All	4.5 V	1, 2, 3	4.25		V
		M, D, P, L, R, F, G, H 3/	All		1	4.25		
Low level output voltage	V_{OL}	For all inputs affecting output under test, $V_{IN} = V_{DD}$ or V_{SS} $I_{OL} = +100\ \mu A$	All	4.5 V	1, 2, 3		0.25	V
		M, D, P, L, R, F, G, H 3/	All		1		0.25	
Input current high	I_{IH}	For input under test, $V_{IN} = V_{DD}$ For all other inputs, $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		+1.0	µA
		M, D, P, L, R, F, G, H 3/	All		1		+1.0	
Input current low	I_{IL}	For input under test, $V_{IN} = V_{SS}$ For all other inputs, $V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		-1.0	µA
		M, D, P, L, R, F, G, H 3/	All		1		-1.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Output current (source)	I_{OH} 4/	For output under test, $V_{OUT} = V_{DD} - 0.4$ V $V_{IN} = V_{DD}$ or V_{SS}	All	4.5 V and 5.5 V	1, 2, 3	-12.0		mA
		M, D, P, L, R, F, G, H 3/	All		1	-12.0		
Output current (sink)	I_{OL} 4/	For output under test, $V_{OUT} = 0.4$ V $V_{IN} = V_{DD}$ or V_{SS}	All	4.5 V and 5.5 V	1, 2, 3	12.0		mA
		M, D, P, L, R, F, G, H 3/	All		1	12.0		
Quiescent supply current	I_{DDQ}	$V_{IN} = V_{DD}$ or V_{SS}	All	5.5 V	1, 2, 3		10.0	µA
		Max rated RHA 3/	All		1		50.0	
Short circuit output current	I_{OS} 5/ 6/	$V_{OUT} = V_{DD}$ and V_{SS}	All	5.5 V	1, 2, 3		±300	mA
Three-state output leakage current, high	I_{OZH}	$\overline{G}$ = 5.5 V For all other inputs, $V_{IN} = V_{DD}$ or V_{SS} $V_{OUT} = V_{DD}$	All	5.5 V	1, 2, 3		+30.0	µA
		M, D, P, L, R, F, G, H 3/	All		1		+30.0	
Three-state output leakage current, low	I_{OZL}	$\overline{G}$ = 5.5 V For all other inputs, $V_{IN} = V_{DD}$ or V_{SS} $V_{OUT} = V_{SS}$	All	5.5 V	1, 2, 3		-30.0	µA
		M, D, P, L, R, F, G, H 3/	All		1		-30.0	
Input capacitance	C_{IN}	f = 1 MHz See 4.4.1c	All	0.0 V	4		15.0	pF
I/O capacitance	$C_{I/O}$	f = 1 MHz See 4.4.1c	All	0.0 V	4		15.0	pF
Switching power dissipation	P_{SW} 7/	C_L = 50 pF, per switching output	All	4.5 V and 5.5 V	4, 5, 6		2.0	mW/ MHz
		M, D, P, L, R, F, G, H 3/	All		4		2.0	
Functional test	8/	$V_{IH} = 0.7\ V_{DD}$, $V_{IL} = 0.3\ V_{DD}$ See 4.4.1b	All	4.5 V and 5.5 V	7, 8	L	H	
		M, D, P, L, R, F, G, H 3/	All		7	L	H	
Propagation delay time, An to Bn or Bn to An	t_{PLH} 9/	C_L = 50 pF minimum See figure 4	01	4.5 V and 5.5 V	9, 10, 11	1.0	11.0	Ns
		M, D, P, L, R, F, G, H 3/	01		9	1.0	11.0	
			02	4.5 V and 5.5 V	9, 10, 11	2.0	15.0	
		M, D, P, L, R, F, G, H 3/	02		9	2.0	15.0	

See footnotes at end of table.

TABLE IA. Electrical performance characteristics - Continued.

Test	Symbol	Test conditions 1/ $-55°C \le T_C \le +125°C$ unless otherwise specified	Device type	V_{DD}	Group A subgroups	Limits 2/		Unit
						Min	Max	
Propagation delay time, An to Bn or Bn to An	t_{PHL} 9/	C_L = 50 pF minimum See figure 4	01	4.5 V and 5.5 V	9, 10, 11	1.0	15.0	Ns
		M, D, P, L, R, F, G, H 3/	01		9	1.0	15.0	
			02	4.5 V and 5.5 V	9, 10, 11	2.0	15.0	
		M, D, P, L, R, F, G, H 3/	02		9	2.0	15.0	
Propagation delay time, output enable, $\overline{G}$ to An or Bn	t_{PZH} 9/	C_L = 50 pF minimum See figure 4	01	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	Ns
		M, D, P, L, R, F, G, H 3/	01		9	2.0	12.0	
			02	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	
		M, D, P, L, R, F, G, H 3/	02		9	2.0	12.0	
	t_{PZL} 9/	C_L = 50 pF minimum See figure 4	01	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	Ns
		M, D, P, L, R, F, G, H 3/	01		9	2.0	12.0	
			02	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	
		M, D, P, L, R, F, G, H 3/	02		9	2.0	12.0	
Propagation delay time, output disable, $\overline{G}$ to An or Bn	t_{PHZ} 9/	C_L = 50 pF minimum See figure 4	01	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	Ns
		M, D, P, L, R, F, G, H 3/	01		9	2.0	12.0	
			02	4.5 V and 5.5 V	9, 10, 11	2.0	15.0	
		M, D, P, L, R, F, G, H 3/	02		9	2.0	15.0	
	t_{PLZ} 9/	C_L = 50 pF minimum See figure 4	01	4.5 V and 5.5 V	9, 10, 11	2.0	12.0	Ns
		M, D, P, L, R, F, G, H 3/	01		9	2.0	12.0	
			02	4.5 V and 5.5 V	9, 10, 11	2.0	15.0	
		M, D, P, L, R, F, G, H 3/	02		9	2.0	15.0	

1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table IA herein. Output terminals not designated shall be high level logic, low level logic, or open, except for the I_{DDQ} test, the output terminals shall be open. When performing the I_{DDQ} test, the current meter shall be placed in the circuit such that all current flows through the meter.

2/ For negative and positive voltage and current values, the sign designates the potential difference in reference to V_{SS} and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

3/ RHA devices supplied to this drawing have been characterized through all levels M, D, P, L, R, F, G, and H of irradiation. However, this device is only tested at the 'H' level. Each device type supplied to this drawing is guaranteed to comply with specification table IA through all RHA levels up to, and including, the maximum RHA level listed in section 1.5 Radiation features. Pre and post irradiation values are identical unless otherwise specified in table IA. When performing post irradiation electrical measurements for any RHA level, T_A=+25°C.

4/ This test is guaranteed based on characterization data but not tested.

5/ This parameter is supplied as design limit but not guaranteed or tested.

6/ No more than one output should be shorted at a time for a maximum duration of one second.

7/ This value is calculated during the design/qualification process and is supplied as a design limit but is not tested. Total power consumption is determined by both idle/standby power consumption (Ps) and "at frequency" power consumption (Pf). To determine standby power consumption, use the formula:

$$P_T = (n \times P_{SW} \times f) + (\text{Loads} \times \text{Prdy} \times I_{OL} \times V_{OL})$$

where n is the number of switching outputs; f is the frequency of the device; loads is the resistive power component, typically a TTL load; and Prdy is the percent duty cycle that the output is sinking current.

8/ The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. For V_{OUT} measurements, L ≤ 0.5 V and H ≥ 4.0 V and are tested at V_{DD} = 4.5 V and 5.5 V.

9/ For propagation delay tests, all paths must be tested.

TABLE IB. SEP test limits. 1/ 2/ 3/

Device type	V_{DD} = 4.5 V		Bias V_{DD} = 5.5 V For latch-up (SEL) test no latch-up occurs at effective LET 4/
	Effective LET no upsets [MeV/(mg/cm^2)]	Maximum device cross section	
All	LET ≤ 80 MeV/(mg/cm$^{2`}$)	6 x 10^{-9} cm^2/bit	LET ≤ 120 MeV/(mg/cm$^{2`}$)

1/ For SEP test conditions, see 4.4.4.4 herein.
2/ Technology characterization and model verification supplemented by in-line data may be used in lieu of end-of-line testing. Test plan must be approved by TRB and qualifying activity.
3/ For SEL worst case temperature T_A = +125°C ±10°C and for SEU worst case temperature T_A = 25°C ±10°C.
4/ Tested to a LET of ≤ 120 MeV/(mg/cm^2) with no latch-up (SEL).

Device type	All
Case outlines	R and X
Terminal number	Terminal symbol
1	DIR
2	A1
3	A2
4	A3
5	A4
6	A5
7	A6
8	A7
9	A8
10	V_{SS}
11	B8
12	B7
13	B6
14	B5
15	B4
16	B3
17	B2
18	B1
19	$\overline{G}$
20	V_{DD}

FIGURE 1. Terminal connections.

Inputs		Operation
$\overline{G}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

H = High voltage level
L = Low voltage leve
X = Don’t care

FIGURE 2. Truth table.

Device type 01

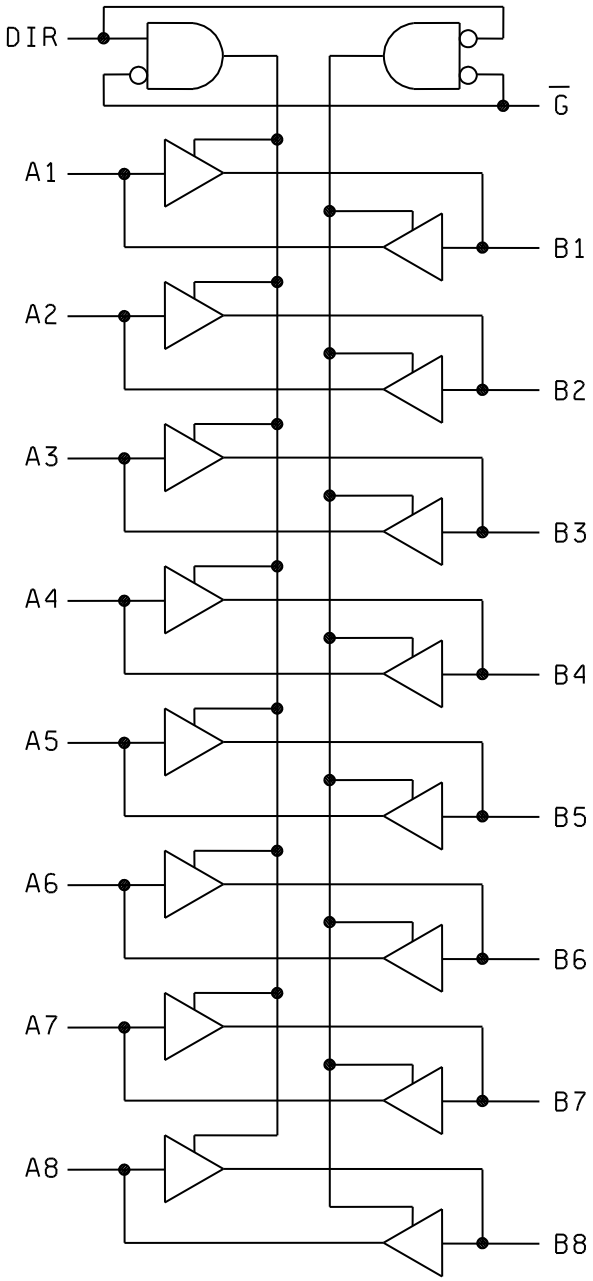


FIGURE 3. Logic diagrams.

Device type 02

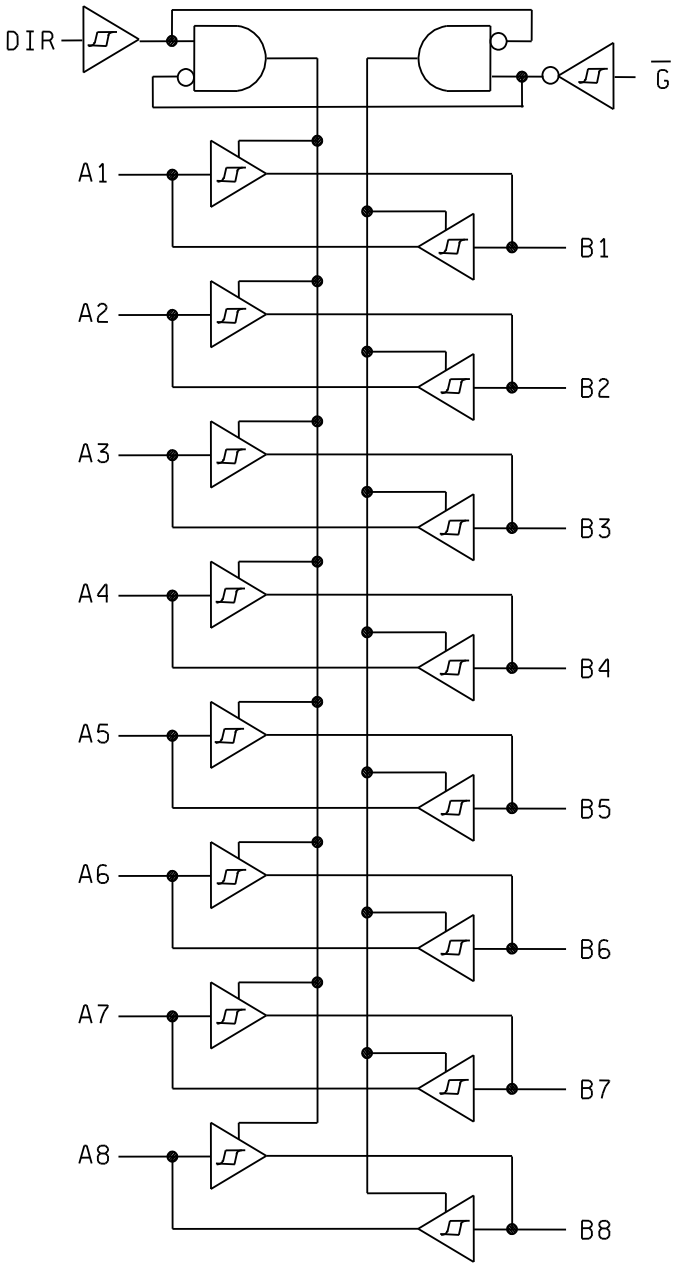
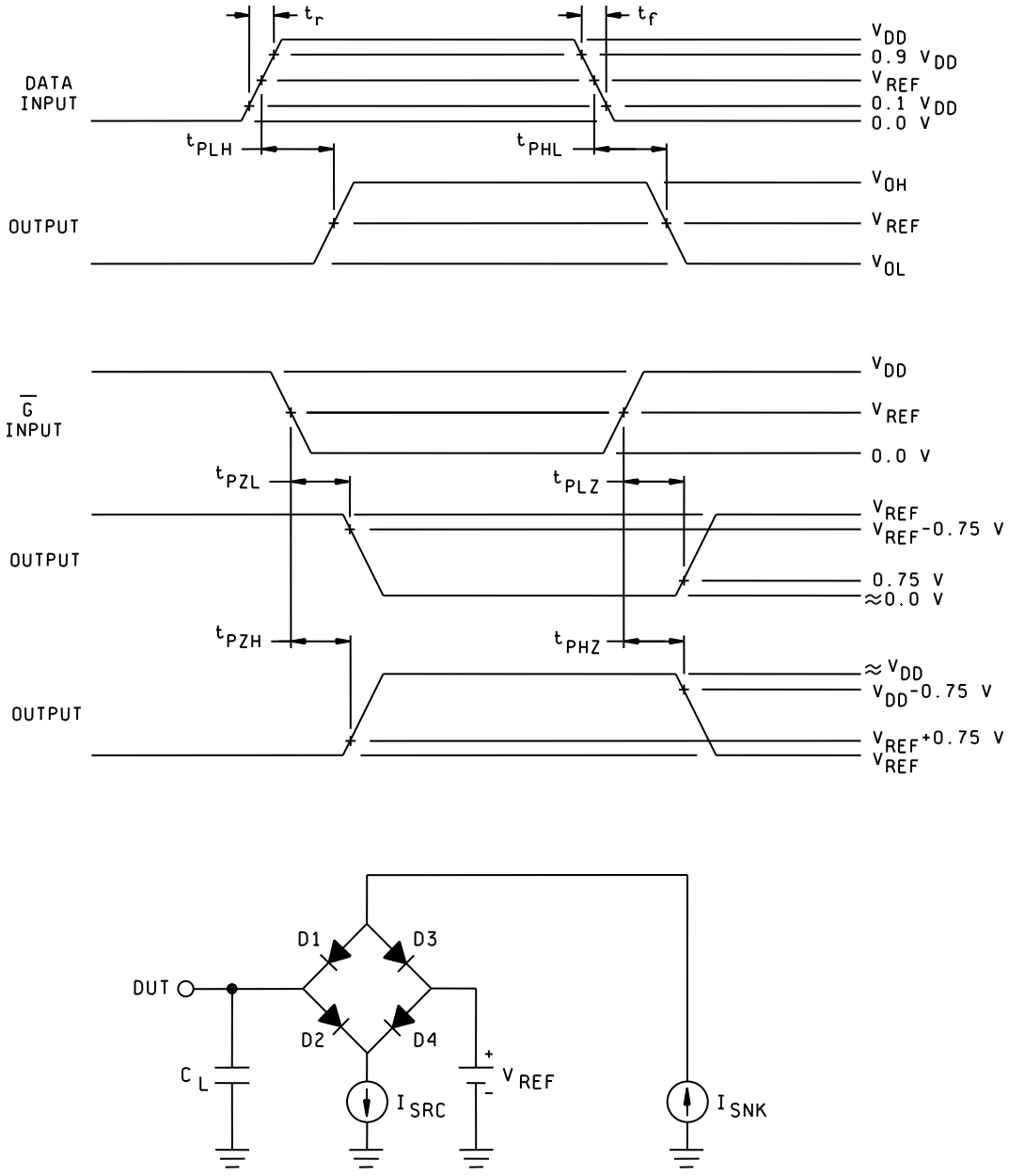


FIGURE 3. Logic diagrams - Continued.



NOTES:
1. $V_{REF} = V_{DD}/2$.
2. C_L = 50 pF minimum or equivalent (includes test jig and probe capacitance).
3. I_{SRC} is set to -1.0 mA and I_{SNK} is set to 1.0 mA for t_{PHL}, t_{PLH}, t_{PZL}, and t_{PZH} measurements. I_{SRC} is set to -12.0 mA and I_{SNK} is set to 12.0 mA for t_{PLZ} and t_{PHZ} measurements.
4. Input signal from pulse generator: V_{IN} = 0.0 V to V_{DD}; f ≤ 10 MHz; t_r = 1.0 ns/V ±0.3 ns/V; t_f = 1.0 ns/V ±0.3 ns/V; t_r and t_f shall be measured from 0.1 V_{DD} to 0.9 V_{DD} and from 0.9 V_{DD} to 0.1 V_{DD}, respectively.

FIGURE 4. Switching waveforms and test circuit.

4. VERIFICATION

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection.

4.2.1 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table IIA herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections, and as specified herein.

4.4.1 Group A inspection.

a. Tests shall be as specified in table IIA herein.

b. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device.

c. C_{IN} and C_{OUT} shall be measured only for initial qualification and after process or design changes which may affect capacitance. C_{IN} shall be measured between the designated terminal and V_{SS} at a frequency of 1 MHz. For C_{IN} and C_{OUT}, test all applicable pins on five devices with zero failures.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.2.1 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table IIA herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table IIA herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table IA at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table IIA herein.

TABLE IIA. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7, 9	1, 7, 9
Final electrical parameters (see 4.2)	1, 2, 3, 7, 8, 9, 10, 11 1/	1, 2, 3, 7, 8, 9, 10, 11 2/ 3/
Group A test requirements (see 4.4)	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11	1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11 3/
Group D end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9

1/ PDA applies to subgroups 1 and 7.
2/ PDA applies to subgroups 1, 7, and deltas.
3/ Delta limits, as specified in table IIB, shall be required where specified, and the delta values shall be completed with reference to the zero hour electrical parameters.

TABLE IIB. Burn-in and operating life test, delta parameters (+25°C).

Parameters	Symbol	Delta limits
Output voltage low	V_{OL}	±100 mV
Output voltage high	V_{OH}	±100 mV

4.4.4.1 Total dose irradiation testing. Total dose irradiation testing shall be performed in accordance with MIL-STD-883, method 1019 condition A, and as specified herein.

4.4.4.1.1 Accelerated annealing testing. Accelerated annealing testing shall be performed on all devices requiring a RHA level greater than 5K Rad (Si). The post-anneal end-point electrical parameter limits shall be as specified in table IA herein and shall be the pre-irradiation end-point electrical parameter limits at 25°C ±5°C. Testing shall be performed at initial qualification and after any design or process changes which may affect the RHA response of the device.

4.4.4.2 Dose rate induced latch-up testing. When required by the customer, dose rate induced latch-up testing shall be performed in accordance with method 1020 of MIL-STD-883 and as specified herein. Tests shall be performed on devices, SEC, or approved test structures at technology qualification and after any design or process changes which may affect the RHA capability of the process.

4.4.4.3 Dose rate upset testing. When required by the customer, dose rate upset testing shall be performed in accordance with method 1021 of MIL-STD-883 and herein.

a. Transient dose rate upset testing for class Q and V devices shall be performed as specified by a TRB approved radiation hardness assurance plan and MIL-PRF-38535. Device parametric parameters that influence upset immunity shall be monitored at the wafer level in accordance with the wafer level hardness assurance plan and MIL-PRF-38535.

4.4.4.4 Single event phenomena (SEP). When specified in the purchase order or contract, SEP testing shall be required on class V devices. SEP testing shall be performed on the Standard Evaluation Circuit (SEC) or alternate SEP test vehicle as approved by the qualifying activity at initial qualification and after any design or process changes which may affect the upset or latchup characteristics. Test four devices with zero failures. ASTM F1192 may be used as a guideline when performing SEP testing. The test conditions for SEP are as follows:

a. The ion beam angle of incidence shall be between normal to the die surface and 60° to the normal, inclusive (i.e. $0° \leq$ angle $\leq 60°$). No shadowing of the ion beam due to fixturing or package related effects is allowed.

b. The fluence shall be $\geq$100 errors or $\geq 10^7$ ions/cm^2.

c. The flux shall be between 10^2 and 10^5 ions/cm^2/s. The cross-section shall be verified to be flux independent by measuring the cross-section at two flux rates which differ by at least an order of magnitude.

d. The particle range shall be $\geq$ 20 micron in silicon.

e. The test temperature shall be +25°C for the upset measurements and the maximum rated operating temperature $\pm$10°C for the latch-up measurements.

f. Bias conditions shall be defined by the manufacturer for the latch-up measurements.

g. For SEP test limits, see table IB herein.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit V_{SS} terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform DLA Land and Maritime when a system application requires configuration control and which SMD's are applicable to that system. DLA Land and Maritime will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DLA Land and Maritime-VA, telephone (614) 692-8108.

6.4 Comments. Comments on this drawing should be directed to DLA Land and Maritime-VA, Columbus, Ohio 43218-3990, or telephone (614) 692-0540.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in MIL-HDBK-103 and QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DLA Land and Maritime-VA and have agreed to this drawing.

6.7 Additional information. When specified in the purchase order or contract, a copy of the following additional data shall be supplied.

a. RHA test conditions of SEP.

b. Number of upsets (SEU).

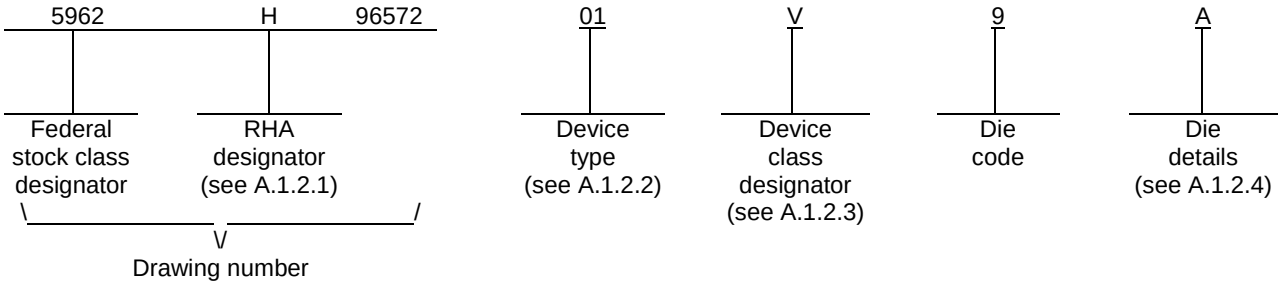
c. Number of transients (SET).

d. Occurrence of latch-up (SEL).

A.1 SCOPE

A.1.1 Scope. This appendix establishes minimum requirements for microcircuit die to be supplied under the Qualified Manufacturers List (QML) Program. QML microcircuit die meeting the requirements of MIL-PRF-38535 and the manufacturers approved QM plan for use in monolithic microcircuits, multi-chip modules (MCMs), hybrids, electronic modules, or devices using chip and wire designs in accordance with MIL-PRF-38534 are specified herein. Two product assurance classes consisting of military high reliability (device class Q) and space application (device class V) are reflected in the Part or Identification Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels is reflected in the PIN.

A.1.2 PIN. The PIN is as shown in the following example:



A.1.2.1 RHA designator. Device classes Q and V RHA identified die shall meet the MIL-PRF-38535 specified RHA levels. A dash (-) indicates a non-RHA die.

A.1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	54ACS245	Radiation hardened, octal bus transceiver with three-state outputs
02	54ACS245S	Radiation hardened, Schmitt octal bus transceiver with three-state outputs

.1.2.3 Device class designator.

Device class	Device requirements documentation
Q or V	Certification and qualification to the die requirements of MIL-PRF-38535

A.1.2.4 Die details. The die details designation is a unique letter which designates the die's physical dimensions, bonding pad location(s) and related electrical function(s), interface materials, and other assembly related information, for each product and variant supplied to this appendix.

A.1.2.4.1 Die physical dimensions.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.2 Die bonding pad locations and electrical functions.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.3 Interface materials.

Die type	Figure number
01	A-1
02	A-2

A.1.2.4.4 Assembly related information.

Die type	Figure number
01	A-1
02	A-2

A.1.3 Absolute maximum ratings. See paragraph 1.3 herein for details.

A.1.4 Recommended operating conditions. See paragraph 1.4 herein for details.

A.2 APPLICABLE DOCUMENTS

A.2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those cited in the solicitation or contract.

DEPARTMENT OF DEFENSE SPECIFICATION

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

DEPARTMENT OF DEFENSE STANDARD

MIL-STD-883 - Test Method Standard Microcircuits.

DEPARTMENT OF DEFENSE HANDBOOKS

MIL-HDBK-103 - List of Standard Microcircuit Drawings.
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Copies of these documents are available online at http://quicksearch.dla.mil or from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094).

A.2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

A.3 REQUIREMENTS

A.3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

A.3.2 Design, construction and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein and the manufacturer's QM plan for device classes Q and V.

A.3.2.1 Die physical dimensions. The die physical dimensions shall be as specified in A.1.2.4.1 and on figures A-1 and A-2.

A.3.2.2 Die bonding pad locations and electrical functions. The die bonding pad locations and electrical functions shall be as specified in A.1.2.4.2 and on figures A-1 and A-2.

A.3.2.3 Interface materials. The interface materials for the die shall be as specified in A.1.2.4.3 and on figures A-1 and A-2.

A.3.2.4 Assembly related information. The assembly related information shall be as specified in A.1.2.4.4 and on figures A-1 and A-2.

A.3.2.5 Truth table. The truth table shall be as defined in paragraph 3.2.3 herein.

A.3.2.6 Radiation exposure circuit. The radiation exposure circuit shall be as defined in paragraph 3.2.6 herein.

A.3.3 Electrical performance characteristics and post-irradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and post-irradiation parameter limits are as specified in table IA of the body of this document.

A.3.4 Electrical test requirements. The wafer probe test requirements shall include functional and parametric testing sufficient to make the packaged die capable of meeting the electrical performance requirements in table IA.

A.3.5 Marking. As a minimum, each unique lot of die, loaded in single or multiple stack of carriers, for shipment to a customer, shall be identified with the wafer lot number, the certification mark, the manufacturer's identification and the PIN listed in A.1.2 herein. The certification mark shall be a "QML" or "Q" as required by MIL-PRF-38535.

A.3.6 Certification of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see A.6.4 herein). The certificate of compliance submitted to DLA Land and Maritime -VA prior to listing as an approved source of supply for this appendix shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and the requirements herein.

A.3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 shall be provided with each lot of microcircuit die delivered to this drawing.

A.4 VERIFICATION

A.4.1 Sampling and inspection. For device classes Q and V, die sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modifications in the QM plan shall not affect the form, fit, or function as described herein.

A.4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and as defined in the manufacturer's QM plan. As a minimum, it shall consist of:

a. Wafer lot acceptance for Class V product using the criteria defined in MIL-STD-883, method 5007.

b. 100% wafer probe (see paragraph A.3.4 herein).

c. 100% internal visual inspection to the applicable class Q or V criteria defined in MIL-STD-883, method 2010 or the alternate procedures allowed in MIL-STD-883, method 5004.

A.4.3 Conformance inspection.

A.4.3.1 Group E inspection. Group E inspection is required only for parts intended to be identified as radiation assured (see A.3.5 herein). RHA levels for device classes Q and V shall be as specified in MIL-PRF-38535. End point electrical testing of packaged die shall be as specified in table IIA herein. Group E tests and conditions are as specified in paragraphs 4.4.4 herein.

A.5 DIE CARRIER

A.5.1 Die carrier requirements. The requirements for the die carrier shall be accordance with the manufacturer's QM plan or as specified in the purchase order by the acquiring activity. The die carrier shall provide adequate physical, mechanical and electrostatic protection.

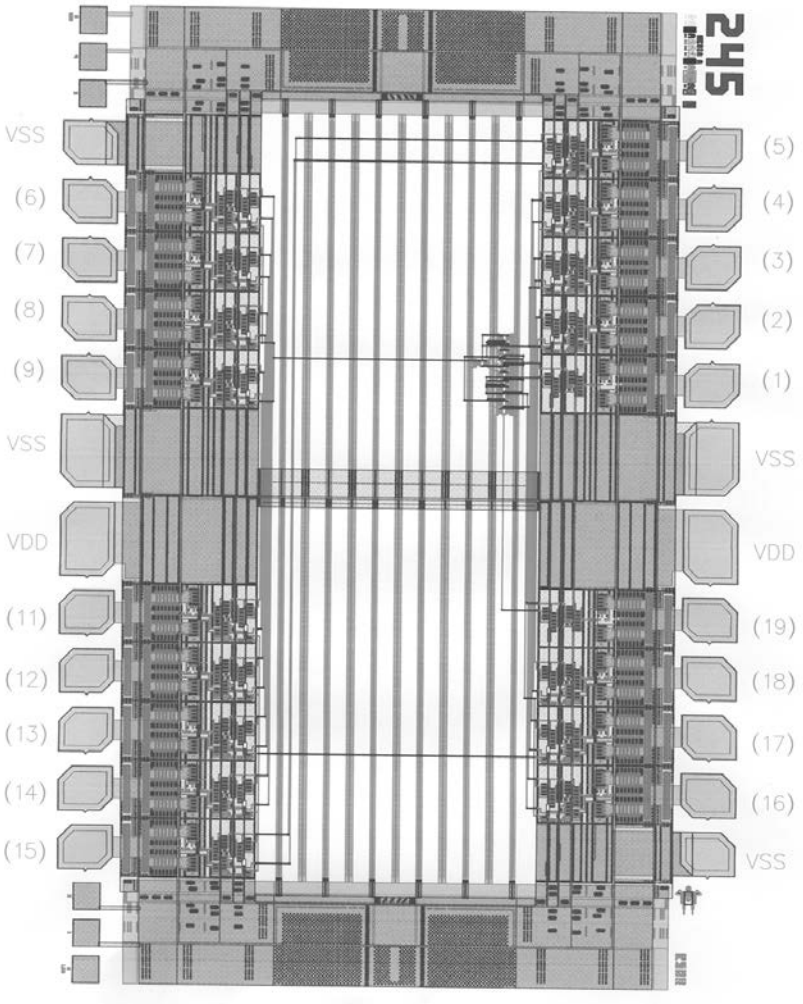
A.6 NOTES

A.6.1 Intended use. Microcircuit die conforming to this drawing are intended for use in microcircuits built in accordance with MIL-PRF-38535 or MIL-PRF-38534 for government microcircuit applications (original equipment), design applications, and logistics purposes.

A.6.2 Comments. Comments on this appendix should be directed to DLA Land and Maritime -VA, P.O. Box 3990, Columbus, Ohio 43218-3990 or telephone (614) 692-0540.

A.6.3 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

A.6.4 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed within QML-38535 have submitted a certificate of compliance (see A.3.6 herein) to DLA Land and Maritime -VA and have agreed to this drawing.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines R and X (see figure 1).

FIGURE A-1. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	111 x 81 mils.
Die thickness:	17 ±1 mils

Interface materials.

Top metallization:	Si Al Cu
Thickness	9.0kÅ – 12.5kÅ
Backside metallization:	None

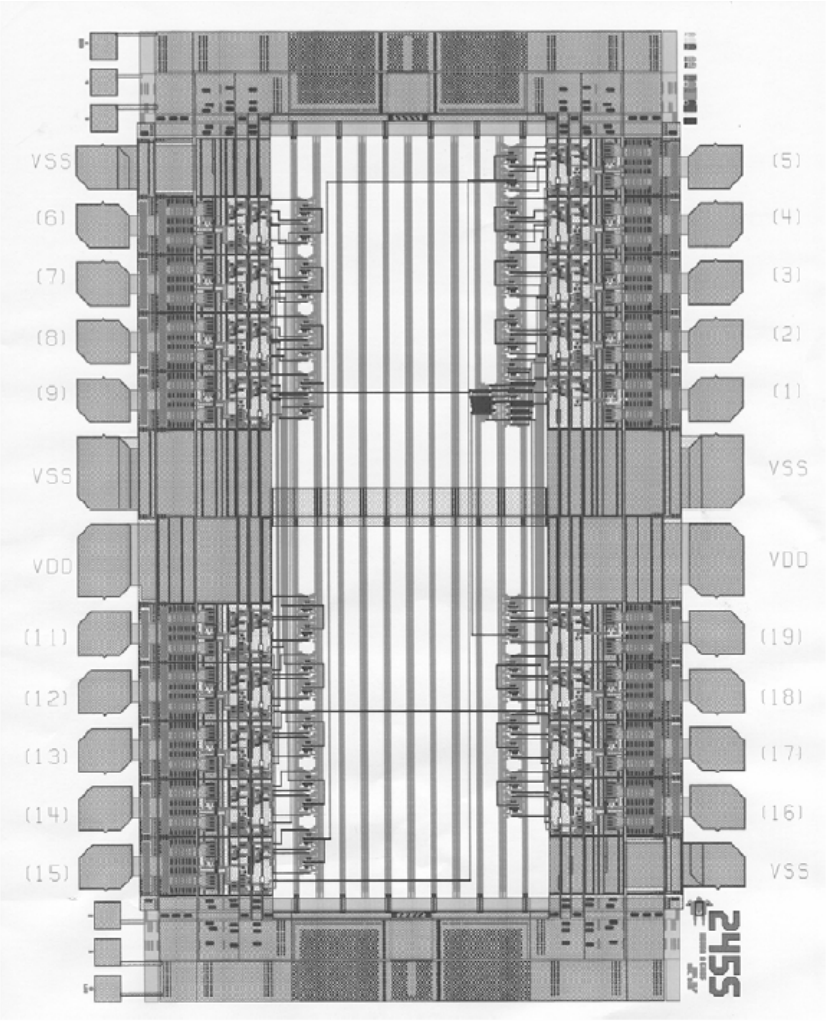
Glassivation.

Type:	Phosphorous Doped SiO2
Thickness:	9.0kÅ – 11.0kÅ
Substrate:	Epitaxial Layer on Single Crystal Silicon.

Assembly related information.

Substrate potential:	Tied to V_{SS}
Special assembly instructions:	None

FIGURE A-1. Die bonding pad locations and electrical functions - Continued.



NOTE: Pad numbers reflect terminal numbers when placed in case outlines R and X (see figure 1).

FIGURE A-2. Die bonding pad locations and electrical functions.

Die physical dimensions.

Die size:	111 x 81 mils.
Die thickness:	17 ±1 mils

Interface materials.

Top metallization:	Si Al Cu
Thickness	9.0kÅ – 12.5kÅ
Backside metallization:	None

Glassivation.

Type:	Phosphorous Doped SiO2
Thickness:	9.0kÅ – 11.0kÅ
Substrate:	Epitaxial Layer on Single Crystal Silicon.

Assembly related information.

Substrate potential:	Tied to V_{SS}
Special assembly instructions:	None

FIGURE A-2. Die bonding pad locations and electrical functions - Continued.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 17-10-30

Approved sources of supply for SMD 5962-96572 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DLA Land and Maritime-VA. This information bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535. DLA Land and Maritime maintains an online database of all current sources of supply at https://landandmaritimeapps.dla.mil/Programs/Smcr/.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962H9657201VRA	65342	UT54ACS245PVAH
5962H9657201VXA	65342	UT54ACS245UVAH
5962H9657201VRC	65342	UT54ACS245PVCH
5962H9657201VXC	65342	UT54ACS245UVCH
5962H9657201QRA	65342	UT54ACS245PQAH
5962H9657201QXA	65342	UT54ACS245UQAH
5962H9657201QRC	65342	UT54ACS245PQCH
5962H9657201QXC	65342	UT54ACS245UQCH
5962H9657201V9A	65342	UT54ACS245-V-DIEH
5962H9657201Q9A	65342	UT54ACS245-Q-DIEH
5962H9657202VRA	65342	UT54ACS245SPVAH
5962H9657202VXA	65342	UT54ACS245SUVAH
5962H9657202VRC	65342	UT54ACS245SPVCH
5962H9657202VXC	65342	UT54ACS245SUVCH
5962H9657202QRA	65342	UT54ACS245SPQAH
5962H9657202QXA	65342	UT54ACS245SUQAH
5962H9657202QRC	65342	UT54ACS245SPQCH
5962H9657202QXC	65342	UT54ACS245SUQCH
5962H9657202V9A	65342	UT54ACS245S-V-DIEH
5962H9657202Q9A	65342	UT54ACS245S-Q-DIEH

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
65342	Aeroflex Colorado Springs Inc. 4350 Centennial Boulevard Colorado Springs, CO 80907-3486