

7474, LS74A, S74 Flip-Flops

Dual D-Type Flip-Flop Product Specification

Logic Products

DESCRIPTION

The '74 is a dual positive edge-triggered D-type flip-flop featuring individual Data, Clock, Set and Reset inputs; also complementary Q and \bar{Q} outputs.

Set (\bar{S}_D) and Reset (\bar{R}_D) are asynchronous active-LOW inputs and operate independently of the Clock input. Information on the Data (D) input is transferred to the Q output on the LOW-to-HIGH transition of the clock pulse. The D inputs must be stable one set-up time prior to the LOW-to-HIGH clock transition for predictable operation. Although the Clock input is level-sensitive, the positive transition of the clock pulse between the 0.8V and 2.0V levels should be equal to or less than the clock-to-output delay time for reliable operation.

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
7474	25MHz	17mA
74LS74A	33MHz	4mA
74S74	100MHz	30mA

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

ORDERING CODE

PACKAGES	COMMERCIAL RANGE $V_{CC} = 5V \pm 5\%$; $T_A = 0^\circ C$ to $+70^\circ C$
Plastic DIP	N7474N, N74LS74AN, N74S74N
Plastic SO	N741S74A, N74S74D

NOTE:

For information regarding devices processed to Military Specifications, see the Signetics Military Products Data Manual.

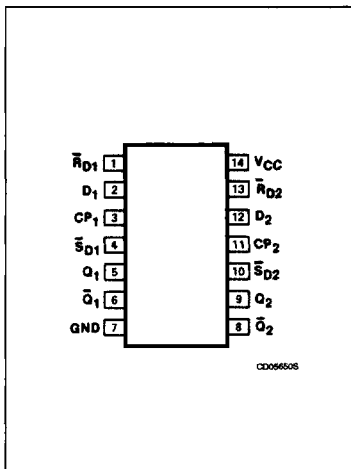
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74	74S	74LS
D	Input	1uI	1Sul	1LSul
\bar{R}_D	Input	2uI	3Sul	2LSul
\bar{S}_D	Input	1uI	2Sul	2LSul
CP	Input	2uI	2Sul	1LSul
Q, \bar{Q}	Outputs	10uI	10Sul	10LSul

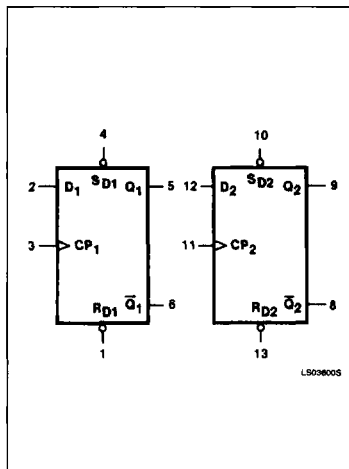
NOTE:

Where a 74 unit load (uI) is understood to be $40\mu A$ I_{IH} and $-1.6mA$ I_{IL} , a 74S unit load (Sul) is $50\mu A$ I_{IH} and $-2.0mA$ I_{IL} , and 74LS unit load (LSul) is $20\mu A$ I_{IH} and $-0.4mA$ I_{IL} .

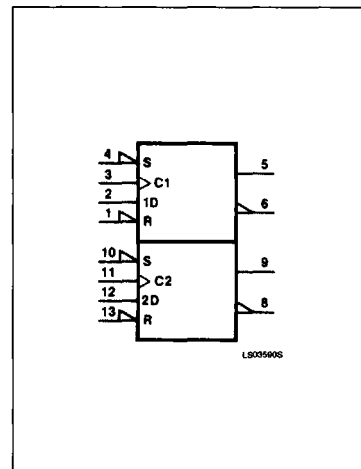
PIN CONFIGURATION



LOGIC SYMBOL



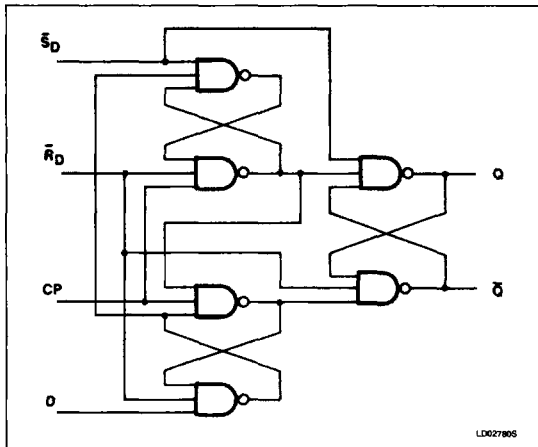
LOGIC SYMBOL (IEEE/IEC)



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LOGIC DIAGRAM



MODE SELECT — FUNCTION TABLE

OPERATING MODE	INPUTS			OUTPUTS		
	\bar{S}_D	\bar{R}_D	CP	D	Q	\bar{Q}
Asynchronous Set	L	H	X	X	H	L
Asynchronous Reset (Clear)	H	L	X	X	L	H
Undetermined ⁽¹⁾	L	L	X	X	H	H
Load "1" (Set)	H	H	↑	h	H	L
Load "0" (Reset)	H	H	↑	l	L	H

H = HIGH voltage level steady state.
 h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 L = LOW voltage level steady state.
 l = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition.
 X = Don't care.
 ↑ = LOW-to-HIGH clock transition.

NOTE:
 (1) Both outputs will be HIGH while both \bar{S}_D and \bar{R}_D are LOW, but the output states are unpredictable if \bar{S}_D and \bar{R}_D go HIGH simultaneously.

ABSOLUTE MAXIMUM RATINGS (Over operating free-air temperature range unless otherwise noted.)

PARAMETER	74	74LS	74S	UNIT
V_{CC} Supply voltage	7.0	7.0	7.0	V
V_{IN} Input voltage	-0.5 to +5.5	-0.5 to +7.0	-0.5 to +5.5	V
I_{IN} Input current	-30 to +5	-30 to +1	-30 to +5	mA
V_{OUT} Voltage applied to output in HIGH output state	-0.5 to + V_{CC}	-0.5 to + V_{CC}	-0.5 to + V_{CC}	V
T_A Operating free-air temperature range	0 to 70			°C

RECOMMENDED OPERATING CONDITIONS

PARAMETER	74			74LS			74S			UNIT
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	
V_{CC} Supply voltage	4.75	5.0	5.25	4.75	5.0	5.25	4.75	5.0	5.25	V
V_{IH} HIGH-level input voltage	2.0			2.0			2.0			V
V_{IL} LOW-level input voltage			+0.8			+0.8			+0.8	V
I_{IK} Input clamp current			-12			-18			-18	mA
I_{OH} HIGH-level output current			-400			-400			-1000	μA
I_{OL} LOW-level output current			16			8			20	mA
T_A Operating free-air temperature	0		70	0		70	0		70	°C

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DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

PARAMETER	TEST CONDITIONS ¹		7474			74LS74A			74S74			UNIT	
			Min	Typ ²	Max	Min	Typ ²	Max	Min	Typ ²	Max		
V _{OH} HIGH-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX, I _{OH} = MAX		2.4	3.4		2.7	3.4		2.7	3.4		V	
V _{OL} LOW-level output voltage	V _{CC} = MIN, V _{IH} = MIN, V _{IL} = MAX	I _{OL} = MAX		0.2	0.4		0.35	0.5			0.5	V	
		I _{OL} = 4mA (74LS)					0.25	0.4				V	
V _{IK} Input clamp voltage	V _{CC} = MIN, I _I = I _{IK}				-1.5			-1.5			-1.2	V	
I _I Input current at maximum input voltage	V _{CC} = MAX	V _I = 5.5V			1.0						1.0	mA	
		V _I = 7.0V	D input					0.1					mA
			\bar{R}_D input					0.2					mA
			\bar{S}_D input					0.2					mA
			CP input					0.1					mA
I _{IH} HIGH-level input current	V _{CC} = MAX	V _I = 2.4V	D input		40							μ A	
			\bar{R}_D input		120							μ A	
			\bar{S}_D input		80							μ A	
			CP input		80							μ A	
	V _I = 2.7V	D input					20			50		μ A	
		\bar{R}_D input					40			150		μ A	
		\bar{S}_D input					40			100		μ A	
		CP input					20			100		μ A	
I _{IL} LOW-level input current ⁵	V _{CC} = MAX	V _I = 0.4V	D input		-1.6			-0.4				mA	
			\bar{R}_D input		-3.2			-0.8				mA	
			\bar{S}_D input		-1.6			-0.8				mA	
			CP input		-3.2			-0.4				mA	
	V _I = 0.5V	D input								-2		mA	
		\bar{R}_D input								-6		mA	
		\bar{S}_D input								-4		mA	
		CP input								-4		mA	
I _{OS} Short-circuit output current ³	V _{CC} = MAX		-18		-57	-20		-100	-40		-100	mA	
I _{CC} Supply current ⁴ (total)	V _{CC} = MAX			17	30		4	8		30	50	mA	

NOTES:

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
- All typical values are at V_{CC} = 5V, T_A = 25°C.
- I_{OS} is tested with V_{OUT} = +0.5V and V_{CC} = V_{CC} MAX + 0.5V. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
- Measure I_{CC} with the Clock inputs grounded and all outputs open, with the Q and \bar{Q} outputs HIGH in turn.
- Set is tested with reset HIGH and reset is tested with set HIGH.

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AC ELECTRICAL CHARACTERISTICS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		$C_L = 15\text{pF}$, $R_L = 400\Omega$		$C_L = 15\text{pF}$, $R_L = 2\text{k}\Omega$		$C_L = 15\text{pF}$, $R_L = 280\Omega$		
		Min	Max	Min	Max	Min	Max	
f_{MAX} Maximum clock frequency	Waveform 1	15		25		75		MHz
t_{PLH} Propagation delay t_{PHL} Clock to output	Waveform 1		25 40		25 40		9 9	ns
t_{PLH} Propagation delay t_{PHL} Set or Reset to output	Waveform 2		25 40		25 40		6 13.5	ns
	Waveform 2 CP = HIGH							
t_{PHL} Set or Reset to output	Waveform 2 CP = LOW		40		40		8	ns

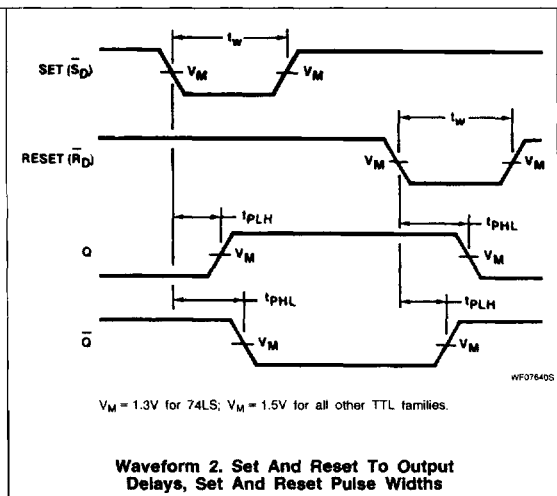
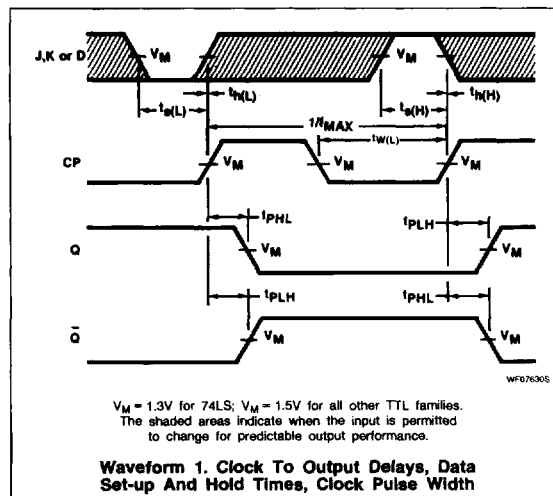
NOTE:

Per industry convention, f_{MAX} is the worst case value of the maximum device operating frequency with no constraints on t_r , t_f , pulse width or duty cycle.

AC SET-UP REQUIREMENTS $T_A = 25^\circ\text{C}$, $V_{CC} = 5.0\text{V}$

PARAMETER	TEST CONDITIONS	74		74LS		74S		UNIT
		Min	Max	Min	Max	Min	Max	
$t_{W(H)}$ Clock pulse width (HIGH)	Waveform 1	30		25		6		ns
$t_{W(L)}$ Clock pulse width (LOW)	Waveform 1	37				7.3		ns
$t_{W(L)}$ Set or reset pulse width (LOW)	Waveform 2	30		25		7		ns
$t_s(H)$ Set-up time (HIGH) data to clock	Waveform 1	20		20		3		ns
$t_s(L)$ Set-up time (LOW) data to clock	Waveform 1	20		20		3		ns
t_h Hold time data to clock	Waveform 1	5		5		2		ns

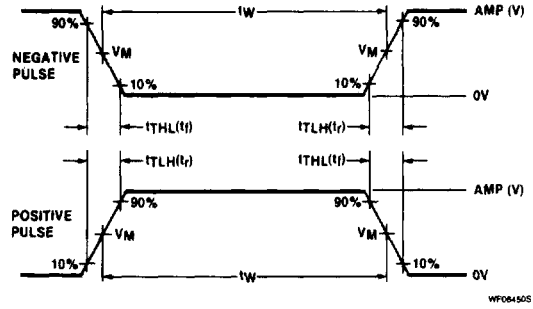
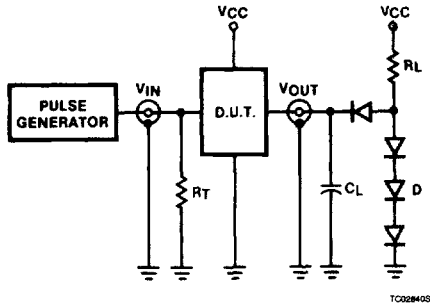
AC WAVEFORMS



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TEST CIRCUITS AND WAVEFORMS



$V_M = 1.3V$ for 74LS; $V_M = 1.5V$ for all other TTL families.

Test Circuit For 74 Totem-Pole Outputs

DEFINITIONS

R_L = Load resistor to V_{CC} ; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of Pulse Generators.

D = Diodes are 1N916, 1N3064, or equivalent.

t_{TLH} , t_{THL} Values should be less than or equal to the table entries.

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	Pulse Width	t_{TLH}	t_{THL}
74	3.0V	1MHz	500ns	7ns	7ns
74LS	3.0V	1MHz	500ns	15ns	6ns
74S	3.0V	1MHz	500ns	2.5ns	2.5ns