Signetics

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FAST Products	

FAST 74F657
Transceivers

74F657 Octal Transceivers With 8-Bit Parity Generator/Checker (3-State)

TYPE	TYPICAL PROPAGATION DELAY	TYPICAL SUPPLY CURRENT (TOTAL)
74F657	8.0ns	100mA

FEATURES

- **Combines 74F245 and 74F280A functions in one package**
- **High impedance base input for reduced loading (70µA in High and Low states)**
- **Ideal in applications where High output drive and light bus loading are required (I_{IL} is 70µA vs FAST std of 600µA)**
- **3-state buffer outputs sink 64mA and source 15 mA**
- **Input diodes for termination effects**
- **24-pin plastic Slim Dip (300mil) package**
- **Industrial temperature range available (-40°C to +85°C)**

DESCRIPTION

The 74F657 is an octal transceiver featuring non-inverting buffers with 3-state outputs and an 8-bit parity generator/checker, and is intended for bus-oriented applications. The buffers have a guaranteed current sinking capability of 24mA at the A ports and 64mA at the B ports. The Transmit/Receive ($T/\overline{R}$) input determines the direction of the data flow through the bidirectional transceivers.

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10% T_A = 0°C to +70°C	INDUSTRIAL RANGE V_{CC} = 5V±10% T_A = -40°C to +85°C
24-Pin Plastic Slim DIP (300mil)	N74F657N	I74F657N
24-Pin Plastic SOL	N74F657D	I74F657D

NOTE:

1.Thermal mounting techniques are recommended. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

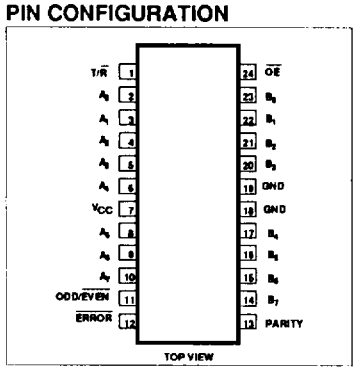
INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7	A ports 3-state inputs	3.5/0.117	70µA/70µA
B_0 - B_7	B ports 3-state inputs	3.5/0.117	70µA/70µA
PARITY	Parity input	3.5/0.117	70µA/70µA
$T/\overline{R}$	Transmit/Receive input	2.0/0.066	40µA/40µA
ODD/$\overline{EVEN}$	Parity select input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output Enable input (active Low)	2.0/0.066	40µA/40µA
A_0 - A_7	A port 3-state outputs	150/40	3.0mA/24mA
B_0 - B_7	B port 3-state outputs	750/106.7	15mA/64mA
PARITY	Parity output	750/106.7	15mA/64mA
$\overline{ERROR}$	Error output	750/106.7	15mA/64mA

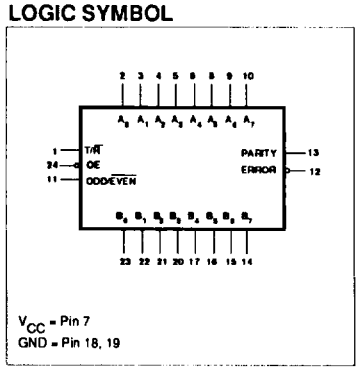
NOTE:

One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

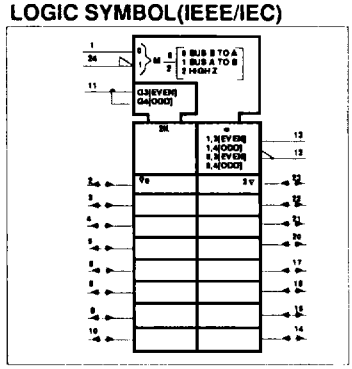
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



Transmit (active-High) enables data from A ports to B ports; Receive (active-Low) enables data from B ports to A ports.
The Output Enable ($\overline{OE}$)input disables both the A and B ports by placing them in a high impedance condition when the $\overline{OE}$ input is High. The parity select (ODD/$\overline{EVEN}$) input gives the user the option of odd or even parity systems. The parity (PARITY) pin is an output from the generator/checker when transmitting from the port A to B (T/$\overline{R}$=High) and an input when receiving from port B to A port (T/$\overline{R}$=Low). When transmitting (T/$\overline{R}$=High) the parity select (ODD/$\overline{EVEN}$) input is set, then the A port data is polled to determine the number of High bits. The parity (PARITY) output then goes to the logic state determined by the parity select (ODD/$\overline{EVEN}$) setting and by the number of High bits on port A. For example, if the parity select (ODD/$\overline{EVEN}$) is set Low (even parity), and the number of High bits on port A is odd, then the parity (PARITY) output will be High, transmitting even parity. If the number of High bits on port A is even, then the parity (PARITY) output will be Low, keeping even parity. When in receive mode (T/$\overline{R}$=Low) the B port is polled to determine the number of High bits. If parity select (ODD/$\overline{EVEN}$) is Low (even parity) and the number of Highs on port B is:

(1) odd and the parity (PARITY) input is High, then $\overline{ERROR}$ will be High, signifying no error.

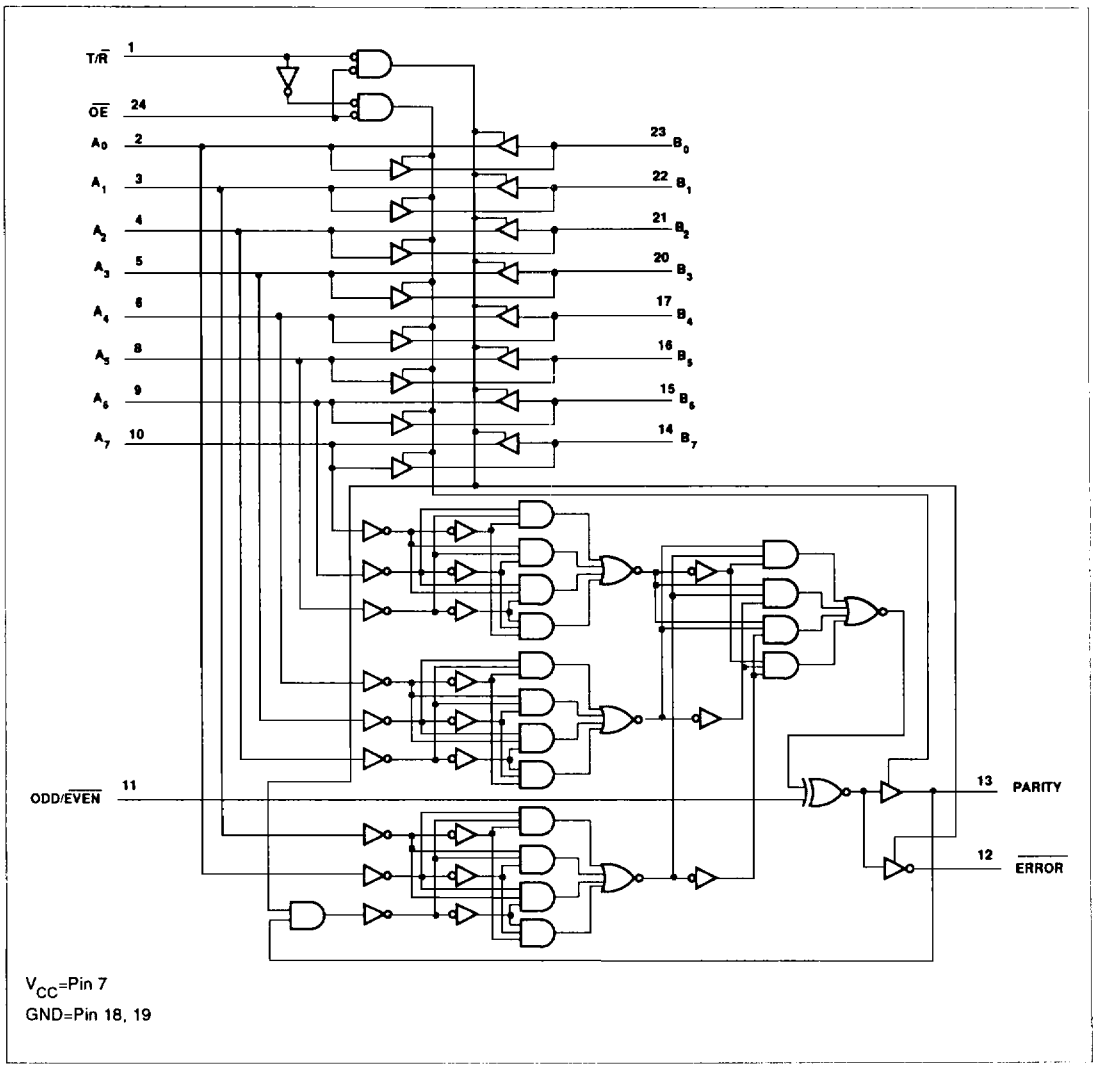
(2) even and the parity (PARITY) input is High, then $\overline{ERROR}$ will be asserted Low, indicating an error.

FUNCTION TABLE

NUMBER OF INPUTS THAT ARE HIGH	INPUTS			INPUT/ OUPUT	OUTPUTS	
	$\overline{OE}$	T/$\overline{R}$	ODD/$\overline{EVEN}$	PARITY	$\overline{ERROR}$	OUTPUTS MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receivet
	L	L	H	L	L	Receive
	L	L	L	H	L	Receivet
	L	L	L	L	H	Receivett
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receivet
	L	L	H	L	H	Receive
	L	L	L	H	H	Receivet
	L	L	L	L	L	Receivett
Don't care	H	X	X	Z	Z	3-state

H = High voltage level
L = Low voltage level
X = Don't care
Z = High impedance "off" state

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	A_0-A_7	48	mA
		B_0-B_7, PARITY, $\overline{ERROR}$	128	mA
T_A	Operating free-air temperature range	Commercial range	0 to +70	°C
		Industrial range	-40 to +85	°C
T_{STG}	Storage temperature		-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current	A_0-A_7			-3	mA
		B_0-B_7, PARITY, $\overline{ERROR}$			-15	mA
I_{OL}	Low-level output current	A_0-A_7			24	mA
		B_0-B_7, PARITY, $\overline{ERROR}$			64	mA
T_A	Operating free-air temperature range	Commercial range	0		70	°C
		Industrial range	-40		85	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS Min	LIMITS Typ[2]	LIMITS Max	UNIT
V_{OH}	High-level output voltage	All outputs	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA[4,5]	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
		B_0-B_7, PARITY, $\overline{ERROR}$		I_{OH}=-12mA[5]	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
				I_{OH}=-15mA[4]	±10%V_{CC}	2.0			V
					±5%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	A_0-A_7	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}=24mA[4,5]	±10%V_{CC}		0.35	0.50	V
					±5%V_{CC}		0.35	0.50	V
		B_0-B_7, PARITY, $\overline{ERROR}$		I_{OL}=48mA[4]	±10%V_{CC}		0.38	0.55	V
				I_{OL}=48mA[5]	±5%V_{CC}		0.42	0.55	V
				I_{OL}=64mA[4]	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximun input voltage	$\overline{OE}$, T/$\overline{R}$, ODD/$\overline{EVEN}$	V_{CC} =0.0V, V_I = 7.0V					100	µA
		A_0-A_7	V_{CC} =5.5V, V_I = 5.5V					2	mA
		B_0-B_7						1	mA
I_{IH}	High-level input current	ODD/$\overline{EVEN}$	V_{CC} =MAX, V_I = 2.7V					20[4]	µA
								40[5]	µA
		$\overline{OE}$, T/$\overline{R}$						40[4]	µA
								80[5]	µA
I_{IL}	Low-level input current	ODD/$\overline{EVEN}$	V_{CC} =MAX, V_I = 0.5V					-20	µA
		$\overline{OE}$, T/$\overline{R}$						-40	µA
I_{IH}+I_{OZH}	Off-state output current High-level voltage applied	A_0-A_7, B_0-B_7 PARITY	V_{CC} =MAX, V_I= 2.7V					70	µA
I_{IL}+I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_I= 0.5V					-70	µA
I_{OZH}	Off-state output current High-level voltage applied	$\overline{ERROR}$	V_{CC} =MAX, V_I= 2.7V					50	µA
I_{OZL}	Off-state output current Low-level voltage applied		V_{CC} =MAX, V_I= 0.5V					-50	µA
I_{OS}	Short circuit output current[3]	A_0-A_7	V_{CC} =MAX			-60		-150	mA
		B_0-B_7				-100		-225	µA
I_{CC}	Supply current (total)	I_{CCH}	V_{CC} =MAX				90	125[4]	mA
							90	135[5]	mA
		I_{CCL}					106	150[4]	mA
							106	160[5]	mA
		I_{CCZ}					98	145	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. For commercial range.
5. For industrial range.

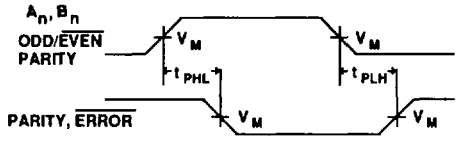
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITION	LIMITS							UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		T_A = -40°C to +85°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	2.5 3.0	5.5 6.0	7.5 7.5	2.5 3.0	8.0 8.0	2.0 2.5	9.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to PARITY	Waveform 1,2	7.0 7.0	10.0 10.0	14.0 15.0	7.0 7.0	16.0 16.0	5.5 6.5	16.5 19.0	ns
t_{PLH} t_{PHL}	Propagation delay ODD/$\overline{\text{EVEN}}$ to PARITY, $\overline{\text{ERROR}}$	Waveform 1,2	4.5 4.5	7.5 8.0	11.0 11.5	4.5 4.5	12.0 12.5	3.5 4.0	13.0 15.5	ns
t_{PLH} t_{PHL}	Propagation delay B_n to $\overline{\text{ERROR}}$	Waveform 1,2	8.0 8.0	14.0 14.0	20.5 20.5	7.5 7.5	22.5 22.5	7.5 7.5	24.5 25.0	ns
t_{PLH} t_{PHL}	Propagation delay PARITY to $\overline{\text{ERROR}}$	Waveform 1,2	8.0 8.0	11.5 12.0	15.5 15.5	7.5 8.0	16.5 17.0	6.5 6.5	18.5 20 0	ns
t_{PZH} t_{PZL}	Output Enable time[1] to High or Low level	Waveform 3 Waveform 4	3.0 4.0	5.5 7.0	8.0 9.5	3.0 4.0	9.0 11.0	2.0 4.0	9.0 13.0	ns
t_{PHZ} t_{PLZ}	Output Disable time from High or Low level	Waveform 3 Waveform 4	2.0 2.0	4.5 4.0	7.5 6.0	2.0 2.0	8.0 6.5	1.0 1.0	8.0 7.5	ns

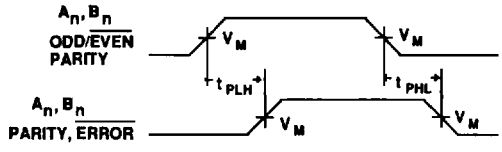
NOTE:

1. These delay times reflect the 3-state recovery time only and not the signal through the buffers or the parity check circuitry. To assure VALID information at the $\overline{\text{ERROR}}$ pin, time must be allowed for the signal to propagate through the drivers (B to A), through the parity check circuitry (same as A to PARITY), and to the $\overline{\text{ERROR}}$ output . VALID data at the $\overline{\text{ERROR}}$ pin ≥ (B to A) + (A to PARITY) .

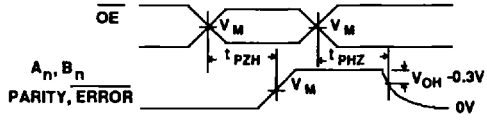
AC WAVEFORMS



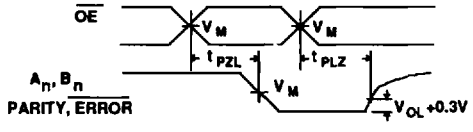
Waveform 1. Propagation Delay for Inverting Outputs



Waveform 2. Propagation Delay for Non-Inverting Outputs



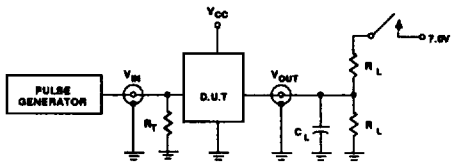
Waveform 3. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 4. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

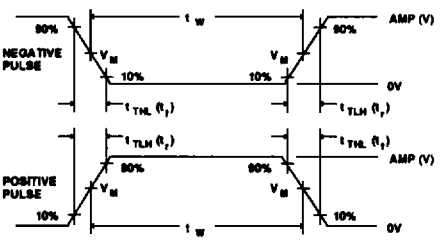
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns