

Si4532DY

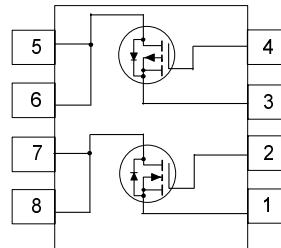
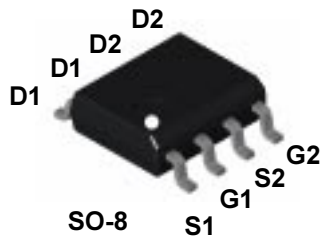
Dual N- and P-Channel Enhancement Mode Field Effect Transistor

General Description

These dual N- and P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance and provide superior switching performance. These devices are particularly suited for low voltage applications such as notebook computer power management and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

Features

- N-Channel 3.9A, 30V. $R_{DS(ON)} = 0.065\Omega @V_{GS} = 10V$
 $R_{DS(ON)} = 0.095\Omega @V_{GS} = 4.5V.$
- P-Channel -3.5A, -30V. $R_{DS(ON)} = 0.085\Omega @V_{GS} = -10V$
 $R_{DS(ON)} = 0.190\Omega @V_{GS} = -4.5V.$
- High density cell design for extremely low $R_{DS(ON)}$.
- High power and current handling capability in a widely used surface mount package.
- Dual (N & P-Channel) MOSFET in surface mount package.



Absolute Maximum Ratings T_A = 25°C unless otherwise noted

Symbol	Parameter	N-Channel	P-Channel	Units
V _{DSS}	Drain-Source Voltage	30	-30	V
V _{GSS}	Gate-Source Voltage	20	-20	V
I _D	Drain Current - Continuous (Note 1a)	3.9	-3.5	A
	- Pulsed	20	-20	
P _D	Power Dissipation for Dual Operation	2		W
	Power Dissipation for Single Operation (Note 1a)	1.6		
	(Note 1b)	1		
	(Note 1c)	0.9		
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150		°C

Thermal Characteristics

R _{θJA}	Thermal Resistance, Junction-to-Ambient	62.5	°C/W
R _{θJC}	Thermal Resistance, Junction-to-Case (Note 1)	40	°C/W

Package Marking and Ordering Information

Device Marking	Device	Reel Size	Tape Width	Quantity
4532	Si4532DY	13"	12mm	2500 units

* Die and manufacturing source subject to change without prior notification.

Electrical Characteristics $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
Off Characteristics							
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	N-Ch	30			V
		$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	P-Ch	-30			V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}, V_{GS} = 0\text{ V}$	N-Ch			1	μA
		$V_{DS} = -24\text{ V}, V_{GS} = 0\text{ V}$	P-Ch			-1	μA
I_{GSSF}	Gate-Body Leakage, Forward	$V_{GS} = 20\text{ V}, V_{DS} = 0\text{ V}$	All			100	nA
I_{GSSR}	Gate-Body Leakage, Reverse	$V_{GS} = -20\text{ V}, V_{DS} = 0\text{ V}$	All			-100	nA

On Characteristics (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	N-Ch	1		3	V
		$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	P-Ch	-1		-3	V
$R_{DS(on)}$	Static Drain-Source On Resistance	$V_{GS} = 10\text{ V}, I_D = 3.9\text{ A}$	N-Ch		0.053	0.065	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 3.1\text{ A}$			0.081	0.095	
		$V_{GS} = -10\text{ V}, I_D = -2.5\text{ A}$	P-Ch		0.06	0.085	
		$V_{GS} = -4.5\text{ V}, I_D = -1.8\text{ A}$			0.095	0.19	
$I_{D(on)}$	On-State Drain Current	$V_{GS} = 10\text{ V}, V_{DS} = 5\text{ V}$	N-Ch	15			A
		$V_{GS} = -10\text{ V}, V_{DS} = -5\text{ V}$	P-Ch	-15			
g_{FS}	Forward Transconductance	$V_{DS} = 15\text{ V}, I_D = 3.9\text{ A}$	N-Ch		7		S
		$V_{DS} = -15\text{ V}, I_D = -2.5\text{ A}$	P-Ch		5		

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch		235		pF	
			P-Ch		420			
C_{oss}	Input Capacitance		$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$	N-Ch		150		pF
				P-Ch		140		
C_{riss}	Reverse Transfer Capacitance			N-Ch		49		pF
				P-Ch		60		

Electrical Characteristics (continued)

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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Switching Characteristics (Note 2)

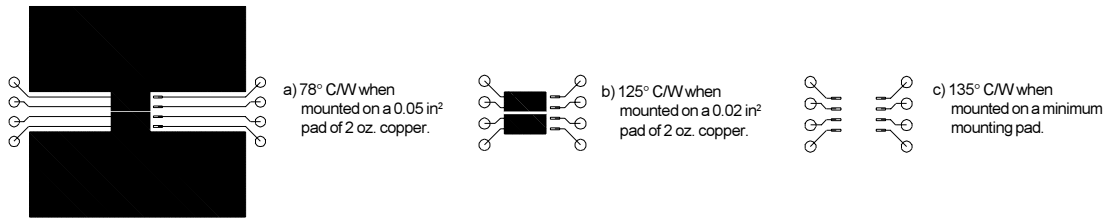
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}$, $I_D = 1\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$	N-Ch		7	13	ns
			P-Ch		9	18	
t_r	Turn-On Rise Time		N-Ch		18	29	ns
			P-Ch		8	16	
$t_{d(off)}$	Turn-Off Delay Time	$V_{DD} = -10\text{ V}$, $I_D = -2.5\text{ A}$, $V_{GS} = -10\text{ V}$, $R_{GEN} = 6\ \Omega$	N-Ch		15	27	ns
			P-Ch		18	29	
t_f	Turn-Off Fall Time		N-Ch		0.8	8	ns
			P-Ch		6	12	
t_{rr}	Drain-Source Reverse Recovery Time	$I_F = 1.7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ $I_F = -1.7\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	N-Ch			80	nS
			P-Ch			80	
Q_g	Total Gate Charge	$V_{DS} = 10\text{ V}$, $I_D = 3.9\text{ A}$, $V_{GS} = 10\text{ V}$	N-Ch		3.7	15	nC
			P-Ch		5	15	
Q_{gs}	Gate-Source Charge	$V_{DS} = -10\text{ V}$, $I_D = -2.5\text{ A}$, $V_{GS} = -10\text{ V}$	N-Ch		0.9		nC
			P-Ch		1.7		
Q_{gd}	Gate-Drain Charge		N-Ch		1.9		nC
			P-Ch		1.8		

Drain-Source Diode Characteristics and Maximum Ratings

I_S	Maximum Continuous Drain-Source Diode Forward Current		N-Ch			1.7	A
			P-Ch			-1.7	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 1.7\text{ A}$ (Note 2)	N-Ch		0.75	1.2	V
			P-Ch		-0.75	-1.2	V

Notes:

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



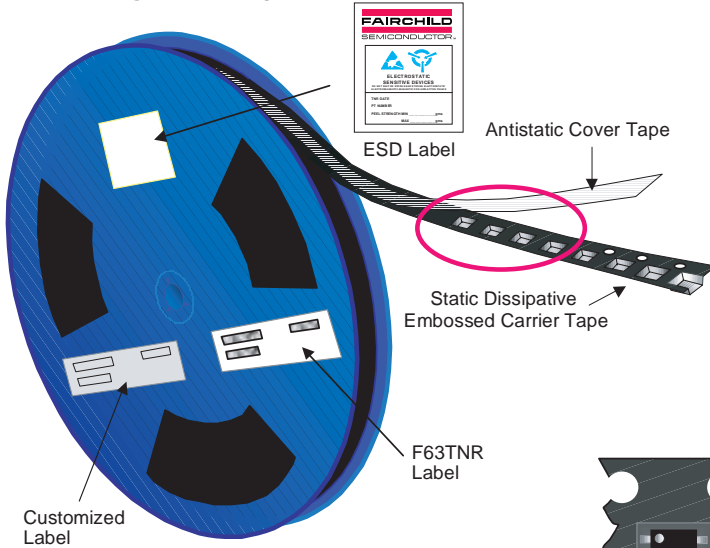
Scale 1 : 1 on letter size paper

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$

SO-8 Tape and Reel Data and Package Dimensions



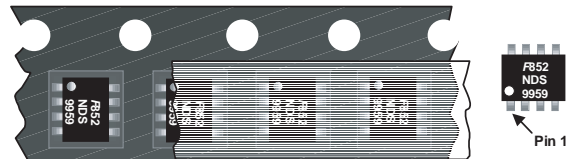
SOIC(8lds) Packaging Configuration: Figure 1.0



Packaging Description:

SOIC-8 parts are shipped in tape. The carrier tape is made from a dissipative (carbon filled) polycarbonate resin. The cover tape is a multilayer film (Heat Activated Adhesive in nature) primarily composed of polyester film, adhesive layer, sealant, and anti-static sprayed agent. These reeled parts in standard option are shipped with 2,500 units per 13" or 330cm diameter reel. The reels are dark blue in color and is made of polystyrene plastic (anti-static coated). Other option comes in 500 units per 7" or 177cm diameter reel. This and some other options are further described in the Packaging Information table.

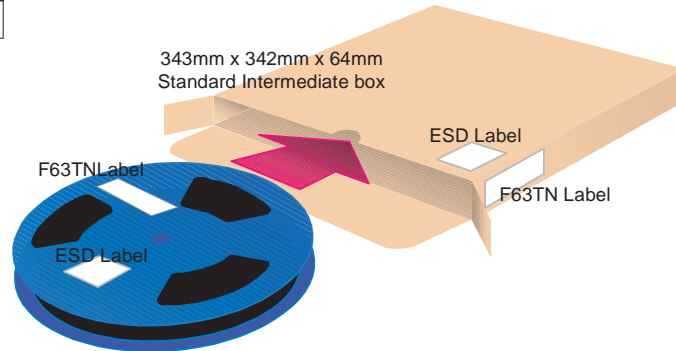
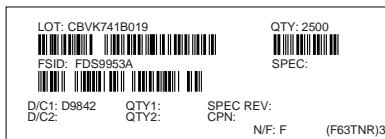
These full reels are individually barcode labeled and placed inside a standard intermediate box (illustrated in figure 1.0) made of recyclable corrugated brown paper. One box contains two reels maximum. And these boxes are placed inside a barcode labeled shipping box which comes in different sizes depending on the number of parts shipped.



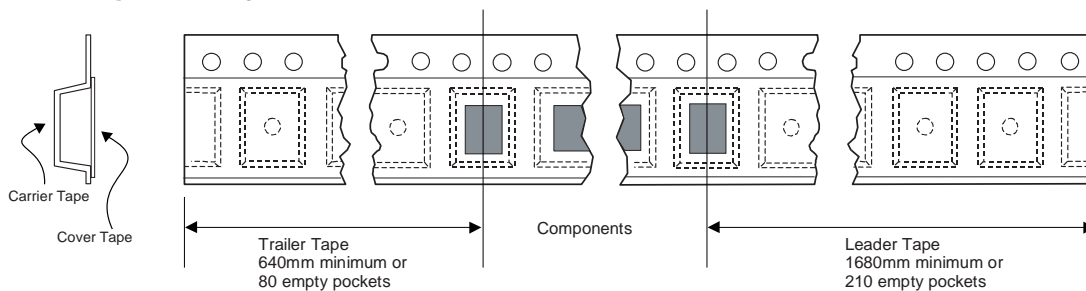
SOIC-8 Unit Orientation

SOIC (8lds) Packaging Information				
Packaging Option	Standard (no flow code)	L86Z	F011	D84Z
Packaging type	TNR	Rail/Tube	TNR	TNR
Qty per Reel/Tube/Bag	2,500	95	4,000	500
Reel Size	13" Dia	-	13" Dia	7" Dia
Box Dimension (mm)	343x64x343	530x130x83	343x64x343	184x187x47
Max qty per Box	5,000	30,000	8,000	1,000
Weight per unit (gm)	0.0774	0.0774	0.0774	0.0774
Weight per Reel (kg)	0.6060	-	0.9696	0.1182
Note/Comments				

F63TNR Label sample

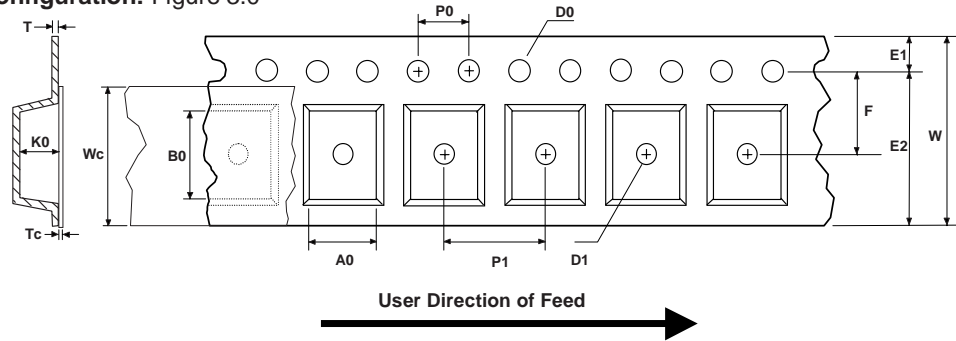


SOIC(8lds) Tape Leader and Trailer Configuration: Figure 2.0



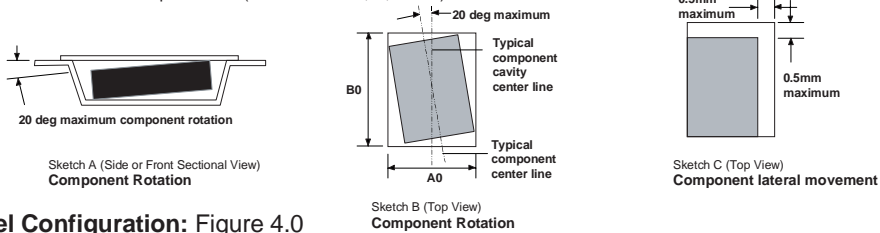
SO-8 Tape and Reel Data and Package Dimensions, continued

SOIC(8lds) Embossed Carrier Tape Configuration: Figure 3.0

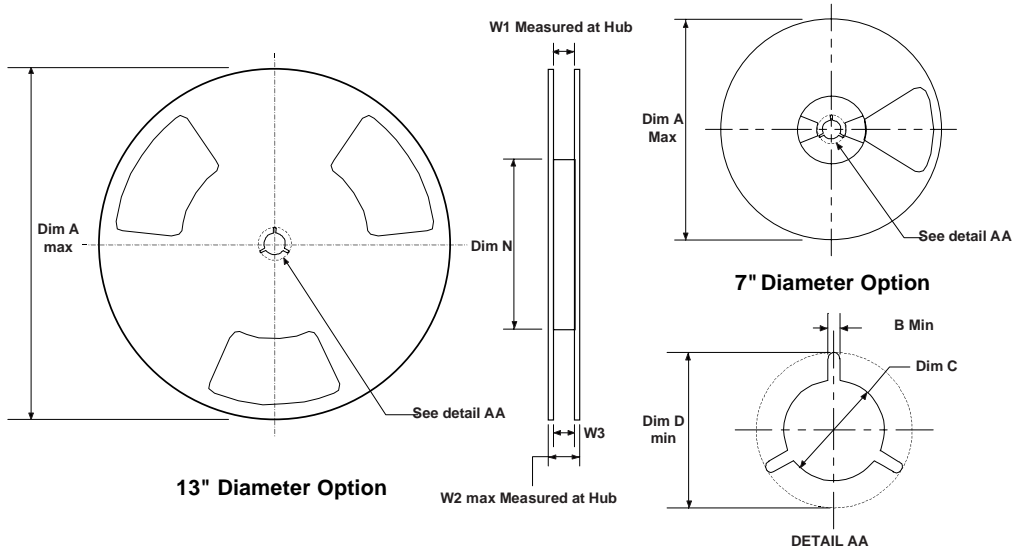


Dimensions are in millimeter														
Pkg type	A0	B0	W	D0	D1	E1	E2	F	P1	P0	K0	T	Wc	Tc
SOIC(8lds) (12mm)	6.50 +/-0.10	5.30 +/-0.10	12.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	10.25 min	5.50 +/-0.05	8.0 +/-0.1	4.0 +/-0.1	2.1 +/-0.10	0.450 +/- 0.150	9.2 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



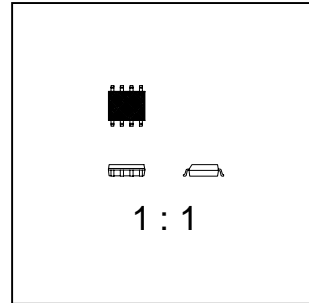
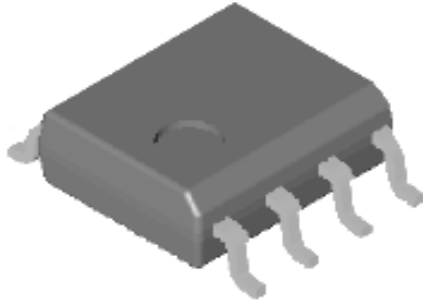
SOIC(8lds) Reel Configuration: Figure 4.0



Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
12mm	7" Dia	7.00 177.8	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	2.165 55	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4
12mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	7.00 178	0.488 +0.078/-0.000 12.4 +2/0	0.724 18.4	0.469 - 0.606 11.9 - 15.4

SO-8 Tape and Reel Data and Package Dimensions, continued

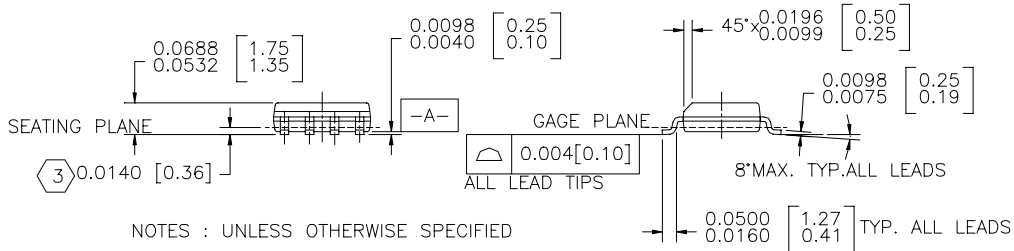
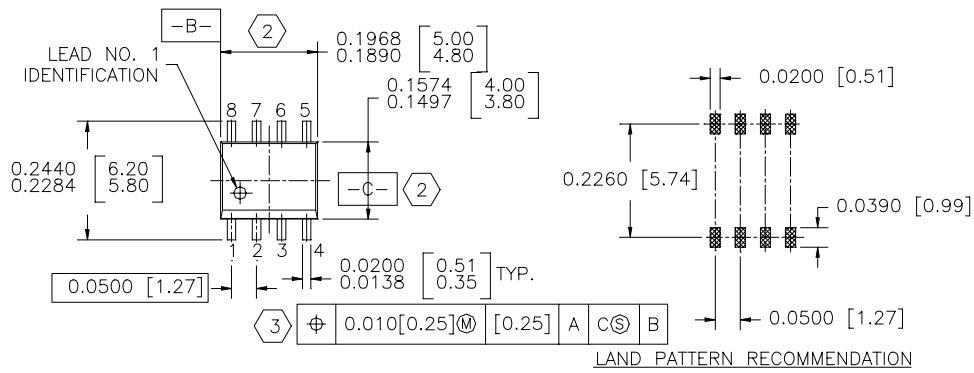
SOIC-8 (FS PKG Code S1)



Scale 1:1 on letter size paper

Dimensions shown below are in:
inches [millimeters]

Part Weight per unit (gram): 0.0774



NOTES : UNLESS OTHERWISE SPECIFIED

1. STANDARD LEAD FINISH:
200 MICROINCHES / 5.08 MICRONS MINIMUM
LEAD / TIN (SOLDER) ON COPPER.

SO 0.150 WIDE 8 LEADS

2. THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH

3. MAXIMUM LEAD 0.024 [0.609]

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