National Semiconductor

MM54HC4302/MM74HC4302
TTL Input Octal TRI-STATE® Latch

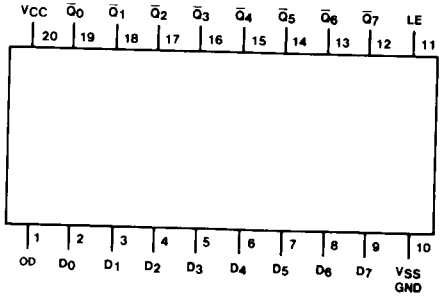
General Description

This high speed OCTAL D-TYPE LATCH is manufactured with silicon gate CMOS technology. All inputs are compatible with TTL logic levels, recognizing a zero input below 0.8 V and a logical one input above 2.0 V. It possesses the low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads (12 LS-TTL loads for 54HC). Due to the large output drive capability and the TRI-STATE feature, this device is ideally suited for interfacing with bus lines in a bus organized system.

When the LATCH ENABLE input is high, the Q outputs will follow the D inputs. When LATCH ENABLE goes low, data at the D inputs will be retained at the outputs until LATCH ENABLE returns high again. When a high logic level is applied to the OUTPUT DISABLE input, all outputs go to a high impedance state, regardless of what signals are present at the other inputs and the state of the storage elements.

The 54HC/74HC logic family is functionally as well as pinout compatible with the standard 54LS/74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Connection Diagram



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Truth Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Logic Diagram