

MEMORY  
CMOS

1M × 16 BIT  
FAST PAGE MODE DYNAMIC RAM

MB81V16160B-50/-60/-50L/-60L

CMOS 1,048,576 × 16 Bit Fast Page Mode Dynamic RAM

■ DESCRIPTION

The Fujitsu MB81V16160B is a fully decoded CMOS Dynamic RAM (DRAM) that contains 16,777,216 memory cells accessible in 16-bit increments. The MB81V16160B features a "fast page" mode of operation whereby high-speed random access of up to 256 bits of data within the same row can be selected. The MB81V16160B DRAM is ideally suited for mainframe, buffers, hand-held computers video imaging equipment, and other memory applications where very low power dissipation and high bandwidth are basic requirements of the design. Since the standby current of the MB81V16160B is very small, the device can be used as a non-volatile memory in equipment that uses batteries for primary and/or auxiliary power.

The MB81V16160B is fabricated using silicon gate CMOS and Fujitsu's advanced four-layer polysilicon and two-layer aluminum process. This process, coupled with advanced stacked capacitor memory cells, reduces the possibility of soft errors and extends the time interval between memory refreshes. Clock timing requirements for the MB81V16160B are not critical and all inputs are LVTTTL compatible.

■ PRODUCT LINE & FEATURES

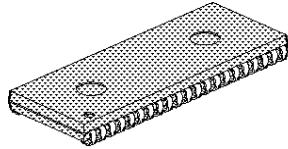
Parameter		MB81V16160B				
		-50	-50L	-60	-60L	
RAS Access Time		50 ns max.		60 ns max.		
Random Cycle Time		110 ns min.		110 ns min.		
Address Access Time		25 ns max.		30 ns max.		
CAS Access Time		13 ns max.		15 ns max.		
Fast Page Mode Cycle Time		35 ns min.		40 ns min.		
Low Power Dissipation	Operating current	432 mW max.		360 mW max.		
	Standby current	LVTTTL Level	3.6 mW max.	3.6 mW max.	3.6 mW max.	3.6 mW max.
		CMOS Level	1.8 mW max.	0.54 mW max.	1.8 mW max.	0.54 mW max.

- 1,048,576 words × 16 bit organization
- Silicon gate, CMOS, Advanced Capacitor Cell
- All input and output are LVTTTL compatible
- 4096 refresh cycles every 65.6 ms
- $1WE / 2CAS$
- Self refresh function (Low power version)
- Early write or  $\overline{OE}$  controlled write capability
- RAS-only, CAS-before-RAS, or Hidden Refresh
- Fast page Mode, Read-Modify-Write capability
- On chip substrate bias generator for high performance
- Standard and low power versions

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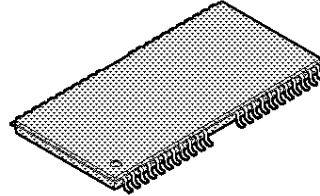
## ■ PACKAGE

42-pin plastic SOJ



(LCC-42P-M01)

50-pin plastic TSOP (II)



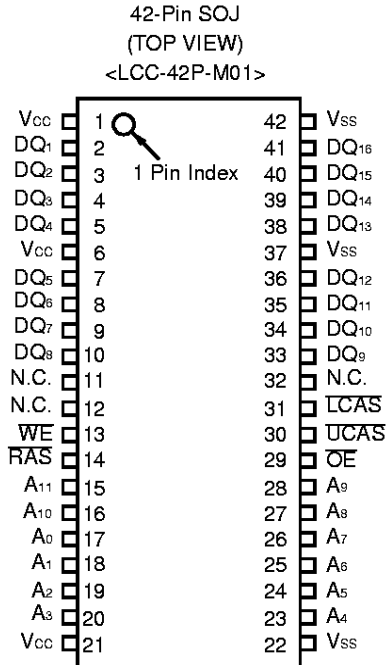
(FPT-50P-M06)  
(Normal Bend)

### Package and Ordering Information

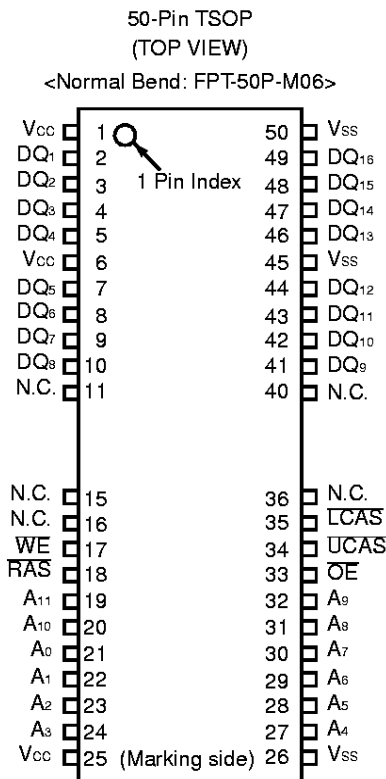
- 42-pin plastic (400 mil) SOJ, order as MB81V16160B-xxPJ
- 50-pin plastic (400 mil) TSOP-II with normal bend leads, order as MB81V16160B-xxPFTN and MB81V16160B-xxLPFTN (Low Power)

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## ■ PIN ASSIGNMENTS AND DESCRIPTIONS

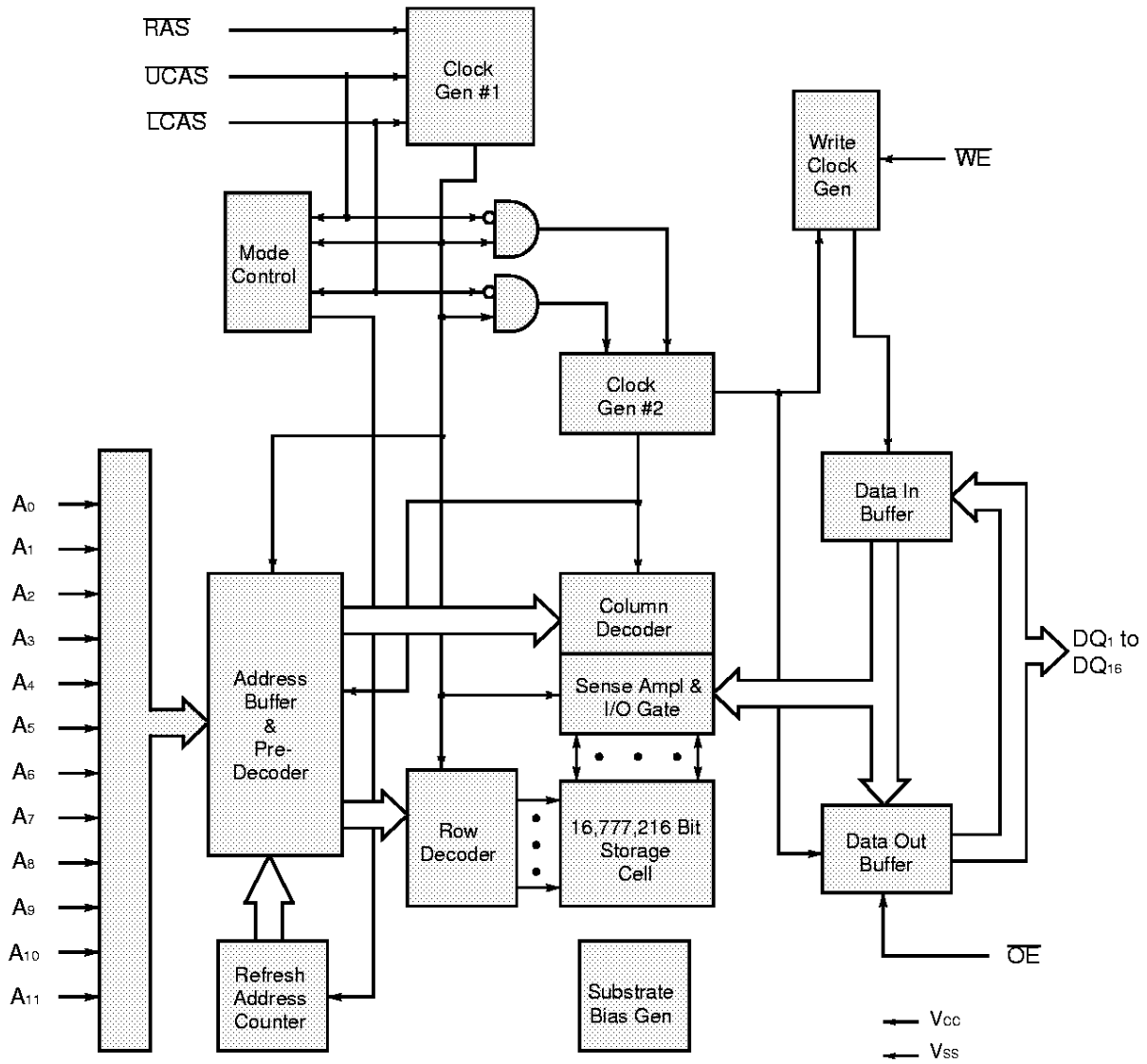


Designator	Function
A <sub>0</sub> to A <sub>11</sub>	Address inputs row : A <sub>0</sub> to A <sub>11</sub> column : A <sub>0</sub> to A <sub>7</sub> refresh : A <sub>0</sub> to A <sub>11</sub>
RAS	Row address strobe
LCAS	Lower column address strobe
UCAS	Upper column address strobe
WE	Write enable
OE	Output enable
DQ <sub>1</sub> to DQ <sub>16</sub>	Data Input/Output
V <sub>cc</sub>	+3.3 volt power supply
V <sub>ss</sub>	Circuit ground



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Fig. 1 - MB81V16160B DYNAMIC RAM - BLOCK DIAGRAM



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## FUNCTIONAL TRUTH TABLE

Operation Mode	Clock Input					Address Input		Input/Output Data				Refresh	Note
	RAS	LCAS	UCAS	WE	OE	Row	Column	DQ <sub>1</sub> to DQ <sub>8</sub>		DQ <sub>9</sub> to DQ <sub>16</sub>			
								Input	Output	Input	Output		
Standby	H	H	H	X	X	—	—	—	High-Z	—	High-Z	—	
Read Cycle	L	L H L	H L L	H	L	Valid	Valid	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes*	$t_{RCS} \geq t_{RCS}(\text{min})$
Write Cycle (Early Write)	L	L H L	H L L	L	X	Valid	Valid	Valid — Valid	High-Z	— Valid Valid	High-Z	Yes*	$t_{WCS} \geq t_{WCS}(\text{min})$
Read-Modify-Write Cycle	L	L H L	H L L	H→L	L→H	Valid	Valid	Valid — Valid	Valid High-Z Valid	— Valid Valid	High-Z Valid Valid	Yes*	
RAS-only Refresh Cycle	L	H	H	X	X	Valid	X	—	High-Z	—	High-Z	Yes	
CAS-before-RAS Refresh Cycle	L	L	L	X	X	X	X	—	High-Z	—	High-Z	Yes	$t_{CSR} \geq t_{CSR}(\text{min})$
Hidden Refresh Cycle	H→L	L H L	H L L	H→X	L	X	X	—	Valid High-Z Valid	—	High-Z Valid Valid	Yes	Previous data is kept

X : "H" or "L"

\* : It is impossible in Fast Page Mode.

## FUNCTIONAL OPERATION

### ADDRESS INPUTS

Twenty input bits are required to decode any sixteen of 16,777,216 cell addresses in the memory matrix. Since only twelve address bits (A<sub>0</sub> to A<sub>11</sub>) are available, the column and row inputs are separately strobed by LCAS or UCAS and RAS as shown in Figure 1. First, twelve row address bits are input on pins A<sub>0</sub> through A<sub>11</sub> and latched with the row address strobe (RAS) then, eight column address bits are input and latched with the column address strobe (LCAS or UCAS). Both row and column addresses must be stable on or before the falling edges of RAS and LCAS or UCAS, respectively. The address latches are of the flow-through type; thus, address information appearing after t<sub>RAH</sub> (min.) + t<sub>T</sub> is automatically treated as the column address.

### WRITE ENABLE

The read or write mode is determined by the logic state of WE. When WE is active Low, a write cycle is initiated; when WE is High, a read cycle is selected. During the read mode, input data is ignored.

### DATA INPUTS

Input data is written into memory in either of three basic ways – an early write cycle, an OE (delayed) write cycle, and a read-modify-write cycle. The falling edge of WE or LCAS / UCAS, whichever is later, serves as the input data-latch strobe. In an early write cycle, the input data of DQ<sub>1</sub> to DQ<sub>8</sub> is strobed by LCAS and DQ<sub>9</sub> to DQ<sub>16</sub> is strobed by UCAS and the setup/hold times are referenced to each LCAS and UCAS because WE goes Low before LCAS / UCAS. In a delayed write or a read-modify-write cycle, WE goes Low after LCAS / UCAS; thus, input data is strobed by WE and all setup/hold times are referenced to the write-enable signal.

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## DATA OUTPUTS

The three-state buffers are LVTTTL compatible with a fanout of one TTL loads. Polarity of the output data is identical to that of the input; the output buffers remain in the high-impedance state until the column address strobe goes Low. When a read or read-modify-write cycle is executed, valid outputs are obtained under the following conditions:

- $t_{RAC}$  : from the falling edge of  $\overline{RAS}$  when  $t_{RCD}$  (max.) is satisfied.
- $t_{CAC}$  : from the falling edge of  $\overline{CAS}$  (for DQ<sub>1</sub> to DQ<sub>8</sub>)  $\overline{UCAS}$  (for DQ<sub>9</sub> to DQ<sub>16</sub>) when  $t_{RCD}$  is greater than  $t_{RCD}$  (max.).
- $t_{AA}$  : from column address input when  $t_{RAD}$  is greater than  $t_{RAD}$  (max.).
- $t_{OEA}$  : from the falling edge of  $\overline{OE}$  when  $\overline{OE}$  is brought Low after  $t_{RAC}$ ,  $t_{CAC}$ , or  $t_{AA}$ .

The data remains valid until either  $\overline{CAS}$  /  $\overline{UCAS}$  or  $\overline{OE}$  returns to a High logic level. When an early write is executed, the output buffers remain in a high-impedance state during the entire cycle.

## FAST PAGE MODE OF OPERATION

The fast page mode of operation provides faster memory access and lower power dissipation. The fast page mode is implemented by keeping the same row address and strobing in successive column addresses. To satisfy these conditions,  $\overline{RAS}$  is held Low for all contiguous memory cycles in which row addresses are common. For each fast page of memory, any of 256 × 16 bits can be accessed and, when multiple MB81V16160Bs are used,  $\overline{CAS}$  is decoded to select the desired memory fast page. Fast page mode operations need not be addressed sequentially and combinations of read, write, and/or read-modify-write cycles are permitted.

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## ■ ABSOLUTE MAXIMUM RATINGS (See WARNING)

Parameter	Symbol	Value	Unit
Voltage at Any Pin Relative to V <sub>SS</sub>	V <sub>IN</sub> , V <sub>OUT</sub>	-0.5 to +4.6	V
Voltage of V <sub>CC</sub> Supply Relative to V <sub>SS</sub>	V <sub>CC</sub>	-0.5 to +4.6	V
Power Dissipation	P <sub>D</sub>	1.0	W
Short Circuit Output Current	—	-50 to +50	mA
Operating Temperature	T <sub>OP</sub>	0 to +70	°C
Storage Temperature	T <sub>STG</sub>	-55 to +125	°C

**WARNING:** Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## ■ RECOMMENDED OPERATING CONDITIONS

Parameter	Notes	Symbol	Min.	Typ.	Max.	Unit	Ambient Operating Temp.
Supply Voltage	*1	V <sub>CC</sub>	3.0	3.3	3.6	V	0°C to +70°C
		V <sub>SS</sub>	0	0	0		
Input High Voltage, All Inputs	*1	V <sub>IH</sub>	2.0	—	V <sub>CC</sub> +0.3	V	
Input Low Voltage, All Inputs*	*1	V <sub>IL</sub>	-0.3	—	0.8	V	

\* : Undershoots of up to -2.0 volts with a pulse width not exceeding 20 ns are acceptable.

**WARNING:** Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representative beforehand.

## ■ CAPACITANCE

(T<sub>A</sub> = 25°C, f = 1 MHz)

Parameter	Symbol	Max.	Unit
Input Capacitance, A <sub>0</sub> to A <sub>11</sub>	C <sub>IN1</sub>	6	pF
Input Capacitance, RAS, LCAS, UCAS, WE, OE	C <sub>IN2</sub>	6	pF
Input/Output Capacitance, DQ <sub>1</sub> to DQ <sub>16</sub>	C <sub>DQ</sub>	7	pF

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## ■ DC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Note 3

Parameter	Notes	Symbol	Conditions	Value				Unit
				Min.	Typ.	Max.		
						Std power	Low power	
Output High Voltage	*1	V <sub>OH</sub>	I <sub>OH</sub> = -2.0 mA	2.4	—	—	—	V
Output Low Voltage	*1	V <sub>OL</sub>	I <sub>OL</sub> = +2.0 mA	—	—	0.4	0.4	
Input Leakage Current (Any Input)		I <sub>IL</sub>	0 V ≤ V <sub>IN</sub> ≤ 3.6 V; 3.0 V ≤ V <sub>CC</sub> ≤ 3.6 V; V <sub>SS</sub> = 0 V; All other pins not under test = 0 V	-10	—	10	10	μA
Output Leakage Current		I <sub>DO(L)</sub>	0 V ≤ V <sub>OUT</sub> ≤ 3.6 V; 3.0 V ≤ V <sub>CC</sub> ≤ 3.6 V; Data out disabled	-10	—	10	10	
Operating Current (Average Power Supply Current)	*2	MB81V16160B -50/50L	RAS & LCAS, UCAS cycling; trc = min.	—	—	120	120	mA
		MB81V16160B -60/60L				100	100	
Standby Current (Power Supply Current)	*2	LVTTL Level	RAS = LCAS, UCAS = V <sub>IH</sub>	—	—	1.0	1.0	mA
		CMOS Level	RAS = LCAS, UCAS ≥ V <sub>CC</sub> - 0.2 V			500	150	
Refresh Current#1 (Average Power Supply Current)	*2	MB81V16160B -50/50L	LCAS, UCAS = V <sub>IH</sub> , RAS cycling; trc = min.	—	—	120	120	mA
		MB81V16160B -60/60L				100	100	
Fast Page Mode Current	*2	MB81V16160B -50/50L	RAS = V <sub>IL</sub> , LCAS, UCAS cycling; tpc = min.	—	—	120	120	mA
		MB81V16160B -60/60L				100	100	
Refresh Current#2 (Average Power Supply Current)	*2	MB81V16160B -50/50L	RAS cycling; CAS-before-RAS; trc = min.	—	—	120	120	mA
		MB81V16160B -60/60L				100	100	
Battery Backup Current (Average Power Supply Current)	*2	MB81V16160B -50/60	RAS cycling; CAS-before-RAS; trc = 16 μs trAS = min. to 300 ns V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IL</sub> ≤ 0.2 V	—	—	800	—	μA
		MB81V16160B -50L/60L	RAS cycling; CAS-before-RAS; trc = 32 μs trAS = min. to 300 ns V <sub>IH</sub> ≥ V <sub>CC</sub> - 0.2 V, V <sub>IL</sub> ≤ 0.2 V			—	300	
Refresh Current#3 (Average Power Supply Current)		MB81V16160B -50L/60L	RAS = V <sub>IL</sub> , CAS = V <sub>IL</sub> Self refresh;	—	—	—	250	μA



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## ■ AC CHARACTERISTICS

(At recommended operating conditions unless otherwise noted.) Notes 3, 4, 5

No.	Parameter	Notes	Symbol	MB81V16160B -50/50L		MB81V16160B -60/60L		Unit
				Min.	Max.	Min.	Max.	
1	Time Between Refresh	Std power	t <sub>REF</sub>	—	65.6	—	65.6	ms
		Low power		—	128	—	128	
2	Random Read/Write Cycle Time		t <sub>RC</sub>	90	—	110	—	ns
3	Read-Modify-Write Cycle Time		t <sub>RWC</sub>	126	—	150	—	ns
4	Access Time from $\overline{\text{RAS}}$	*6,9	t <sub>RAC</sub>	—	50	—	60	ns
5	Access Time from $\overline{\text{CAS}}$	*7,9	t <sub>CAC</sub>	—	13	—	15	ns
6	Column Address Access Time	*8,9	t <sub>AA</sub>	—	25	—	30	ns
7	Output Hold Time		t <sub>OH</sub>	3	—	3	—	ns
8	Output Buffer Turn On Delay Time		t <sub>ON</sub>	0	—	0	—	ns
9	Output Buffer Turn off Delay Time	*10	t <sub>OFF</sub>	—	13	—	15	ns
10	Transition Time		t <sub>T</sub>	3	50	3	50	ns
11	$\overline{\text{RAS}}$ Precharge Time		t <sub>RP</sub>	30	—	40	—	ns
12	$\overline{\text{RAS}}$ Pulse Width		t <sub>RAS</sub>	50	100000	60	100000	ns
13	$\overline{\text{RAS}}$ Hold Time		t <sub>RSH</sub>	13	—	15	—	ns
14	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time		t <sub>CRP</sub>	0	—	0	—	ns
15	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	*11,12	t <sub>RC</sub> D	17	37	20	45	ns
16	$\overline{\text{CAS}}$ Pulse Width		t <sub>CAS</sub>	13	—	15	—	ns
17	$\overline{\text{CAS}}$ Hold Time		t <sub>CSH</sub>	50	—	60	—	ns
18	$\overline{\text{CAS}}$ Precharge Time (Normal)	*19	t <sub>CPN</sub>	7	—	10	—	ns
19	Row Address Setup Time		t <sub>ASR</sub>	0	—	0	—	ns
20	Row Address Hold Time		t <sub>RAH</sub>	7	—	10	—	ns
21	Column Address Setup Time		t <sub>ASC</sub>	0	—	0	—	ns
22	Column Address Hold Time		t <sub>CAH</sub>	7	—	10	—	ns
23	Column Address Hold Time from $\overline{\text{RAS}}$		t <sub>AR</sub>	24	—	30	—	ns
24	$\overline{\text{RAS}}$ to Column Address Delay Time	*13	t <sub>RAD</sub>	12	25	15	30	ns
25	Column Address to $\overline{\text{RAS}}$ Lead Time		t <sub>RAL</sub>	25	—	30	—	ns
26	Column Address to $\overline{\text{CAS}}$ Lead Time		t <sub>CAL</sub>	25	—	30	—	ns
27	Read Command and Setup Time		t <sub>RCS</sub>	0	—	0	—	ns
28	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	*14	t <sub>RRH</sub>	0	—	0	—	ns
29	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	*14	t <sub>RCH</sub>	0	—	0	—	ns
30	Write Command Setup Time	*15	t <sub>WCS</sub>	0	—	0	—	ns

(Continued)

# MB81V16160B-50/-60/-50L/-60L

(Continued)

No.	Parameter	Notes	Symbol	MB81V16160B -50/50L		MB81V16160B -60/60L		Unit
				Min.	Max.	Min.	Max.	
31	Write Command Hold Time		t <sub>WCH</sub>	7	—	10	—	ns
32	Write Command Hold Time from RAS		t <sub>WCR</sub>	24	—	30	—	ns
33	WE Pulse Width		t <sub>WP</sub>	7	—	10	—	ns
34	Write Command to RAS Lead Time		t <sub>RWL</sub>	13	—	15	—	ns
35	Write Command to CAS Lead Time		t <sub>CWL</sub>	13	—	15	—	ns
36	DIN Setup Time		t <sub>DS</sub>	0	—	0	—	ns
37	DIN Hold Time		t <sub>DH</sub>	7	—	10	—	ns
38	Data Hold Time from RAS		t <sub>DHR</sub>	24	—	30	—	ns
39	RAS to WE Delay Time	*20	t <sub>RWD</sub>	68	—	80	—	ns
40	CAS to WE Delay Time	*20	t <sub>CWD</sub>	31	—	35	—	ns
41	Column Address to WE Delay Time	*20	t <sub>AWD</sub>	43	—	50	—	ns
42	RAS Precharge Time to CAS Active Time (Refresh cycles)		t <sub>RPC</sub>	5	—	5	—	ns
43	CAS Setup Time for CAS-before-RAS Refresh		t <sub>CSR</sub>	0	—	0	—	ns
44	CAS Hold Time for CAS-before-RAS Refresh		t <sub>CHR</sub>	10	—	10	—	ns
45	Access Time from OE	*9	t <sub>OE A</sub>	—	13	—	15	ns
46	Output Buffer Turn Off Delay from OE	*10	t <sub>OE Z</sub>	—	13	—	15	ns
47	OE to RAS Lead Time for Valid Data		t <sub>OE L</sub>	5	—	5	—	ns
48	OE Hold Time Referenced to WE	*16	t <sub>OE H</sub>	5	—	5	—	ns
49	OE to Data In Delay Time		t <sub>OE D</sub>	13	—	15	—	ns
50	CAS to Data In Delay Time		t <sub>CDD</sub>	13	—	15	—	ns
51	DIN to CAS Delay Time	*17	t <sub>DZC</sub>	0	—	0	—	ns
52	DIN to OE Delay Time	*17	t <sub>DZO</sub>	0	—	0	—	ns
53	Fast Page Mode RAS Pulse Width		t <sub>RASP</sub>	—	100000	—	100000	ns
54	Fast Page Mode Read/Write Cycle Time		t <sub>PC</sub>	35	—	40	—	ns
55	Fast Page Mode Read-Modify-Write Cycle Time		t <sub>PRWC</sub>	71	—	80	—	ns
56	Access Time from CAS Precharge	*9,18	t <sub>CPA</sub>	—	30	—	35	ns
57	Fast Page Mode CAS Precharge Time		t <sub>CP</sub>	7	—	10	—	ns
58	Fast Page Mode RAS Hold Time from CAS Precharge		t <sub>RHCP</sub>	30	—	35	—	ns
59	Fast Page Mode CAS Precharge to WE Delay Time		t <sub>CPWD</sub>	48	—	55	—	ns

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- Notes:**
- \*1. Referenced to  $V_{SS}$ .
  - \*2.  $I_{CC}$  depends on the output load conditions and cycle rates; the specified values are obtained with the output open.  
 $I_{CC}$  depends on the number of address change as  $\overline{RAS} = V_{IL}$ ,  $\overline{UCAS} = V_{IH}$ ,  $\overline{LCAS} = V_{IH}$  and  $V_{IL} > -0.3$  V.  
 $I_{CC1}$ ,  $I_{CC3}$ ,  $I_{CC4}$  and  $I_{CC5}$  are specified at one time of address change during  $\overline{RAS} = V_{IL}$  and  $\overline{UCAS} = V_{IH}$ ,  $\overline{LCAS} = V_{IH}$ .  
 $I_{CC2}$  is specified during  $\overline{RAS} = V_{IH}$  and  $V_{IL} > -0.3$  V.  
 $I_{CC6}$  is measured on condition that all address signals are fixed steady state.
  - \*3. An initial pause ( $\overline{RAS} = \overline{CAS} = V_{IH}$ ) of 200 $\mu$ s is required after power-up followed by any eight  $\overline{RAS}$ -only cycles before proper device operation is achieved. In case of using internal refresh counter, a minimum of eight  $\overline{CAS}$ -before- $\overline{RAS}$  initialization cycles instead of 8  $\overline{RAS}$  cycles are required.
  - \*4. AC characteristics assume  $t_T = 5$  ns.
  - \*5. Input voltage levels are 0 V and 3.0 V, and input reference levels are  $V_{IH}(\min)$  and  $V_{IL}(\max)$  for measuring timing of input signals. Also, the transition time ( $t_T$ ) is measured between  $V_{IH}(\min)$  and  $V_{IL}(\max)$ .  
 The output reference levels are  $V_{OH} = 2.0$  V and  $V_{OL} = 0.8$  V.
  - \*6. Assumes that  $t_{RCD} \leq t_{RCD}(\max)$ ,  $t_{RAD} \leq t_{RAD}(\max)$ . If  $t_{RCD}$  is greater than the maximum recommended value shown in this table,  $t_{RAC}$  will be increased by the amount that  $t_{RCD}$  exceeds the value shown. Refer to Fig.2 and 3.
  - \*7. If  $t_{RCD} \geq t_{RCD}(\max)$ ,  $t_{RAD} \geq t_{RAD}(\max)$ , and  $t_{ASC} \geq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{CAC}$ .
  - \*8. If  $t_{RAD} \geq t_{RAD}(\max)$  and  $t_{ASC} \leq t_{AA} - t_{CAC} - t_T$ , access time is  $t_{AA}$ .
  - \*9. Measured with a load equivalent to one TTL load and 100 pF.
  - \*10.  $t_{OFF}$  and  $t_{OEZ}$  are specified that output buffer change to high-impedance state.
  - \*11. Operation within the  $t_{RCD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RCD}(\max)$  is specified as a reference point only; if  $t_{RCD}$  is greater than the specified  $t_{RCD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  - \*12.  $t_{RCD}(\min) = t_{RAH}(\min) + 2t_T + t_{ASC}(\min)$ .
  - \*13. Operation within the  $t_{RAD}(\max)$  limit ensures that  $t_{RAC}(\max)$  can be met.  $t_{RAD}(\max)$  is specified as a reference point only; if  $t_{RAD}$  is greater than the specified  $t_{RAD}(\max)$  limit, access time is controlled exclusively by  $t_{CAC}$  or  $t_{AA}$ .
  - \*14. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a read cycle.
  - \*15.  $t_{WCS}$  is specified as a reference point only. If  $t_{WCS} \geq t_{WCS}(\min)$  the data output pin will remain High-Z state through entire cycle.
  - \*16. Assumes that  $t_{WCS} < t_{WCS}(\min)$ .
  - \*17. Either  $t_{DZC}$  or  $t_{DZO}$  must be satisfied.
  - \*18.  $t_{CPA}$  is access time from the selection of a new column address (that is caused by changing both  $\overline{UCAS}$  and  $\overline{LCAS}$  from "L" to "H"). Therefore, if  $t_{CP}$  is long,  $t_{CPA}$  is longer than  $t_{CPA}(\max)$ .
  - \*19. Assumes that  $\overline{CAS}$ -before- $\overline{RAS}$  refresh.
  - \*20.  $t_{WCS}$ ,  $t_{CWD}$ ,  $t_{RWD}$  and  $t_{AWD}$  are not restrictive operating parameters. They are included in the data sheet as an electrical characteristic only. If  $t_{WCS} > t_{WCS}(\min)$ , the cycle is an early write cycle and DQ pin will maintain high-impedance state through out the entire cycle. If  $t_{CWD} > t_{CWD}(\min)$ ,  $t_{RWD} > t_{RWD}(\min)$ , and  $t_{AWD} > t_{AWD}(\min)$ , the cycle is a read-modify-write cycle and data from the selected cell will appear at the DQ pin. If neither of the above conditions is satisfied, the cycle is a delayed write cycle and invalid data will appear the DQ pin, and write operation can be executed by satisfying  $t_{RWL}$ ,  $t_{CWL}$ , and  $t_{RAL}$  specifications.

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Fig. 2 –  $t_{RAC}$  vs.  $t_{RCD}$

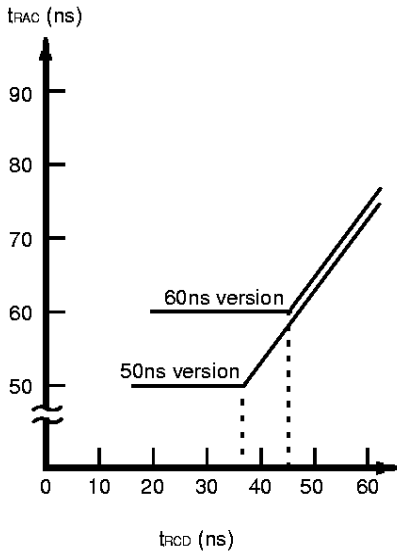


Fig. 3 –  $t_{RAC}$  vs.  $t_{RAD}$

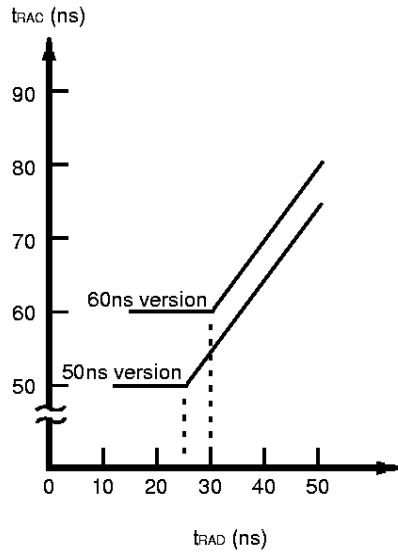
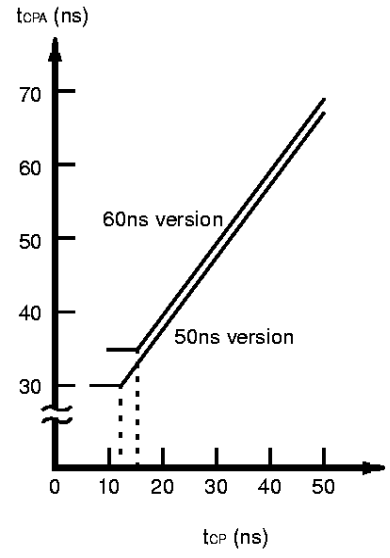


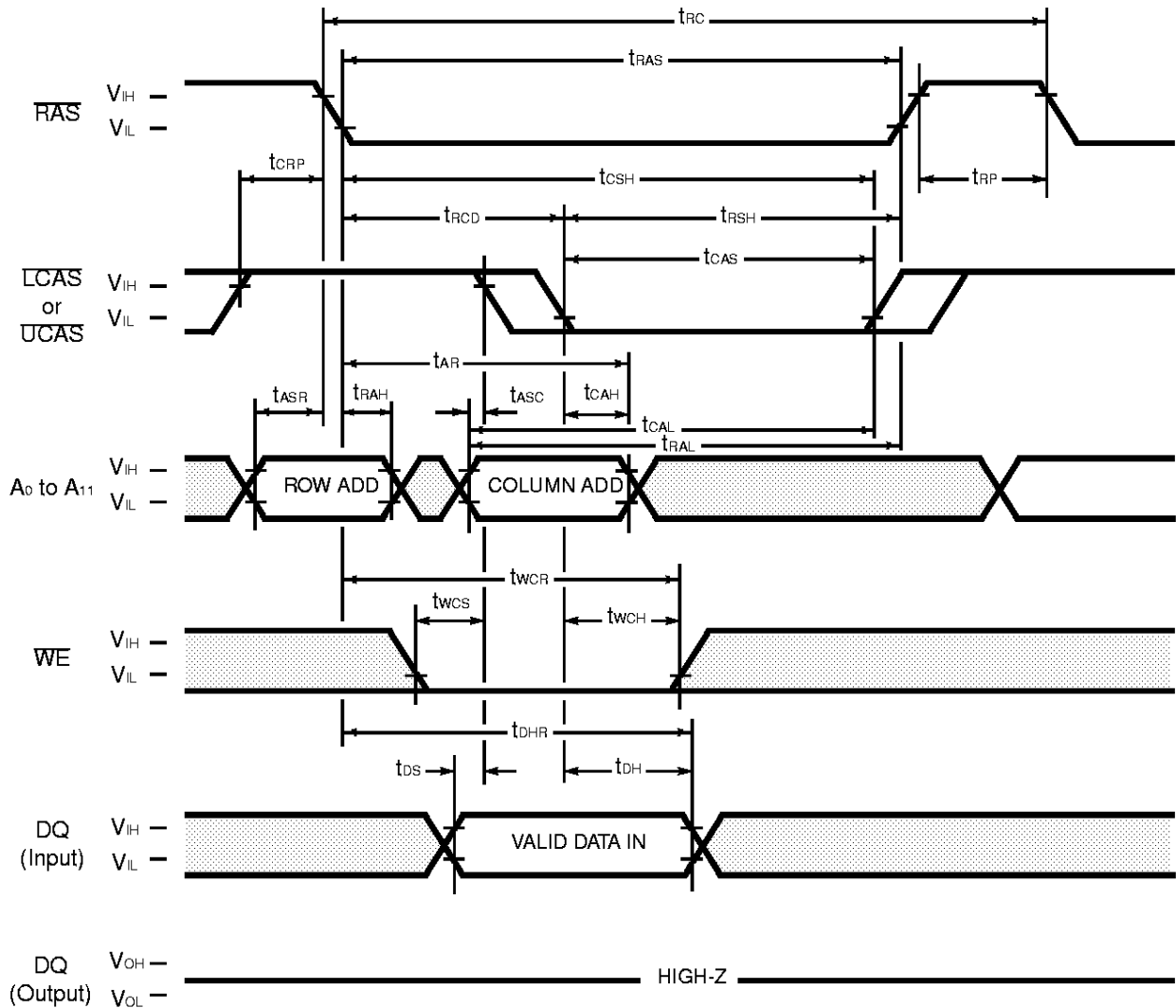
Fig. 4 –  $t_{CPA}$  vs.  $t_{CP}$







# MB81V16160B-50/-60/-50L/-60L

Fig. 6 – EARLY WRITE CYCLE ( $\overline{OE}$  = “H” or “L”)



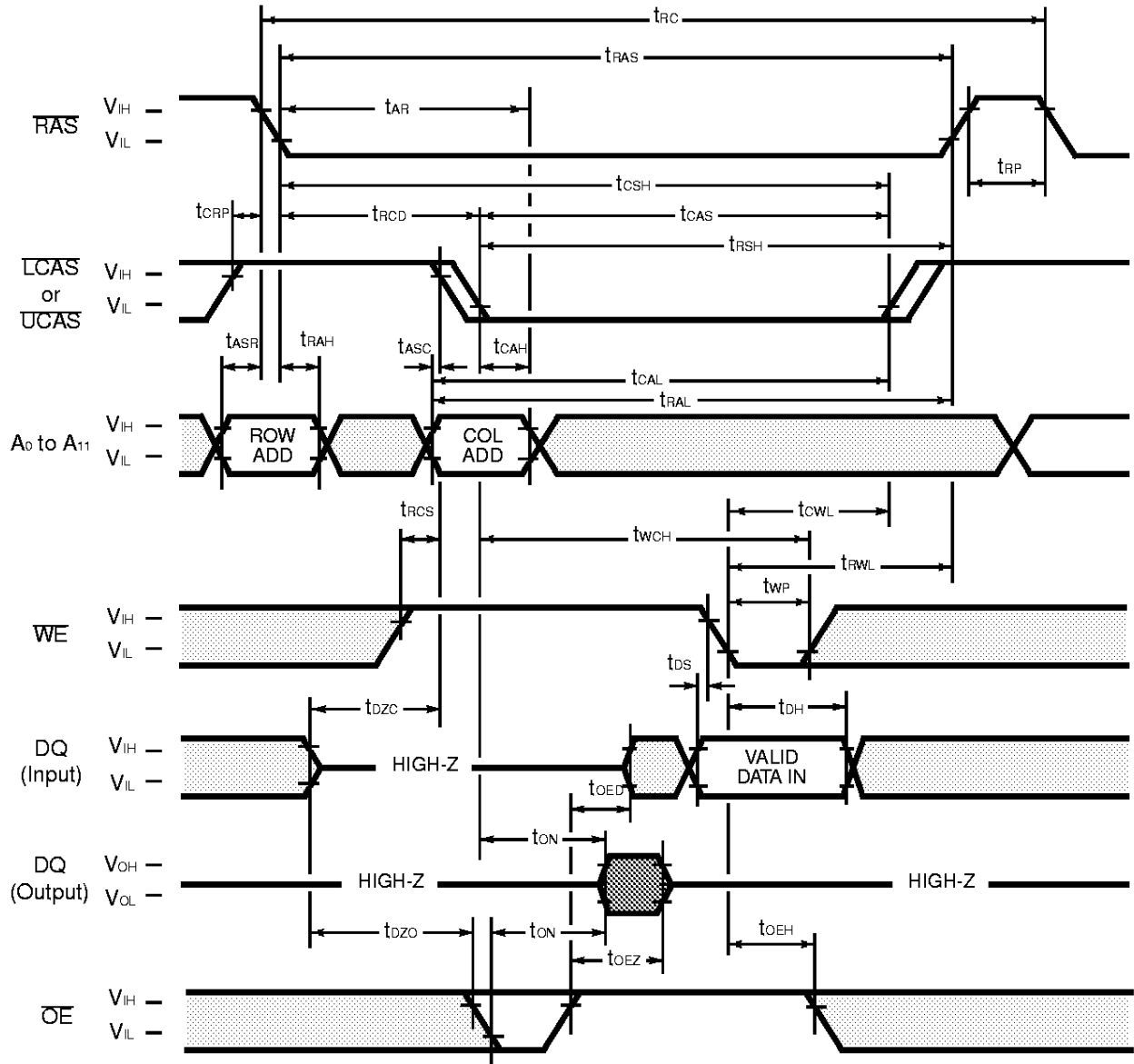
 "H" or "L" level (excluding Address and DQ)  
 "H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

**DESCRIPTION**

A write cycle is similar to a read cycle except  $\overline{WE}$  is set to a Low state and  $\overline{OE}$  is an "H" or "L" signal. A write cycle can be implemented in either of three ways – early write, delayed write, or read-modify-write. During all write cycles, timing parameters  $t_{RWL}$ ,  $t_{CWL}$ ,  $t_{RAL}$  and  $t_{CAL}$  must be satisfied. In the early write cycle shown above  $t_{wCS}$  satisfied, data on the DQ pins are latched with the falling edge of LCAS or UCAS and written into memory.

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Fig. 7 – DELAYED WRITE CYCLE



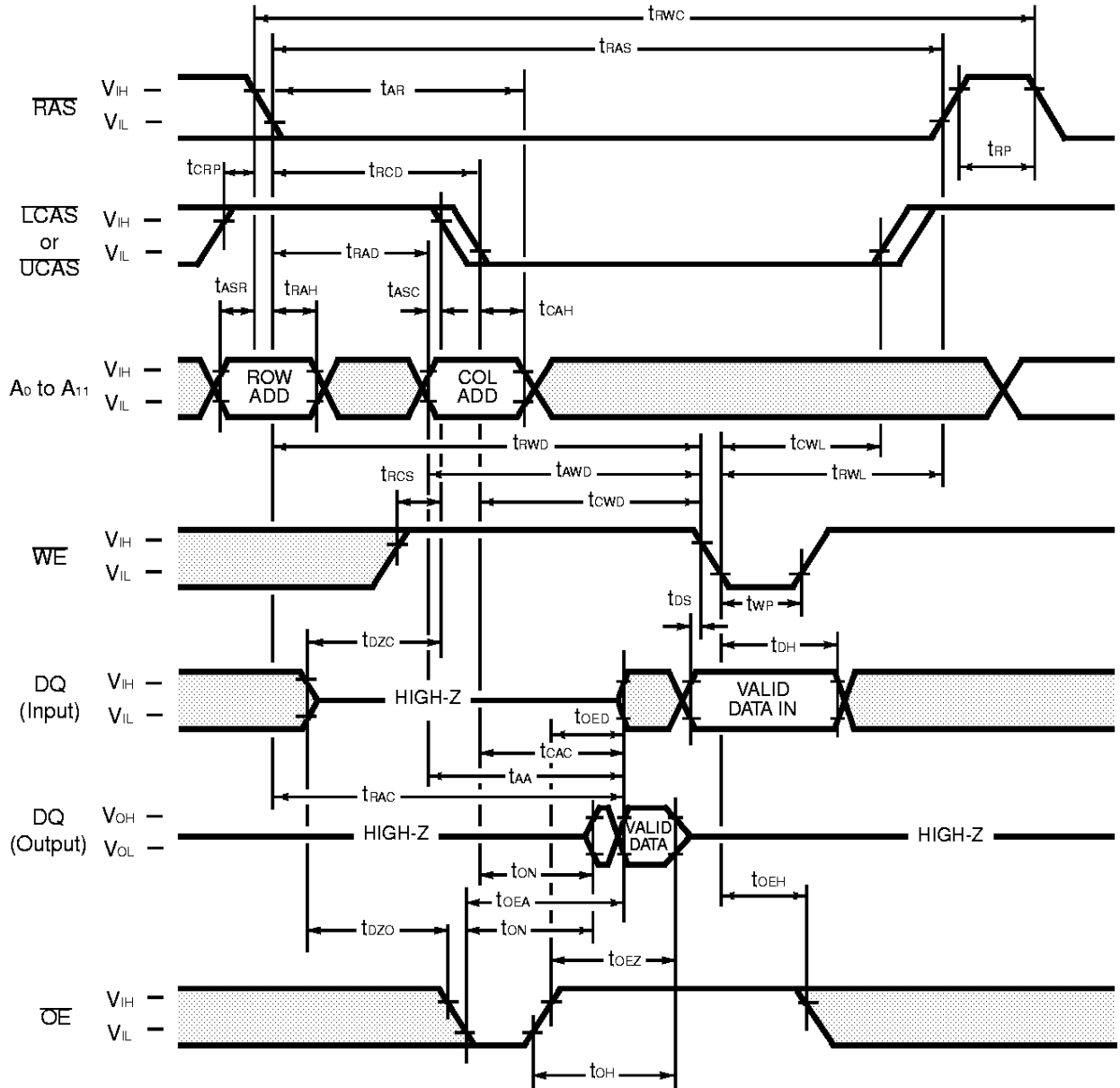
- "H" or "L" level (excluding Address and DQ)
- "H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)
- Invalid Data

**DESCRIPTION**

In the delayed write cycle,  $t_{wCS}$  is not satisfied; thus, the data on the DQ pins is latched with the falling edge of WE and written into memory. The Output Enable (OE) signal must be changed from Low to High before WE goes Low ( $t_{OED} + t_t + t_{DS}$ ).

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Fig. 8 – READ-MODIFY-WRITE CYCLE



"H" or "L" level (excluding Address and DQ)  
 "H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

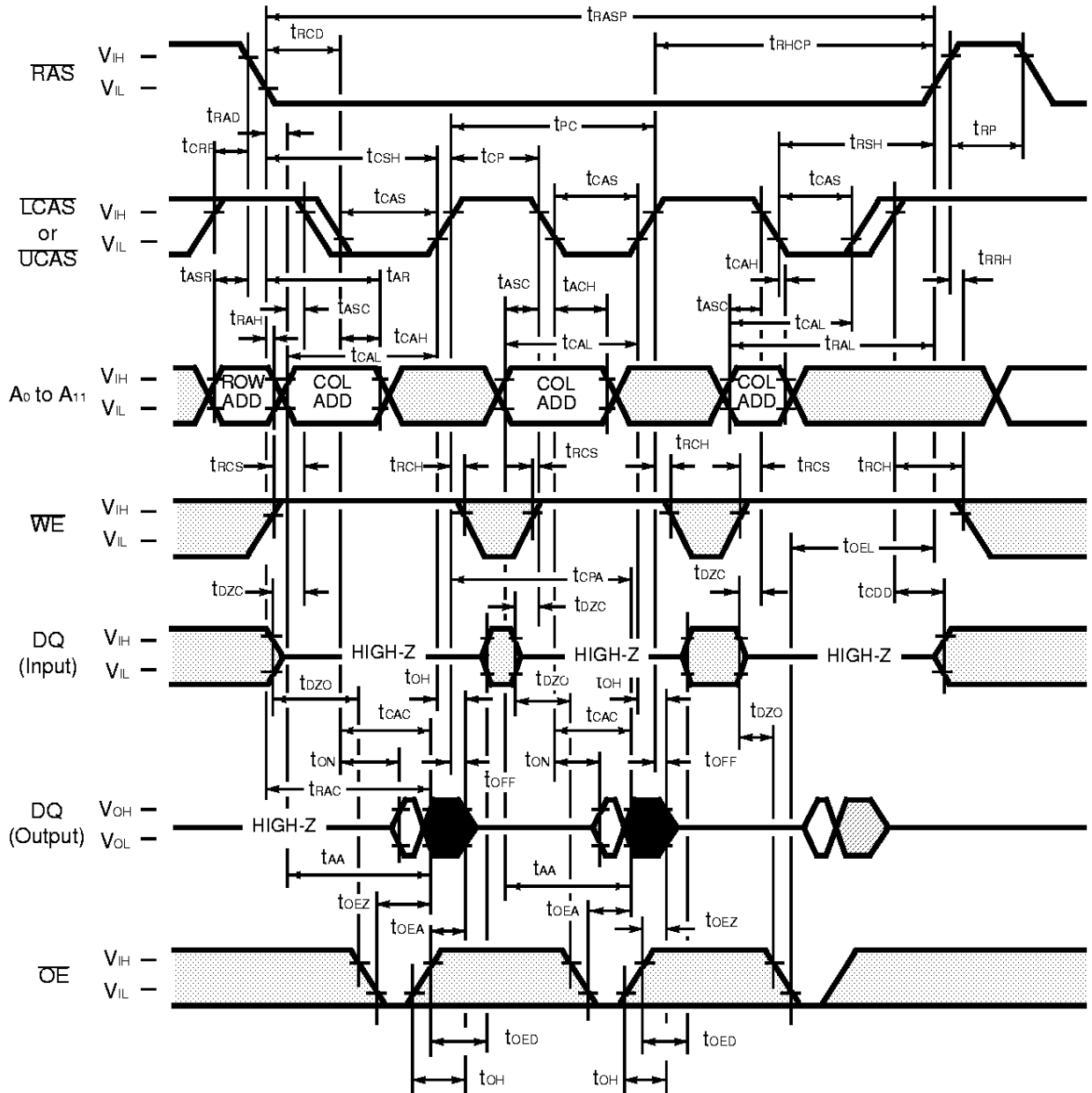
**DESCRIPTION**




The read-modify-write cycle is executed by changing WE from High to Low after the data appears on the DQ pins. In the read-modify-write cycle, OE must be changed from Low to High after the memory access time.



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Fig. 9 – FAST PAGE MODE READ CYCLE



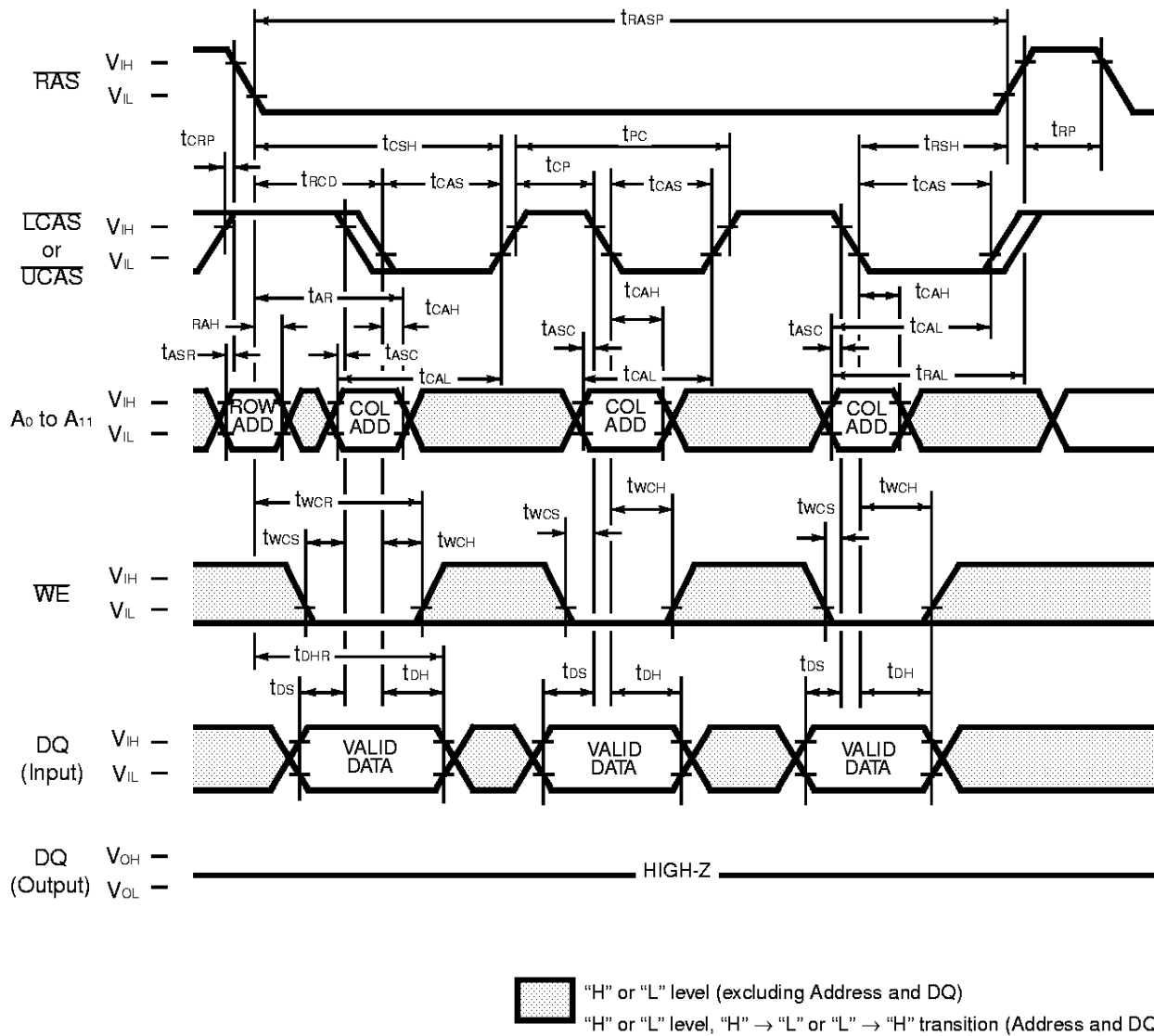
-  "H" or "L" level (excluding Address and DQ)
-  "H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)
-  Valid Data

**DESCRIPTION**

The fast page mode of operation permits faster successive memory operations at multiple column locations of the same row address. This operation is performed by strobing in the row address and maintaining RAS at a Low level and WE at a High level during all successive memory cycles in which the row address is latched. The address time is determined by t<sub>CAC</sub>, t<sub>AA</sub>, t<sub>CPA</sub>, or t<sub>OEa</sub>, whichever one is the latest in occurring.

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Fig. 10 – FAST PAGE MODE EARLY WRITE CYCLE ( $\overline{OE}$  = “H” or “L”)



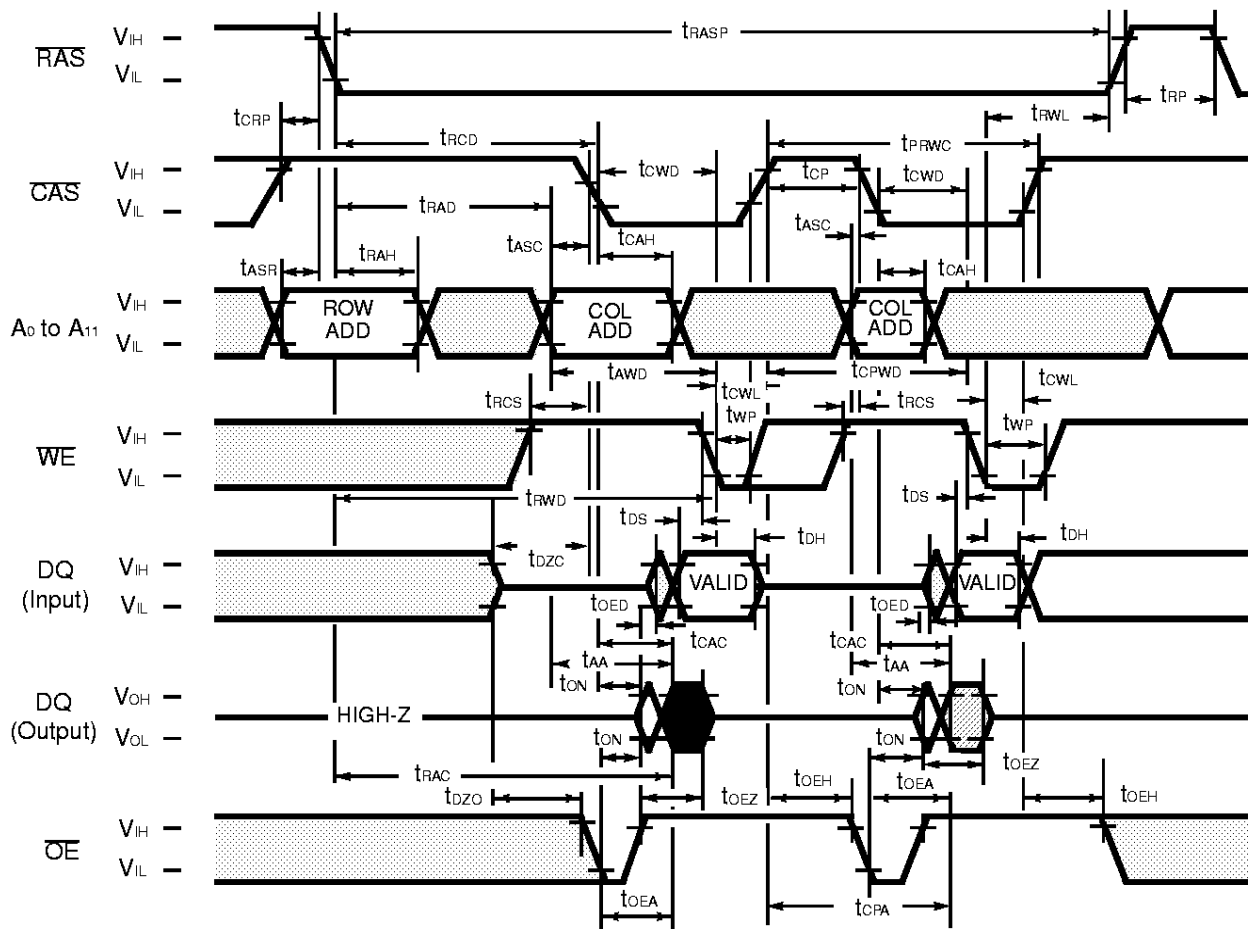
## DESCRIPTION

The fast page mode early write cycle is executed in the same manner as the fast page mode read cycle except the states of WE and  $\overline{OE}$  are reversed. Data appearing on the DQ<sub>1</sub> to DQ<sub>8</sub> is latched on the falling edge of LCAS and one appearing on the DQ<sub>9</sub> to DQ<sub>16</sub> is latched on the falling edge of UCAS and the data is written into the memory. During the fast page mode early write cycle, including the delayed ( $\overline{OE}$ ) write and read-modify-write cycles, t<sub>OWL</sub> must be satisfied.



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Fig. 12 – FAST PAGE MODE READ MODIFY WRITE CYCLE



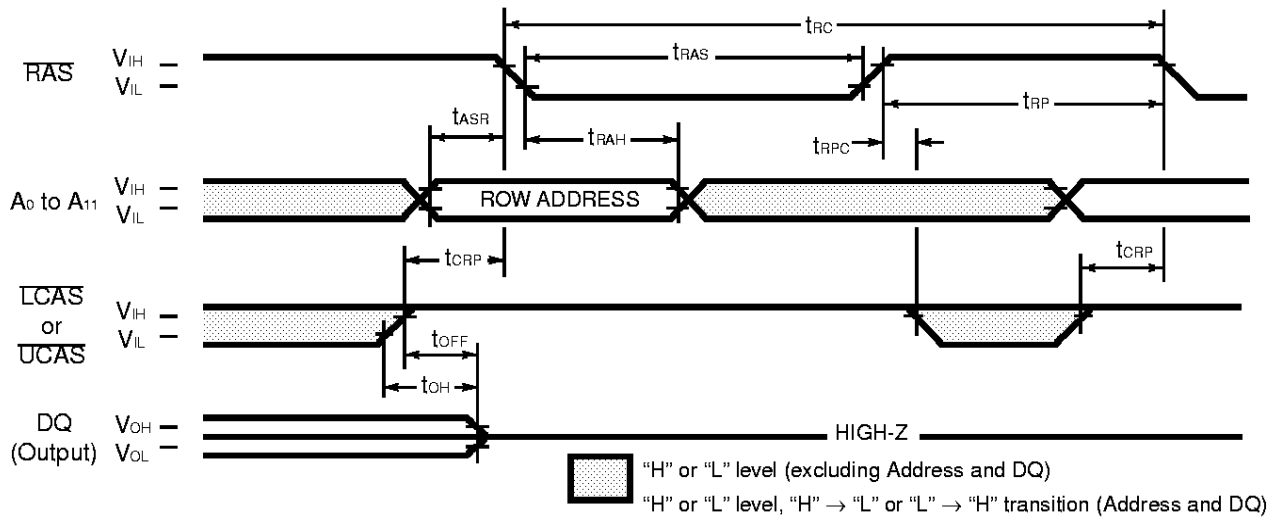
- "H" or "L" level (excluding Address and DQ)
- "H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)
- Valid Data

**DESCRIPTION**

During the fast page mode of operation, the read-modify-write cycle can be executed by switching **WE** from High to Low after input data appears at the DQ pins during a normal cycle.

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Fig. 13 – RAS-ONLY REFRESH ( $\overline{WE} = \overline{OE} = \text{"H"} \text{ or } \text{"L"}\text{"}$ )

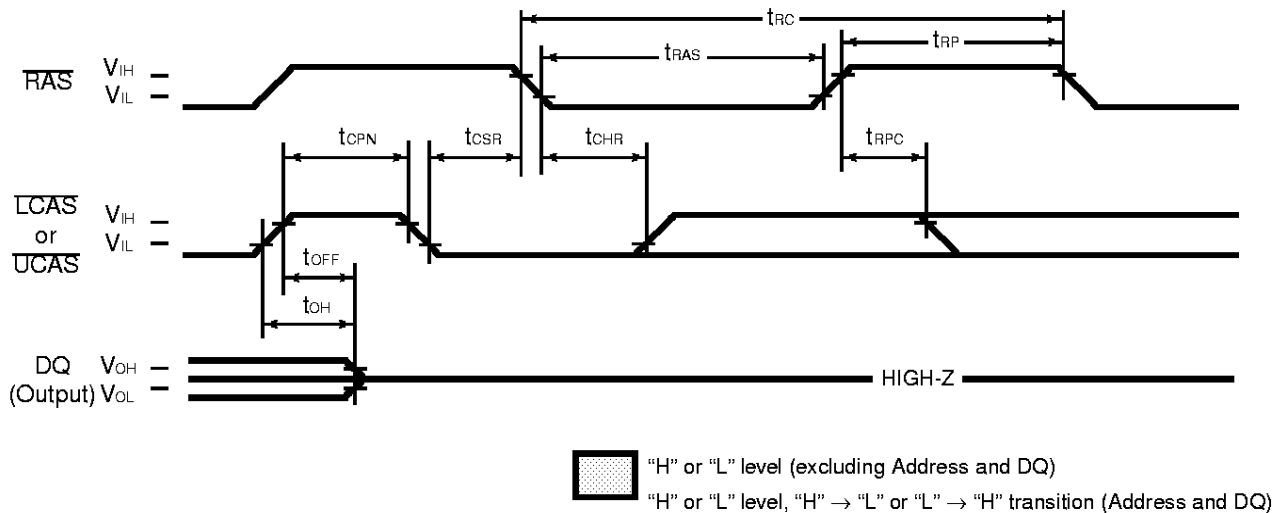


**DESCRIPTION**

Refresh of RAM memory cells is accomplished by performing a read, a write, or a read-modify-write cycle at each of 4096 row addresses every 65.6-milliseconds. Three refresh modes are available: RAS-only refresh, CAS-before-RAS refresh, and hidden refresh.

RAS-only refresh is performed by keeping RAS Low and LCAS and UCAS High throughout the cycle; the row address to be refreshed is latched on the falling edge of RAS. During RAS-only refresh, DQ pins are kept in a high-impedance state.

Fig. 14 – CAS-BEFORE-RAS REFRESH (ADDRESSES =  $\overline{WE} = \overline{OE} = \text{"H"} \text{ or } \text{"L"}\text{"}$ )

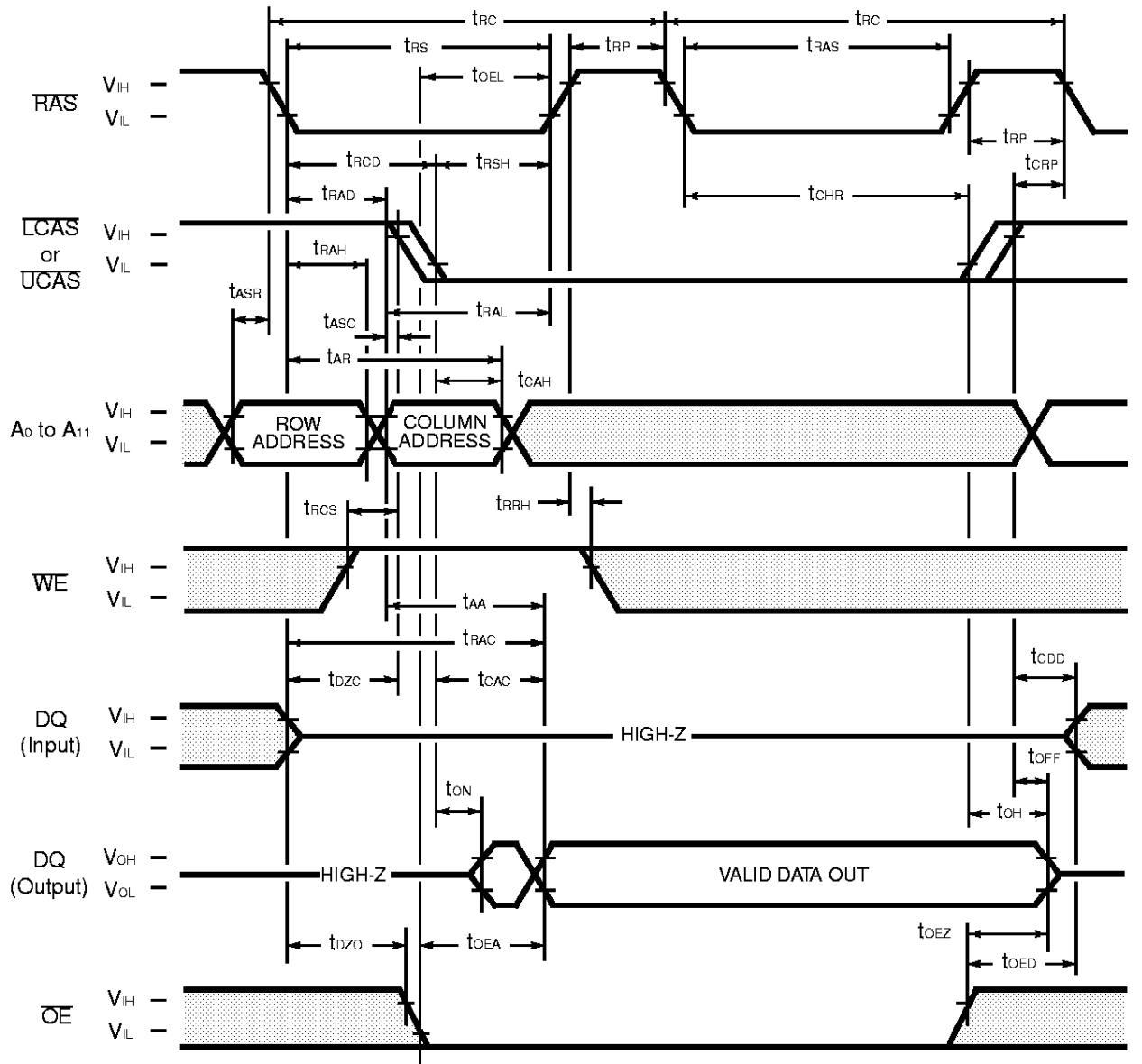



**DESCRIPTION**

CAS-before-RAS refresh is an on-chip refresh capability that eliminates the need for external refresh addresses. If LCAS or UCAS is held Low for the specified setup time (tCSR) before RAS goes Low, the on-chip refresh control clock generators and refresh address counter are enabled. An internal refresh operation automatically occurs and the refresh address counter is internally incremented in preparation for the next CAS-before-RAS refresh operation.

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Fig. 15 – HIDDEN REFRESH CYCLE




 "H" or "L" level (excluding Address and DQ)  
 "H" or "L" level, "H" → "L" or "L" → "H" transition (Address and DQ)

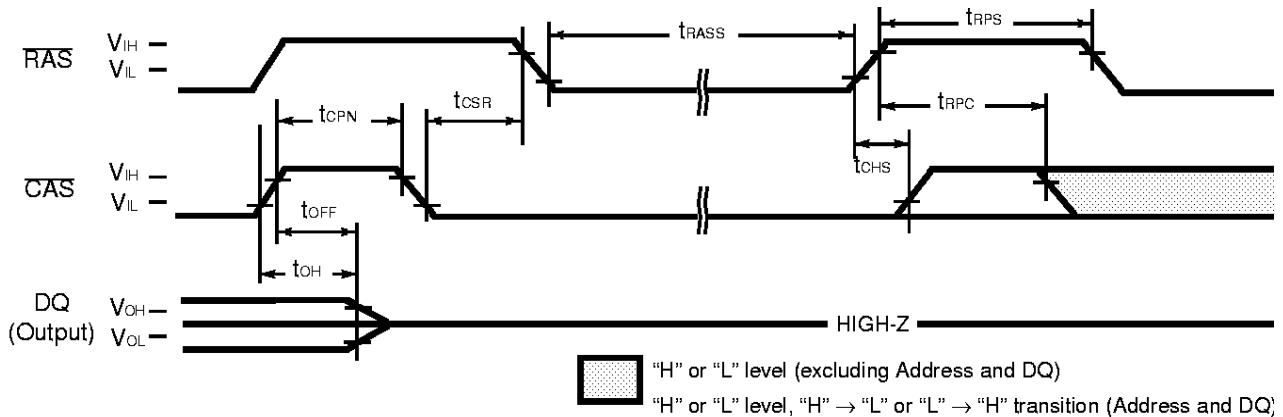
**DESCRIPTION**

A hidden refresh cycle may be performed while maintaining the latest valid data at the output by extending the active time of  $\overline{LCAS}$  or  $\overline{UCAS}$  and cycling  $\overline{RAS}$ . The refresh row address is provided by the on-chip refresh address counter. This eliminates the need for the external row address that is required by DRAMs that do not have  $\overline{CAS}$ -before- $\overline{RAS}$  refresh capability.



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Fig. 17 – SELF REFRESH CYCLE ( $A_0$  to  $A_{11} = \overline{WE} = \overline{OE} = \text{“H” or “L”}$ )



(At recommended operating conditions unless otherwise noted.)

No.	Parameter	Symbol	MB81V16160B-50L		MB81V16160B-60L		Unit
			Min.	Max.	Min.	Max.	
65	RAS Pulse Width	$t_{RASS}$	100	—	100	—	$\mu s$
66	RAS Precharge Time	$t_{RPS}$	90	—	110	—	ns
67	CAS Hold Time	$t_{CHS}$	-50	—	-50	—	ns

Note: Assumes Self Refresh cycle only.

## DESCRIPTION

The self refresh cycle provides a refresh operation without external clock and external Address. Self refresh control circuit on chip is operated in the self refresh cycle and refresh operation can be automatically executed using internal refresh address counter.

If  $\overline{CAS}$  goes to "L" before  $\overline{RAS}$  goes to "L" (CBR) and the condition of  $\overline{CAS}$  "L" and  $\overline{RAS}$  "L" is kept for term of  $t_{RASS}$  (more than 100  $\mu s$ ), the device can enter the self refresh cycle. Following that, refresh operation is automatically executed at fixed intervals using internal refresh address counter during " $\overline{RAS}=\text{L}$ " and " $\overline{CAS}=\text{L}$ ".

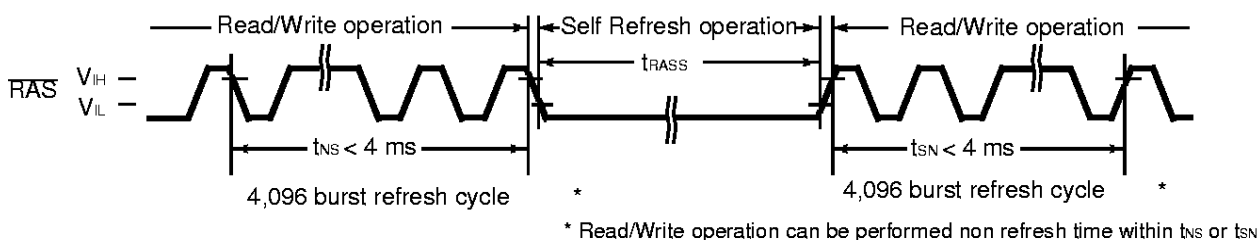
Exit from self refresh cycle is performed by toggling  $\overline{RAS}$  and  $\overline{CAS}$  to "H" with specified  $t_{CHS}$  min. In this time,  $\overline{RAS}$  must be kept "H" with specified  $t_{RPS}$  min.

Using self refresh mode, data can be retained without external  $\overline{CAS}$  signal during system is in standby.

Restriction for Self Refresh operation ;

For self refresh operation, the notice below must be considered.

- 1) In the case that distributed CBR refresh are operated between read/write cycles  
 Self Refresh cycles can be executed without special rule if 4,096 cycles of distributed CBR refresh are executed within  $t_{REF}$  max.
- 2) In the case that burst CBR refresh or distributed/burst  $\overline{RAS}$ -only refresh are operated between read/write cycles  
 4,096 times of burst CBR refresh or 4,096 times of burst  $\overline{RAS}$ -only refresh must be executed before and after Self Refresh cycles.



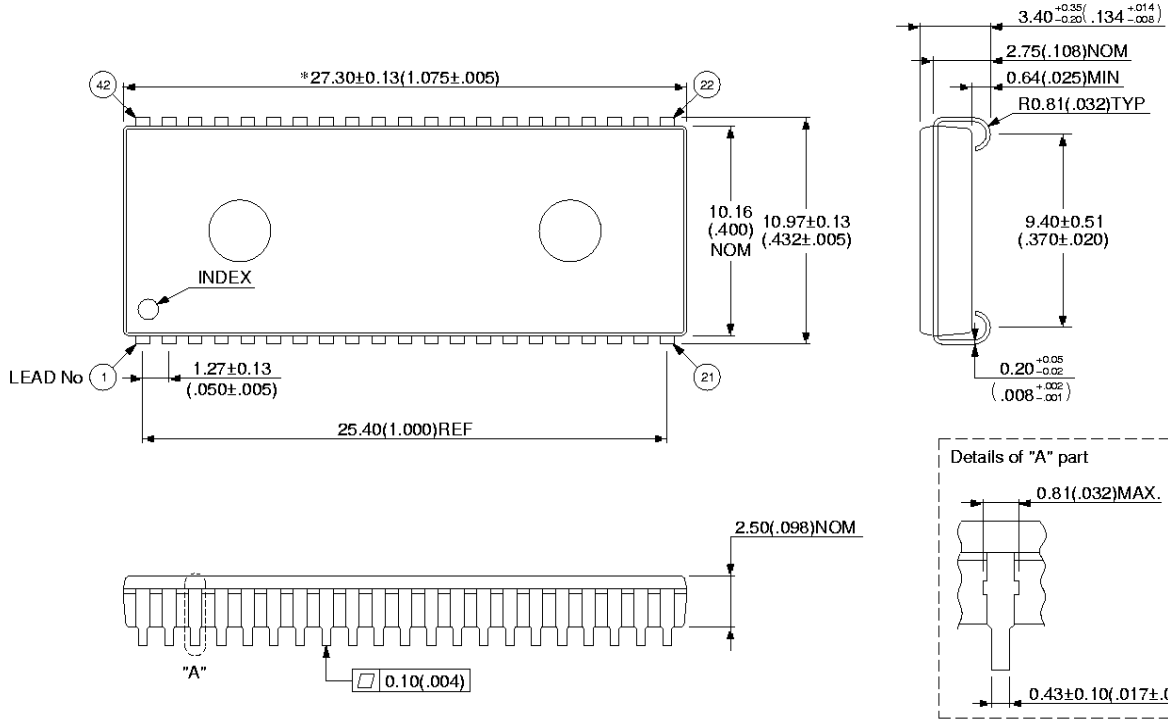


# MB81V16160B-50/-60/-50L/-60L

## ■ PACKAGE DIMENSIONS

42-pin plastic SOJ  
(LCC-42P-M01)

\* : Resin protrusion. (Each side: 0.15 (.006) MAX)



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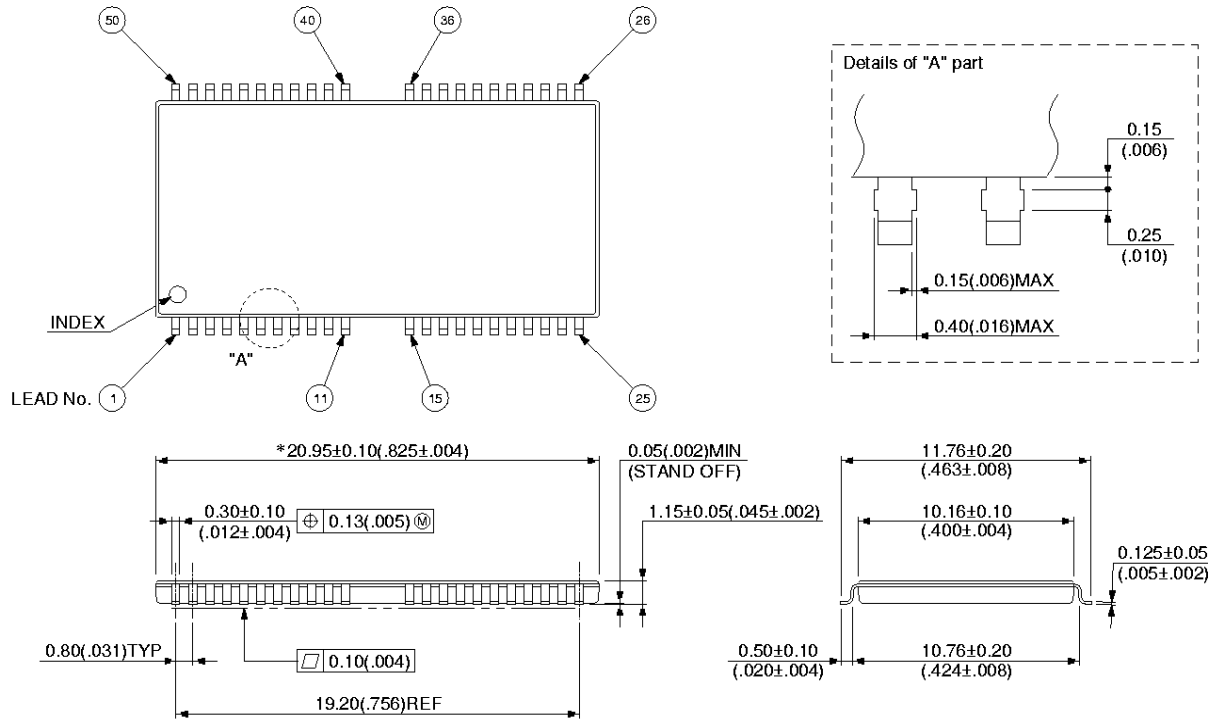
Dimensions in mm (inches)

# MB81V16160B-50/-60/-50L/-60L

(Continued)

50-pin plastic TSOP (II)  
(FPT-50P-M06)

\* : Resin protrusion. (Each side: 0.15 (.006) MAX)



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Dimensions in mm (inches)

# MB81V16160B-50/-60/-50L/-60L

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