

Document Title

256Kx36 & 256Kx32 & 512Kx18-Bit Flow Through NtRAM™

Revision History

<u>Rev. No.</u>	<u>History</u>	<u>Draft</u>	<u>Date</u>	<u>Remark</u>
0.0	1. Initial document.		May. 18. 2001	Preliminary
0.1	1. Add x32 org part and industrial temperature part		Aug. 11. 2001	Preliminary
0.2	1. change scan order(1) form 4T to 6T at 119BGA(x18)		Aug. 28. 2001	Preliminary
1.0	1. Final spec release 2. Change ISB2 form 50mA to 60mA		Nov. 16. 2001	Final

The attached data sheets are prepared and approved by SAMSUNG Electronics. SAMSUNG Electronics CO., LTD. reserve the right to change the specifications. SAMSUNG Electronics will evaluate and reply to your requests and questions on the parameters of this device. If you have any questions, please contact the SAMSUNG branch office near your office, call or contact Headquarters.

8Mb NtRAM(Flow Through / Pipelined) Ordering Information

Org.	Part Number	Mode	VDD	Speed FT ; Access Time(ns) Pipelined ; Cycle Time(MHz)	PKG	Temp
512Kx18	K7M801825B-Q(H)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5 ns	Q: 100TQFP H: 119BGA	C: Commercial Temperature Range I: Industrial Temperature Range
	K7N801801B-Q(H)C(I)16/13	Pipelined	3.3	167/133 MHz		
	K7N801809B-Q(H)C(I)25/22/20	Pipelined	3.3	250/225/200 MHz		
	K7N801845B-Q(H)C(I)16/13	Pipelined	2.5	167/133 MHz		
	K7N801849B-Q(H)C(I)25/22/20	Pipelined	2.5	250/225/200 MHz		
256Kx32	K7M803225B-QC(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5 ns		
	K7N803201B-QC(I)16/13	Pipelined	3.3	167/133 MHz		
	K7N803209B-QC(I)25/22/20	Pipelined	3.3	250/225/200 MHz		
	K7N803245B-QC(I)16/13	Pipelined	2.5	167/133 MHz		
	K7N803249B-QC(I)25/22/20	Pipelined	2.5	250/225/200 MHz		
256Kx36	K7M803625B-Q(H)C(I)65/75/85	FlowThrough	3.3	6.5/7.5/8.5 ns		
	K7N803601B-Q(H)C(I)16/13	Pipelined	3.3	167/133 MHz		
	K7N803609B-Q(H)C(I)25/22/20	Pipelined	3.3	250/225/200 MHz		
	K7N803645B-Q(H)C(I)16/13	Pipelined	2.5	167/133 MHz		
	K7N803649B-Q(H)C(I)25/22/20	Pipelined	2.5	250/225/200 MHz		

256Kx36 & 512Kx18-Bit Flow Through NtRAM™

FEATURES

- 3.3V+0.165V/-0.165V Power Supply.
- I/O Supply Voltage 3.3V+0.165V/-0.165V for 3.3V I/O or 2.5V+0.4V/-0.125V for 2.5V I/O
- Byte Writable Function.
- Enable clock and suspend operation.
- Single READ/WRITE control pin.
- Self-Timed Write Cycle.
- Three Chip Enable for simple depth expansion with no data contention .
- A interleaved burst or a linear burst mode.
- Asynchronous output enable control.
- Power Down mode.
- TTL-Level Three-State Outputs.
- 100-TQFP-1420A /119BGA(7x17 Ball Grid Array Package).
- Operating in commercial and industrial temperature range.

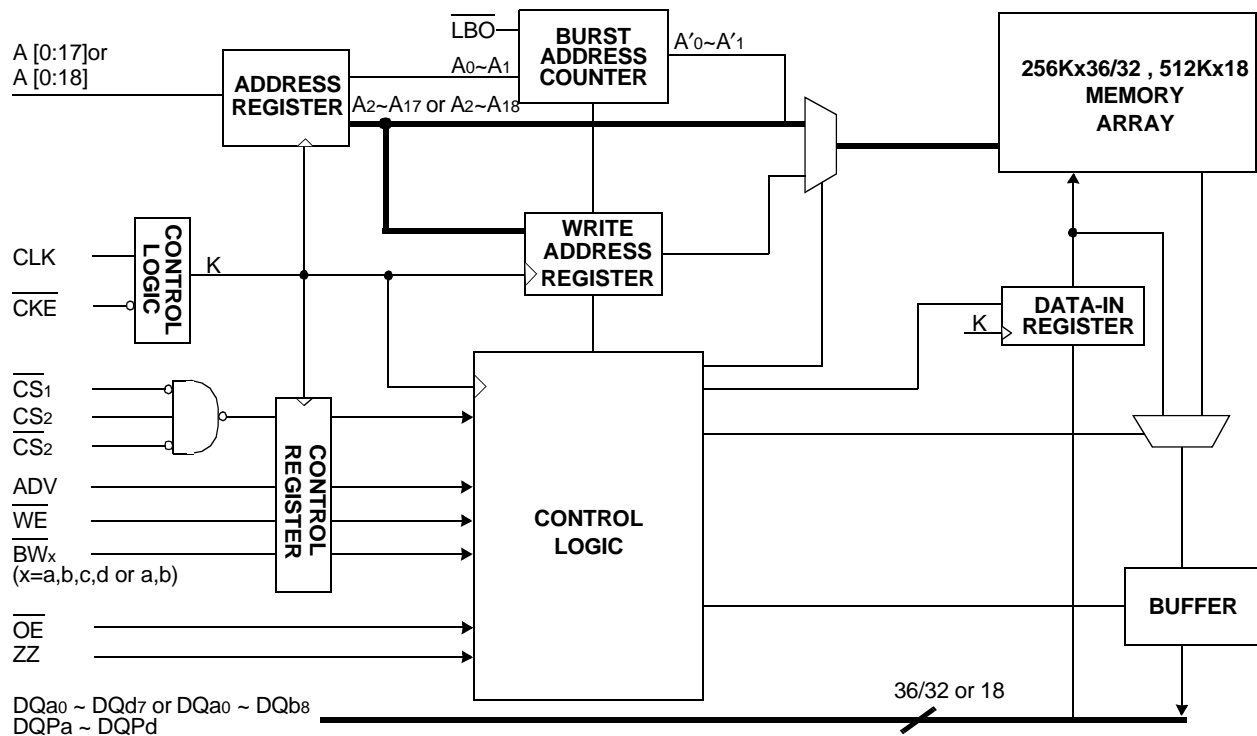
FAST ACCESS TIMES

Parameter	Symbol	-65	-75	-85	Unit
Cycle Time	t _{CYC}	7.5	8.5	10	ns
Clock Access Time	t _{CD}	6.5	7.5	8.5	ns
Output Enable Access Time	t _{OE}	3.5	3.5	4.0	ns

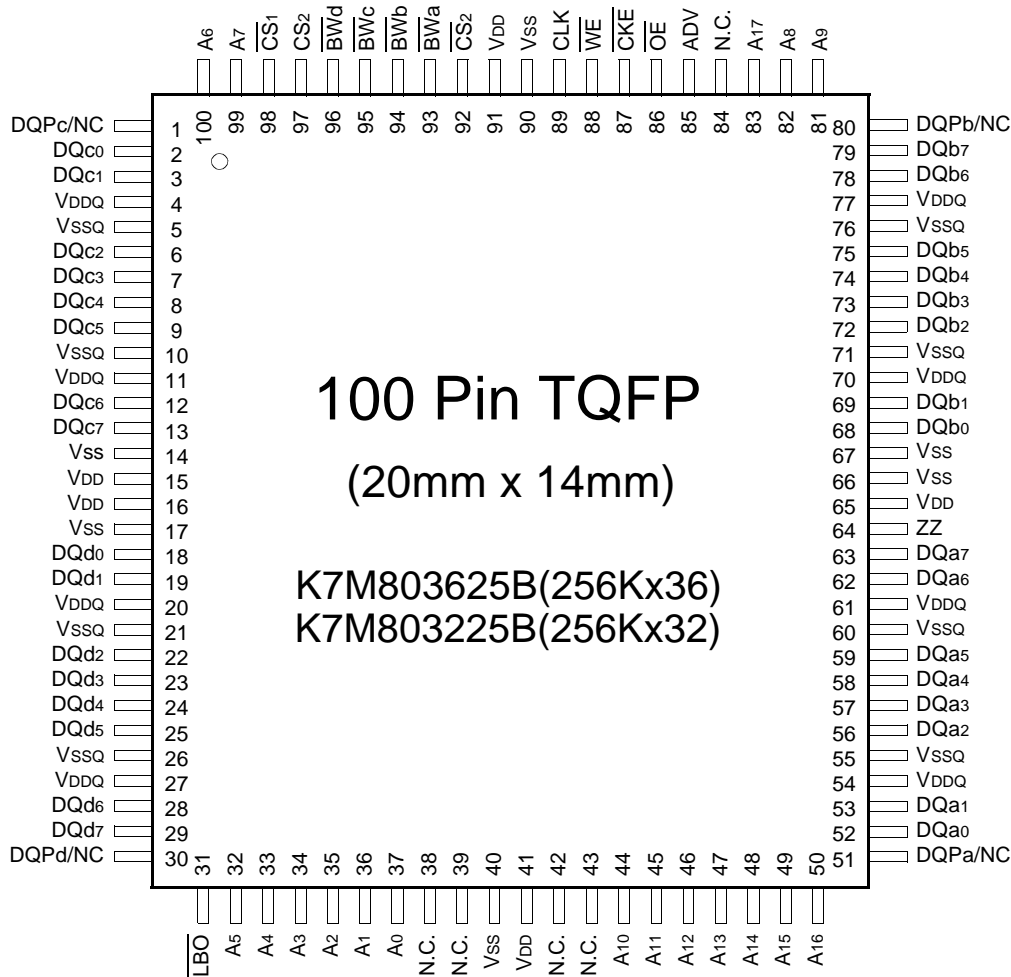
GENERAL DESCRIPTION

The K7M803625B, K7M803225B and K7M801825B are 9,437,184-bit Synchronous Static SRAMs. The NtRAM™, or No Turnaround Random Access Memory utilizes all bandwidth in any combination of operating cycles. Address, data inputs, and all control signals except output enable and linear burst order are synchronized to input clock. Burst order control must be tied "High or Low". Asynchronous inputs include the sleep mode enable(ZZ). Output Enable controls the outputs at any given time. Write cycles are internally self-timed and initiated by the rising edge of the clock input. This feature eliminates complex off-chip write pulse generation and provides increased timing flexibility for incoming signals. For read cycles, Flow-Through SRAM allows output data to simply flow freely from the memory array. The K7M803625B, K7M803225B and K7M801825B are implemented with SAMSUNG's high performance CMOS technology and is available in 100pin TQFP and 119BGA packages (100pin TQFP only for K7M803225B). Multiple power and ground pins minimize ground bounce.

LOGIC BLOCK DIAGRAM



PIN CONFIGURATION(TOP VIEW)

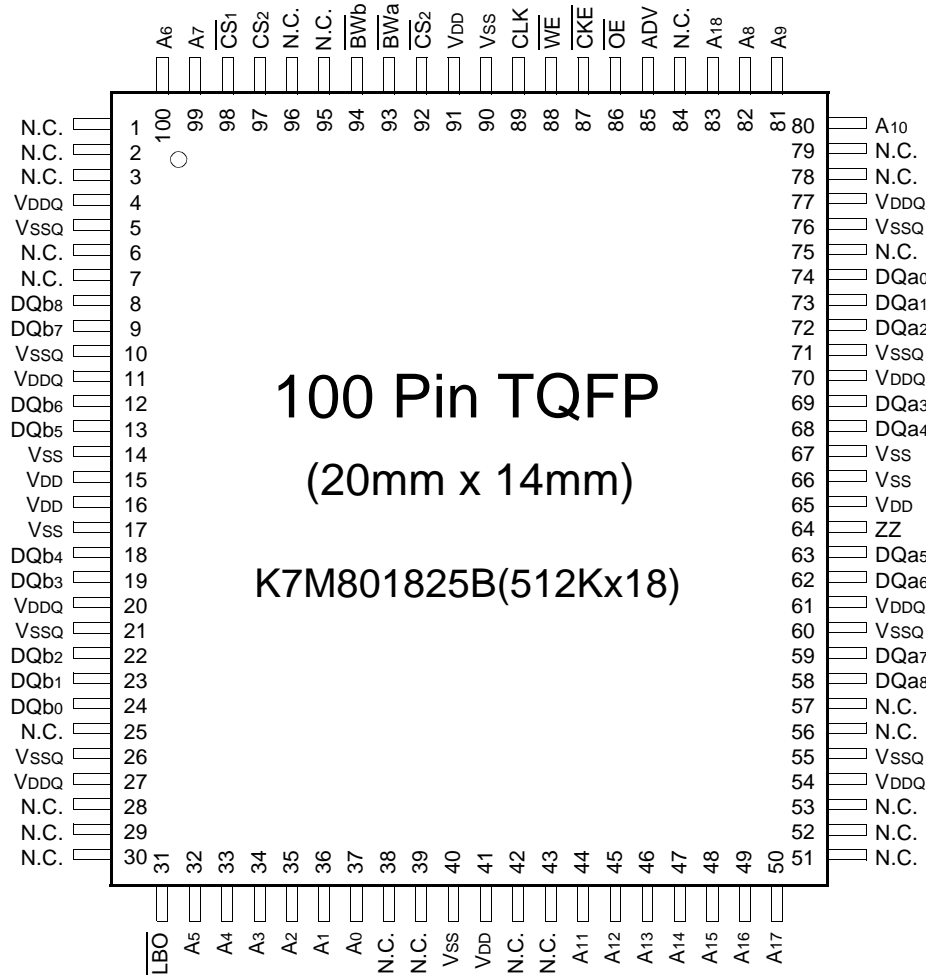


PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A17	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,81 82,83,99,100	VDD	Power Supply(+3.3V)	15,16,41,65,91
			VSS	Ground	14,17,40,66,67,90
			N.C.	No Connect	38,39,42,43,84
ADV	Address Advance/Load	85	DQa0~a7	Data Inputs/Outputs	52,53,56,57,58,59,62,63
WE	Read/Write Control Input	88	DQb0~b7		68,69,72,73,74,75,78,79
CLK	Clock	89	DQc0~c7		2,3,6,7,8,9,12,13
CKE	Clock Enable	87	DQd0~d7		18,19,22,23,24,25,28,29
CS1	Chip Select	98	DQPa~Pd		51,80,1,30
CS2	Chip Select	97	/NC		
CS2	Chip Select	92	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
BWx(x=a,b,c,d)	Byte Write Inputs	93,94,95,96	VSSQ	Output Ground	5,10,21,26,55,60,71,76
OE	Output Enable	86			
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

- Notes :** 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.
3. DQPa~DQPd are NC for K7M803225B

PIN CONFIGURATION(TOP VIEW)



PIN NAME

SYMBOL	PIN NAME	TQFP PIN NO.	SYMBOL	PIN NAME	TQFP PIN NO.
A0 - A18	Address Inputs	32,33,34,35,36,37,44 45,46,47,48,49,50,80 81,82,83,99,100	VDD	Power Supply(+3.3V)	15,16,41,65,91
			VSS	Ground	14,17,40,66,67,90
			N.C.	No Connect	1,2,3,6,7,25,28,29,30, 38,39,42,43,51,52,53, 56,57,75,78,79,84,95,96
ADV	Address Advance/Load	85	DQa0~a8	Data Inputs/Outputs	58,59,62,63,68,69,72,73,74
WE	Read/Write Control Input	88	DQb0~b8		8,9,12,13,18,19,22,23,24
CLK	Clock	89	VDDQ	Output Power Supply (2.5V or 3.3V)	4,11,20,27,54,61,70,77
CKE	Clock Enable	87	VSSQ	Output Ground	5,10,21,26,55,60,71,76
CS1	Chip Select	98			
CS2	Chip Select	97			
CS2	Chip Select	92			
BWx(x=a,b)	Byte Write Inputs	93,94			
OE	Output Enable	86			
ZZ	Power Sleep Mode	64			
LBO	Burst Mode Control	31			

Notes : 1. The pin 84 is reserved for address bit for the 16Mb NtRAM.
2. A0 and A1 are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7M803625B(256Kx36)

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	NC**	A	A	V _{DDQ}
B	NC	CS ₂	A	ADV	A	\overline{CS}_2	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQc	DQPc	V _{SS}	NC	V _{SS}	DQPb	DQb
E	DQc	DQc	V _{SS}	\overline{CS}_1	V _{SS}	DQb	DQb
F	V _{DDQ}	DQc	V _{SS}	\overline{OE}	V _{SS}	DQb	V _{DDQ}
G	DQc	DQc	\overline{BW}_c	A	\overline{BW}_b	DQb	DQb
H	DQc	DQc	V _{SS}	\overline{WE}	V _{SS}	DQb	DQb
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	DQd	DQd	V _{SS}	CLK	V _{SS}	DQa	DQa
L	DQd	DQd	\overline{BW}_d	NC	\overline{BW}_a	DQa	DQa
M	V _{DDQ}	DQd	V _{SS}	\overline{CKE}	V _{SS}	DQa	V _{DDQ}
N	DQd	DQd	V _{SS}	A ₁ *	V _{SS}	DQa	DQa
P	DQd	DQPd	V _{SS}	A ₀ *	V _{SS}	DQPa	DQa
R	NC	A	\overline{LBO}	V _{DD}	NC	A	NC
T	NC	NC	A	A	A	NC	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

** Pin 4A is reserved for address expansion to 16Mb.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V _{DD}	Power Supply
A ₀ ,A ₁	Burst Address Inputs	V _{SS}	Ground
ADV	Address Advance/Load	N.C.	No Connect
\overline{WE}	Read/Write Control Input		
CLK	Clock	DQa	Data Inputs/Outputs
\overline{CKE}	Clock Enable	DQb	Data Inputs/Outputs
\overline{CS}_1	Chip Select	DQc	Data Inputs/Outputs
CS ₂	Chip Select	DQd	Data Inputs/Outputs
\overline{CS}_2	Chip Select	DQPa~Pd	Data Inputs/Outputs
\overline{BW}_x	Byte Write Inputs		
(x=a,b,c,d)		V _{DDQ}	Output Power Supply
\overline{OE}	Output Enable		
ZZ	Power Sleep Mode		
LBO	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

119BGA PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7M801825B(512Kx18)

	1	2	3	4	5	6	7
A	V _{DDQ}	A	A	NC**	A	A	V _{DDQ}
B	NC	CS ₂	A	ADV	A	\overline{CS}_2	NC
C	NC	A	A	V _{DD}	A	A	NC
D	DQ _b	NC	V _{SS}	NC	V _{SS}	DQ _a	NC
E	NC	DQ _b	V _{SS}	\overline{CS}_1	V _{SS}	NC	DQ _a
F	V _{DDQ}	NC	V _{SS}	\overline{OE}	V _{SS}	DQ _a	V _{DDQ}
G	NC	DQ _b	\overline{BW}_b	A	V _{SS}	NC	DQ _a
H	DQ _b	NC	V _{SS}	\overline{WE}	V _{SS}	DQ _a	NC
J	V _{DDQ}	V _{DD}	NC	V _{DD}	NC	V _{DD}	V _{DDQ}
K	NC	DQ _b	V _{SS}	CLK	V _{SS}	NC	DQ _a
L	DQ _b	NC	V _{SS}	NC	\overline{BW}_a	DQ _a	NC
M	V _{DDQ}	DQ _b	V _{SS}	\overline{CKE}	V _{SS}	NC	V _{DDQ}
N	DQ _b	NC	V _{SS}	A ₁ *	V _{SS}	DQ _a	NC
P	NC	DQ _b	V _{SS}	A ₀ *	V _{SS}	NC	DQ _a
R	NC	A	\overline{LBO}	V _{DD}	NC	A	NC
T	NC	A	A	NC	A	A	ZZ
U	V _{DDQ}	TMS	TDI	TCK	TDO	NC	V _{DDQ}

Note : * A₀ and A₁ are the two least significant bits(LSB) of the address field and set the internal burst counter if burst is desired.

** Pin 4A is reserved for address expansion to 16Mb.

PIN NAME

SYMBOL	PIN NAME	SYMBOL	PIN NAME
A	Address Inputs	V _{DD}	Power Supply
A ₀ ,A ₁	Burst Address Inputs	V _{SS}	Ground
ADV	Address Advance/Load	N.C.	No Connect
\overline{WE}	Read/Write Control Input		
CLK	Clock		
\overline{CKE}	Clock Enable	DQ _a	Data Inputs/Outputs
\overline{CS}_1	Chip Select	DQ _b	Data Inputs/Outputs
\overline{CS}_2	Chip Select	DQ _{Pa} , Pb	Data Inputs/Outputs
\overline{CS}_2	Chip Select		
\overline{BW}_x (x=a,b)	Byte Write Inputs	V _{DDQ}	Output Power Supply
\overline{OE}	Output Enable		
ZZ	Power Sleep Mode		
\overline{LBO}	Burst Mode Control		
TCK	JTAG Test Clock		
TMS	JTAG Test Mode Select		
TDI	JTAG Test Data Input		
TDO	JTAG Test Data Output		

FUNCTION DESCRIPTION

The K7M803625B, K7M803225B and K7M801825B are NfRAM™ designed to sustain 100% bus bandwidth by eliminating turn-around cycle when there is transition from Read to Write, or vice versa.

All inputs (with the exception of OE, LBO and ZZ) are synchronized to rising clock edges.

All read, write and deselect cycles are initiated by the ADV input. Subsequent burst addresses can be internally generated by the burst advance pin (ADV). ADV should be driven to Low once the device has been deselected in order to load a new address for next operation.

Clock Enable(CKE) pin allows the operation of the chip to be suspended as long as necessary. When CKE is high, all synchronous inputs are ignored and the internal device registers will hold their previous values.

NfRAM™ latches external address and initiates a cycle, when CKE, ADV are driven to low and all three chip enables(CS1, CS2, CS2) are active .

Output Enable(OE) can be used to disable the output at any given time.

Read operation is initiated when at the rising edge of the clock, the address presented to the address inputs are latched in the address register, CKE is driven low, all three chip enables(CS1, CS2, CS2) are active, the write enable input signals WE are driven high, and ADV driven low. Data appears at the outputs within the same clock cycle as the address for the data. Also during read operation OE must be driven low for the device to drive out the requested data.

Write operation occurs when WE is driven low at the rising edge of the clock. BW[d:a] can be used for byte write operation. The Flow Through NfRAM™ uses a late write cycle to utilize 100% of the bandwidth.

At the first rising edge of the clock, WE and address are registered, and the data associated with that address is required one cycle later.

Subsequent addresses are generated by ADV High for the burst access as shown below. The starting point of the burst sequence is provided by the external address. The burst address counter wraps around to its initial state upon completion.

The burst sequence is determined by the state of the LBO pin. When this pin is low, linear burst sequence is selected.

And when this pin is high, Interleaved burst sequence is selected.

During normal operation, ZZ must be driven low. When ZZ is driven high, the SRAM will enter a Power Sleep Mode after 2 cycles. At this time, internal state of the SRAM is preserved. When ZZ returns to low, the SRAM normally operates after 2 cycles of wake up time.

BURST SEQUENCE TABLE

(Interleaved Burst, LBO=High)

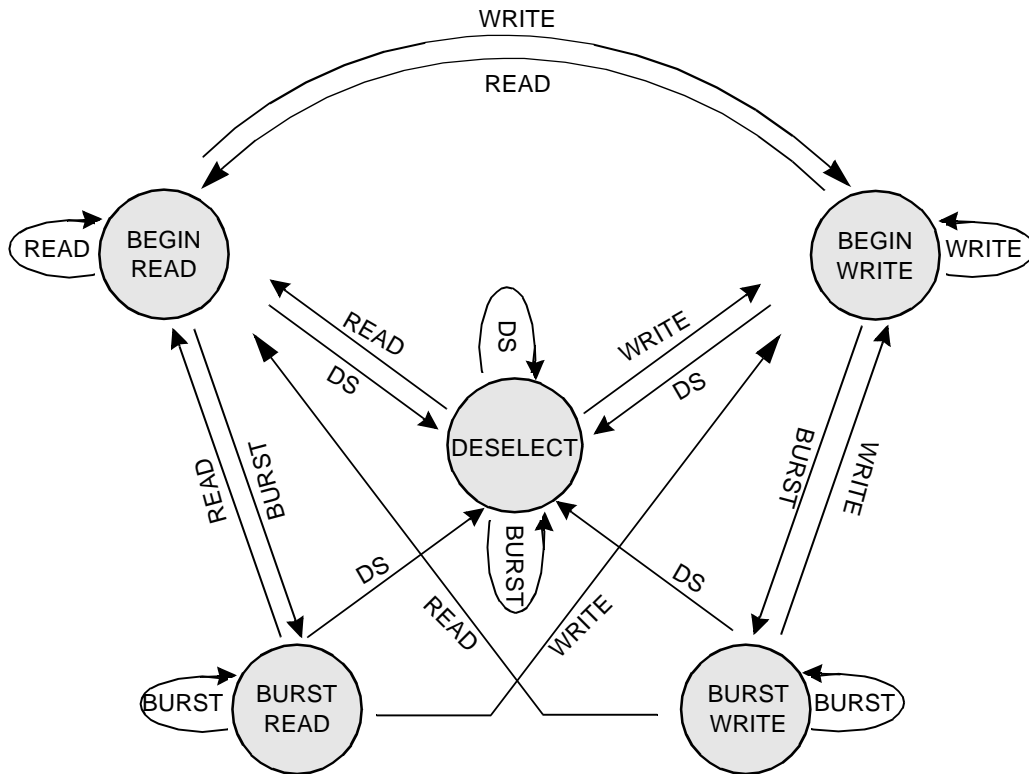
LBO PIN	HIGH	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	0	0	1	1	1	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	1	0	0	1	0	0

(Linear Burst, LBO=Low)

LBO PIN	LOW	Case 1		Case 2		Case 3		Case 4	
		A1	A0	A1	A0	A1	A0	A1	A0
	First Address	0	0	0	1	1	0	1	1
	↓	0	1	1	0	1	1	0	0
	↓	1	0	1	1	0	0	0	1
	Fourth Address	1	1	0	0	0	1	1	0

Note : 1. LBO pin must be tied to High or Low, and Floating State must not be allowed.

STATE DIAGRAM FOR NtRAM™



COMMAND	ACTION
DS	DESELECT
READ	BEGIN READ
WRITE	BEGIN WRITE
BURST	BEGIN READ BEGIN WRITE CONTINUE DESELECT

Notes : 1. An IGNORE CLOCK EDGE cycle is not shown in the above diagram. This is because CKE HIGH only blocks the clock(CLK) input and does not change the state of the device.
 2. States change on the rising edge of the clock(CLK)

TRUTH TABLES

SYNCHRONOUS TRUTH TABLE

\overline{CS}_1	\overline{CS}_2	\overline{CS}_2	ADV	\overline{WE}	\overline{BW}_x	\overline{OE}	\overline{CKE}	CLK	ADDRESS ACCESSED	OPERATION
H	X	X	L	X	X	X	L	↑	N/A	Not Selected
X	L	X	L	X	X	X	L	↑	N/A	Not Selected
X	X	H	L	X	X	X	L	↑	N/A	Not Selected
X	X	X	H	X	X	X	L	↑	N/A	Not Selected Continue
L	H	L	L	H	X	L	L	↑	External Address	Begin Burst Read Cycle
X	X	X	H	X	X	L	L	↑	Next Address	Continue Burst Read Cycle
L	H	L	L	H	X	H	L	↑	External Address	NOP/Dummy Read
X	X	X	H	X	X	H	L	↑	Next Address	Dummy Read
L	H	L	L	L	L	X	L	↑	External Address	Begin Burst Write Cycle
X	X	X	H	X	L	X	L	↑	Next Address	Continue Burst Write Cycle
L	H	L	L	L	H	X	L	↑	N/A	NOP/Write Abort
X	X	X	H	X	H	X	L	↑	Next Address	Write Abort
X	X	X	X	X	X	X	H	↑	Current Address	Ignore Clock

- Notes :** 1. X means "Don't Care". 2. The rising edge of clock is symbolized by (↑).
3. A continue deselect cycle can only be entered if a deselect cycle is executed first.
4. $\overline{WRITE} = L$ means Write operation in WRITE TRUTH TABLE.
 $\overline{WRITE} = H$ means Read operation in WRITE TRUTH TABLE.
5. Operation finally depends on status of asynchronous input pins(ZZ and \overline{OE}).

WRITE TRUTH TABLE (x36/32)

\overline{WE}	\overline{BW}_a	\overline{BW}_b	\overline{BW}_c	\overline{BW}_d	Operation
H	X	X	X	X	READ
L	L	H	H	H	WRITE BYTE a
L	H	L	H	H	WRITE BYTE b
L	H	H	L	H	WRITE BYTE c
L	H	H	H	L	WRITE BYTE d
L	L	L	L	L	WRITE ALL BYTES
L	H	H	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

WRITE TRUTH TABLE (x18)

\overline{WE}	\overline{BW}_a	\overline{BW}_b	OPERATION
H	X	X	READ
L	L	H	WRITE BYTE a
L	H	L	WRITE BYTE b
L	L	L	WRITE ALL BYTES
L	H	H	WRITE ABORT/NOP

- Notes :** 1. X means "Don't Care".
2. All inputs in this table must meet setup and hold time around the rising edge of CLK(↑).

ASYNCHRONOUS TRUTH TABLE

Operation	ZZ	\overline{OE}	I/O STATUS
Sleep Mode	H	X	High-Z
Read	L	L	DQ
	L	H	High-Z
Write	L	X	Din, High-Z
Deselected	L	X	High-Z

Notes

1. X means "Don't Care".
2. Sleep Mode means power Sleep Mode of which stand-by current does not depend on cycle time.
3. Deselected means power Sleep Mode of which stand-by current depends on cycle time.

ABSOLUTE MAXIMUM RATINGS*

PARAMETER	SYMBOL	RATING	UNIT
Voltage on V _{DD} Supply Relative to V _{SS}	V _{DD}	-0.3 to 4.6	V
Voltage on Any Other Pin Relative to V _{SS}	V _{IN}	-0.3 to V _{DD} +0.3	V
Power Dissipation	P _D	1.4	W
Storage Temperature	T _{STG}	-65 to 150	°C
Operating Temperature	Commercial	T _{OPR}	0 to 70
	Industrial	T _{OPR}	-40 to 85
Storage Temperature Range Under Bias	T _{BIAS}	-10 to 85	°C

*Notes : Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

OPERATING CONDITIONS at 3.3V I/O (0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V _{DD}	3.135	3.3	3.465	V
	V _{DDQ}	3.135	3.3	3.465	V
Ground	V _{SS}	0	0	0	V

* The above parameters are also guaranteed at industrial temperature range.

OPERATING CONDITIONS at 2.5V I/O (0°C ≤ T_A ≤ 70°C)

PARAMETER	SYMBOL	MIN	Typ.	MAX	UNIT
Supply Voltage	V _{DD}	3.135	3.3	3.465	V
	V _{DDQ}	2.375	2.5	2.9	V
Ground	V _{SS}	0	0	0	V

* The above parameters are also guaranteed at industrial temperature range.

CAPACITANCE* (T_A=25°C, f=1MHz)

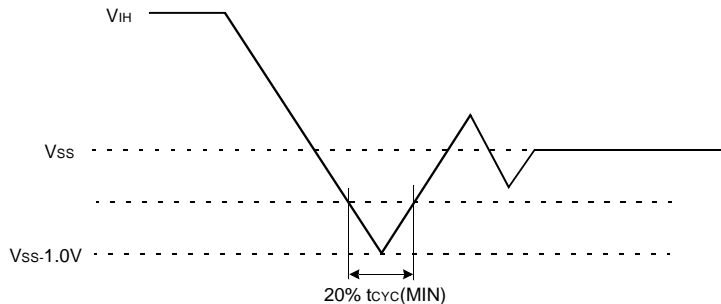
PARAMETER	SYMBOL	TEST CONDITION	MIN	MAX	UNIT
Input Capacitance	C _{IN}	V _{IN} =0V	-	5	pF
Output Capacitance	C _{OUT}	V _{OUT} =0V	-	7	pF

*Note : Sampled not 100% tested.

DC ELECTRICAL CHARACTERISTICS(V_{DD}=3.3V+0.165V/-0.165V, T_A=0°C to +70°C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNIT	NOTES	
Input Leakage Current(except ZZ)	I _{IL}	V _{DD} =Max ; V _{IN} =V _{SS} to V _{DD}	-2	+2	μA		
Output Leakage Current	I _{OL}	Output Disabled,	-2	+2	μA		
Operating Current	I _{CC}	Device Selected, I _{OUT} =0mA, ZZ≤V _{IL} , Cycle Time ≥ t _{CYC} Min	-65	-	300	mA	1,2
			-75	-	280		
			-85	-	260		
Standby Current	I _{SB}	Device deselected, I _{OUT} =0mA, ZZ≤V _{IL} , f=Max, All Inputs≤0.2V or ≥ V _{DD} -0.2V	-65	-	140	mA	
			-75	-	130		
			-85	-	120		
	I _{SB1}	Device deselected, I _{OUT} =0mA, ZZ≤0.2V, f=0, All Inputs=fixed (V _{DD} -0.2V or 0.2V)	-	-	100	mA	
I _{SB2}	Device deselected, I _{OUT} =0mA, ZZ≥V _{DD} -0.2V, f=Max, All Inputs≤V _{IL} or ≥V _{IH}	-	-	60	mA		
Output Low Voltage(3.3V I/O)	V _{OL}	I _{OL} =8.0mA	-	0.4	V		
Output High Voltage(3.3V I/O)	V _{OH}	I _{OH} =-4.0mA	2.4	-	V		
Output Low Voltage(2.5V I/O)	V _{OL}	I _{OL} =1.0mA	-	0.4	V		
Output High Voltage(2.5V I/O)	V _{OH}	I _{OH} =-1.0mA	2.0	-	V		
Input Low Voltage(3.3V I/O)	V _{IL}		-0.3*	0.8	V		
Input High Voltage(3.3V I/O)	V _{IH}		2.0	V _{DD} +0.3**	V	3	
Input Low Voltage(2.5V I/O)	V _{IL}		-0.3*	0.7	V		
Input High Voltage(2.5V I/O)	V _{IH}		1.7	V _{DD} +0.3**	V	3	

- Notes :** 1. The above parameters are also guaranteed at industrial temperature range.
2. Reference AC Operating Conditions and Characteristics for input and timing.
3. Data states are all zero.
4. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V.

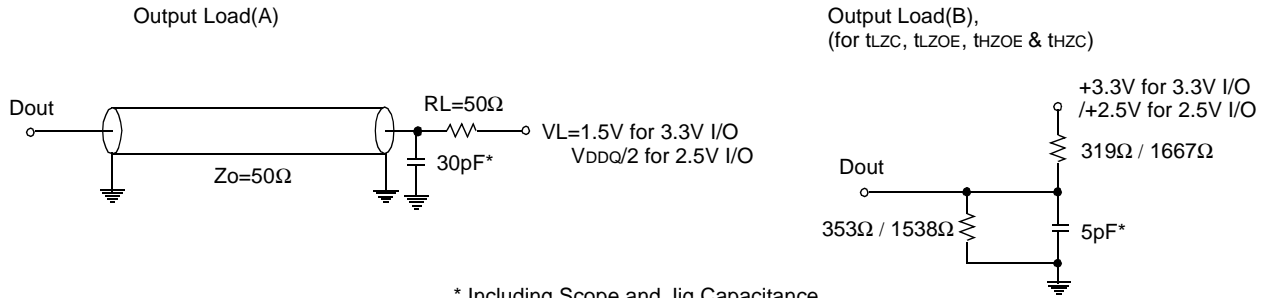


TEST CONDITIONS

(V_{DD}=3.3V+0.165V/-0.165V, V_{DDQ}=3.3V+0.165V/-0.165V or V_{DD}=3.3V+0.165V/-0.165V, V_{DDQ}=2.5V+0.4V/-0.125V, T_A=0to70°C)

Parameter	Value
Input Pulse Level(for 3.3V I/O)	0 to 3.0V
Input Pulse Level(for 2.5V I/O)	0 to 2.5V
Input Rise and Fall Time(Measured at 20% to 80% for 3.3V I/O)	1.0V/ns
Input Rise and Fall Time(Measured at 20% to 80% for 2.5V I/O)	1.0V/ns
Input and Output Timing Reference Levels for 3.3V I/O	1.5V
Input and Output Timing Reference Levels for 2.5V I/O	V _{DDQ} /2
Output Load	See Fig. 1

* The above parameters are also guaranteed at industrial temperature range.



* Including Scope and Jig Capacitance

Fig. 1

AC TIMING CHARACTERISTICS($V_{DD}=3.3V+0.165V/-0.165V$, $T_A=0^{\circ}C$ to $+70^{\circ}C$)

PARAMETER	SYMBOL	-65		-75		-85		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t _{CYC}	7.5	-	8.5	-	10	-	ns
Clock Access Time	t _{CD}	-	6.5	-	7.5	-	8.5	ns
Output Enable to Data Valid	t _{OE}	-	3.5	-	3.5	-	4.0	ns
Clock High to Output Low-Z	t _{LZC}	2.5	-	2.5	-	2.5	-	ns
Output Hold from Clock High	t _{OH}	2.5	-	2.5	-	2.5	-	ns
Output Enable Low to Output Low-Z	t _{LZOE}	0	-	0	-	0	-	ns
Output Enable High to Output High-Z	t _{HZOE}	-	3.5	-	3.5	-	4.0	ns
Clock High to Output High-Z	t _{HZC}	-	3.8	-	4.0	-	5.0	ns
Clock High Pulse Width	t _{CH}	2.5	-	2.8	-	3.0	-	ns
Clock Low Pulse Width	t _{CL}	2.5	-	2.8	-	3.0	-	ns
Address Setup to Clock High	t _{AS}	1.5	-	2.0	-	2.0	-	ns
\overline{CKE} Setup to Clock High	t _{CES}	1.5	-	2.0	-	2.0	-	ns
Data Setup to Clock High	t _{DS}	1.5	-	2.0	-	2.0	-	ns
Write Setup to Clock High (\overline{WE} , \overline{BWx})	t _{WS}	1.5	-	2.0	-	2.0	-	ns
Address Advance Setup to Clock High	t _{ADVS}	1.5	-	2.0	-	2.0	-	ns
Chip Select Setup to Clock High	t _{CSS}	1.5	-	2.0	-	2.0	-	ns
Address Hold from Clock High	t _{AH}	0.5	-	0.5	-	0.5	-	ns
\overline{CKE} Hold from Clock High	t _{CEH}	0.5	-	0.5	-	0.5	-	ns
Data Hold from Clock High	t _{DH}	0.5	-	0.5	-	0.5	-	ns
Write Hold from Clock High (\overline{WE} , \overline{BWx})	t _{WH}	0.5	-	0.5	-	0.5	-	ns
Address Advance Hold from Clock High	t _{ADVH}	0.5	-	0.5	-	0.5	-	ns
Chip Select Hold from Clock High	t _{CSH}	0.5	-	0.5	-	0.5	-	ns
ZZ High to Power Down	t _{PDS}	2	-	2	-	2	-	cycle
ZZ Low to Power Up	t _{PUS}	2	-	2	-	2	-	cycle

- Notes :**
- The above parameters are also guaranteed at industrial temperature range.
 - All address inputs must meet the specified setup and hold times for all rising clock(CLK) edges when ADV is sampled low and \overline{CS} is sampled low. All other synchronous inputs must meet the specified setup and hold times whenever this device is chip selected.
 - Chip selects must be valid at each rising edge of CLK(when ADV is Low) to remain enabled.
 - A write cycle is defined by \overline{WE} low having been registered into the device at ADV Low, A Read cycle is defined by \overline{WE} High with ADV Low, Both cases must meet setup and hold times.
 - To avoid bus contention, At a given voltage and temperature t_{LZC} is more than t_{HZC}.
 The soecs as shown do not imply bus contention because t_{LZC} is a Min. parameter that is worst case at totally different test conditions (0°C,3.465V) than t_{HZC}, which is a Max. parameter(worst case at 70°C,3.135V)
 It is not possible for two SRAMs on the same board to be at such different voltage and temperature.

SLEEP MODE

SLEEP MODE is a low current, power-down mode in which the device is deselected and current is reduced to I_{SB2} . The duration of SLEEP MODE is dictated by the length of time the ZZ is in a High state.

After entering SLEEP MODE, all inputs except ZZ become disabled and all outputs go to High-Z

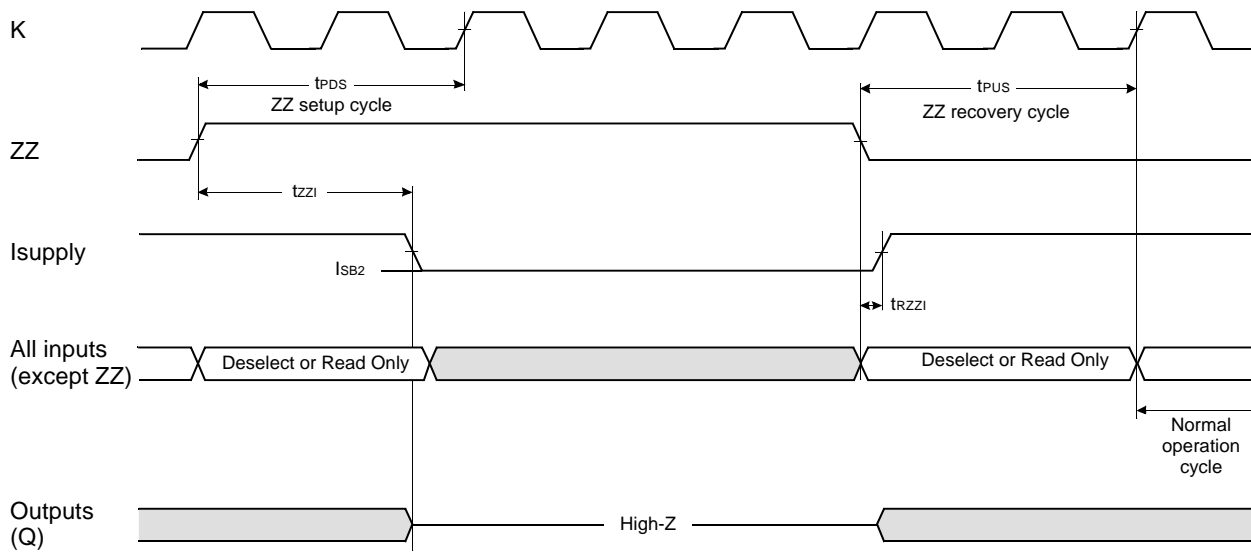
The ZZ pin is an asynchronous, active high input that causes the device to enter SLEEP MODE.

When the ZZ pin becomes a logic High, I_{SB2} is guaranteed after the time t_{ZZI} is met. Any operation pending when entering SLEEP MODE is not guaranteed to successful complete. Therefore, SLEEP MODE (READ or WRITE) must not be initiated until valid pending operations are completed. Similarly, when exiting SLEEP MODE during t_{PUS} , only a DESELECT or READ cycle should be given while the SRAM is transitioning out of SLEEP MODE.

SLEEP MODE ELECTRICAL CHARACTERISTICS

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Current during SLEEP MODE	$ZZ \geq V_{IH}$	I_{SB2}		10	mA
ZZ active to input ignored		t_{PDS}	2		cycle
ZZ inactive to input sampled		t_{PUS}	2		cycle
ZZ active to SLEEP current		t_{ZZI}		2	cycle
ZZ inactive to exit SLEEP current		t_{RZZI}	0		

SLEEP MODE WAVEFORM

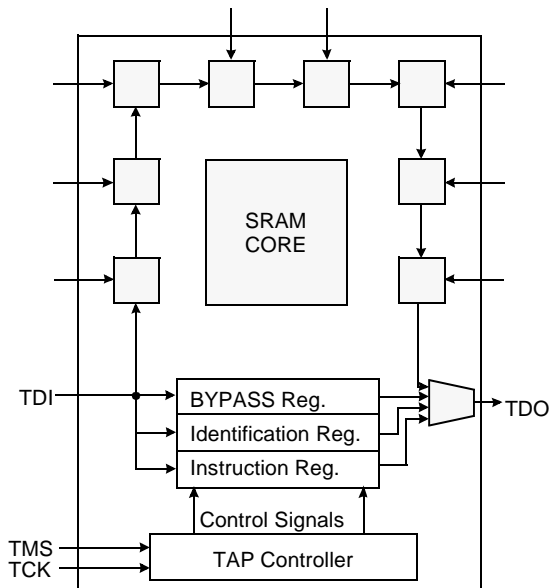


□ DON'T CARE

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

This part contains an IEEE standard 1149.1 Compatible Test Access Port(TAP). The package pads are monitored by the Serial Scan circuitry when in test mode. This is to support connectivity testing during manufacturing and system diagnostics. Internal data is not driven out of the SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{ss} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and may be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram



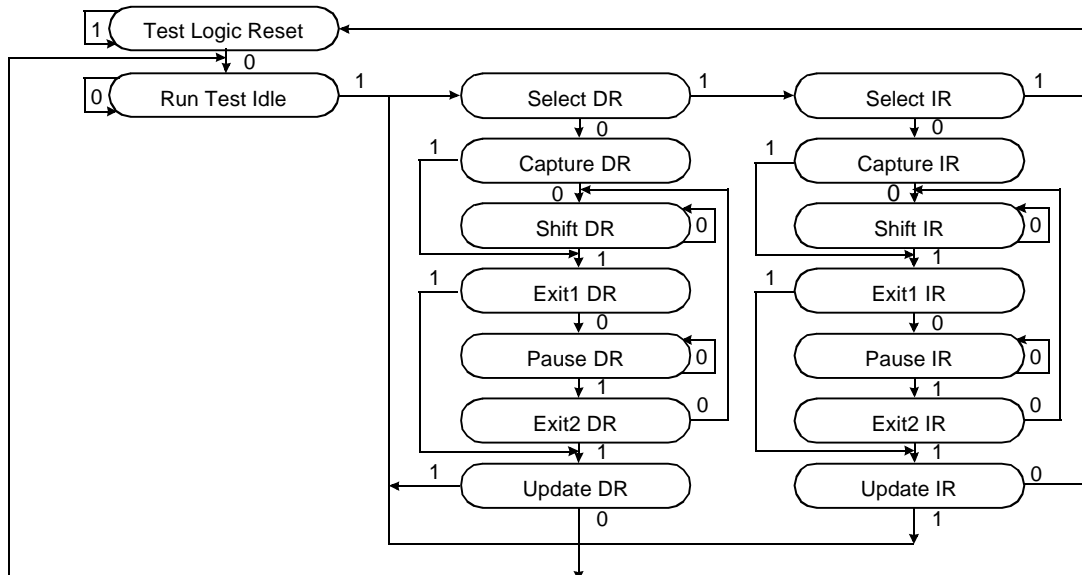
JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	3
0	1	0	SAMPLE-Z	Boundary Scan Register	2
0	1	1	BYPASS	Bypass Register	4
1	0	0	SAMPLE	Boundary Scan Register	5
1	0	1	RESERVED	Do Not Use	6
1	1	0	BYPASS	Bypass Register	4
1	1	1	BYPASS	Bypass Register	4

NOTE :

1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs. This instruction is not IEEE 1149.1 compliant.
2. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
3. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
4. Bypass register is initiated to V_{ss} when BYPASS instruction is invoked. The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
5. SAMPLE instruction dose not places DQs in Hi-Z.
6. This instruction is reserved for future use.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
256Kx36	3 bits	1 bits	32 bits	70 bits
512Kx18	3 bits	1 bits	32 bits	70 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit(0)
256Kx36	0000	00110 00100	XXXXXX	00001001110	1
512Kx18	0000	00111 00011	XXXXXX	00001001110	1

119BGA BOUNDARY SCAN EXIT ORDER(x36)

36	4B	ADV	\overline{OE}	4F	35
37	4E	\overline{CS}_1	A	4G	34
38	4H	\overline{WE}	CLK	4K	33
39	3G	\overline{BW}_c	\overline{CKE}	4M	32
40	3C	A	NC	4A	31
41	3B	A	\overline{BW}_b	5G	30
42	3A	A	A	5C	29
43	2B	CS2	A	5B	28
44	2C	A	A	5A	27
45	2A	A	\overline{CS}_2	6B	26
46	2D	DQPc	A	6A	25
47	1E	DQc	A	6C	24
48	2F	DQc	DQPb	6D	23
49	1G	DQc	DQb	6E	22
50	2H	DQc	DQb	6G	21
51	1D	DQc	DQb	7H	20
52	2E	DQc	DQb	7D	19
53	2G	DQc	DQb	7E	18
54	1H	DQc	DQb	6F	17
55	2K	DQd	DQb	7G	16
56	1L	DQd	DQb	6H	15
57	2M	DQd	DQa	7K	14
58	1N	DQd	DQa	6L	13
59	1P	DQd	DQa	6N	12
60	1K	DQd	DQa	7P	11
61	2L	DQd	DQa	6K	10
62	2N	DQd	DQa	7L	9
63	2P	DQPd	DQa	6M	8
64	3R	\overline{LBO}	DQa	7N	7
65	3L	\overline{BW}_d	DQPa	6P	6
66	2R	A	ZZ	7T	5
67	3T	A	A	6R	4
68	4N	A1	\overline{BW}_a	5L	3
69	4P	A0	A	5T	2
70	2T	NC	A	4T	1

119BGA BOUNDARY SCAN EXIT ORDER(x18)

36	4B	ADV	\overline{OE}	4F	35
37	4E	\overline{CS}_1	A	4G	34
38	4H	\overline{WE}	CLK	4K	33
39	3G	\overline{BW}_b	\overline{CKE}	4M	32
40	3C	A	NC	4A	31
41	3B	A	NC	5G	30
42	3A	A	A	5C	29
43	2B	CS2	A	5B	28
44	2C	A	A	5A	27
45	2A	A	\overline{CS}_2	6B	26
46	2D	NC	A	6A	25
47	1E	NC	A	6C	24
48	2F	NC	NC	7D	23
49	1G	NC	NC	6E	22
50	2H	NC	NC	6G	21
51	1D	DQb	NC	7H	20
52	2E	DQb	DQPa	6D	19
53	2G	DQb	DQa	7E	18
54	1H	DQb	DQa	6F	17
55	2K	DQb	DQa	7G	16
56	1L	DQb	DQa	6H	15
57	2M	DQb	DQa	7K	14
58	1N	DQb	DQa	6L	13
59	2P	DQPb	DQa	6N	12
60	1K	NC	DQa	7P	11
61	2L	NC	NC	6K	10
62	2N	NC	NC	7L	9
63	1P	NC	NC	6M	8
64	3R	\overline{LBO}	NC	7N	7
65	3L	NC	NC	6P	6
66	2R	A	ZZ	7T	5
67	3T	A	A	6R	4
68	4N	A1	\overline{BW}_a	5L	3
69	4P	A0	A	5T	2
70	2T	A	A	6T	1

NOTE : NC ; Dont care.

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V _{DD}	3.135	3.3	3.465	V	
Input High Level (3.3V I/O / 2.5V I/O)	V _{IH}	2.0 / 1.7	-	V _{DD} +0.3	V	1
Input Low Level (3.3V I/O / 2.5V I/O)	V _{IL}	-0.3	-	0.8 / 0.7	V	
Output High Voltage (3.3V I/O / 2.5V I/O)	V _{OH}	2.4 / 2.0	-	-	V	
Output Low Voltage (3.3V I/O / 2.5V I/O)	V _{OL}	-	-	0.4 / 0.4	V	

NOTE : The input level of SRAM pin is to follow the SRAM DC specification.

1. In Case of I/O Pins, the Max. V_{IH}=V_{DDQ}+0.3V

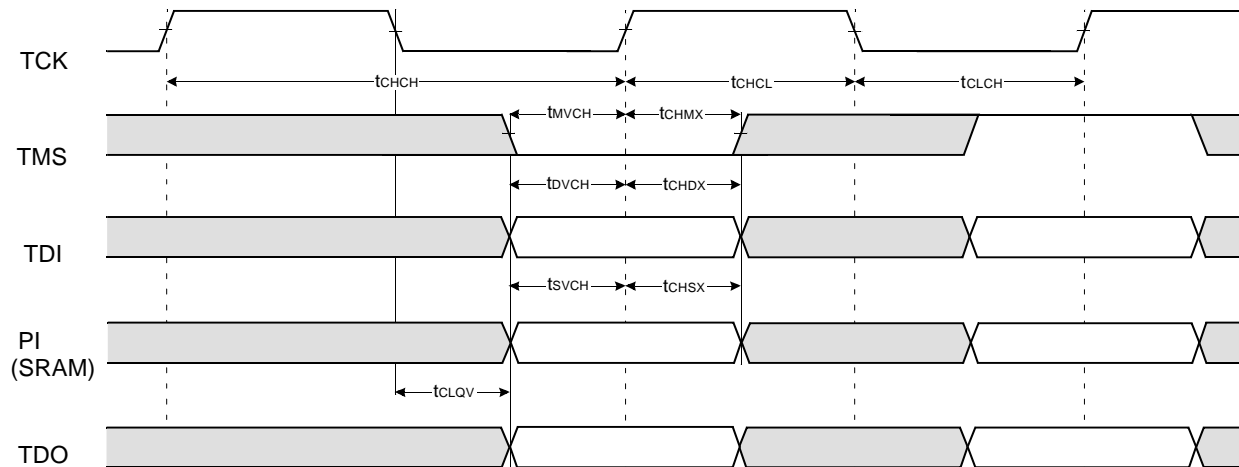
JTAG AC TEST CONDITIONS

Parameter	Symbol	Min	Unit	Note
Input High/Low Level (3.3V I/O / 2.5V I/O)	V _{IH} /V _{IL}	3.0 / 0 , 2.5 / 0	V	
Input Rise/Fall Time (3.3V I/O / 2.5V I/O)	TR/TF	1.0 / 1.0 , 1.0 / 1.0	ns	
Input and Output Timing Reference Level		V _{DDQ} /2	V	

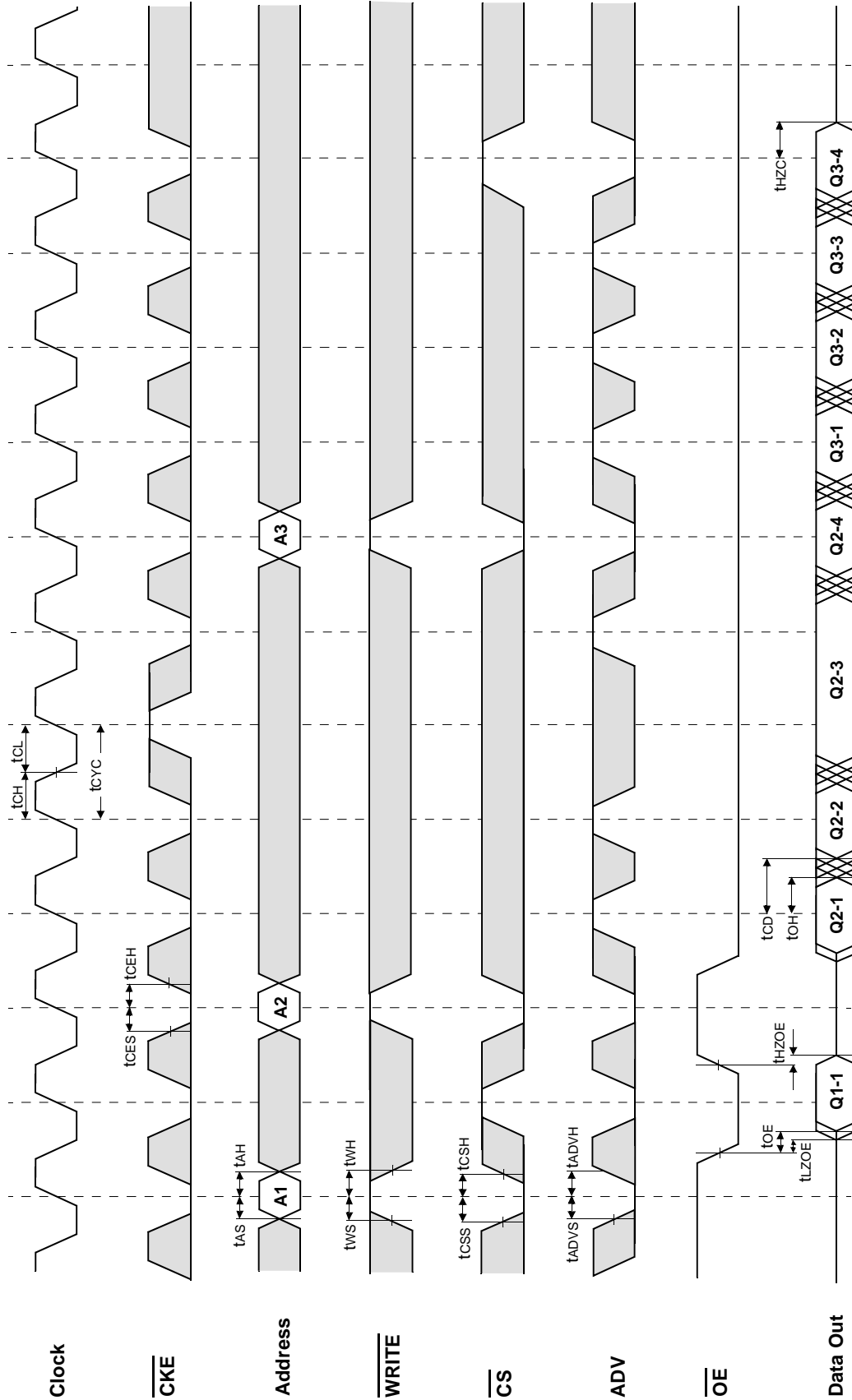
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t _{CHCH}	50	-	ns	
TCK High Pulse Width	t _{CHCL}	20	-	ns	
TCK Low Pulse Width	t _{CLCH}	20	-	ns	
TMS Input Setup Time	t _{MVCH}	5	-	ns	
TMS Input Hold Time	t _{CHMX}	5	-	ns	
TDI Input Setup Time	t _{DVCH}	5	-	ns	
TDI Input Hold Time	t _{CHDX}	5	-	ns	
SRAM Input Setup Time	t _{SVCH}	5	-	ns	
SRAM Input Hold Time	t _{CHSX}	5	-	ns	
Clock Low to Output Valid	t _{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



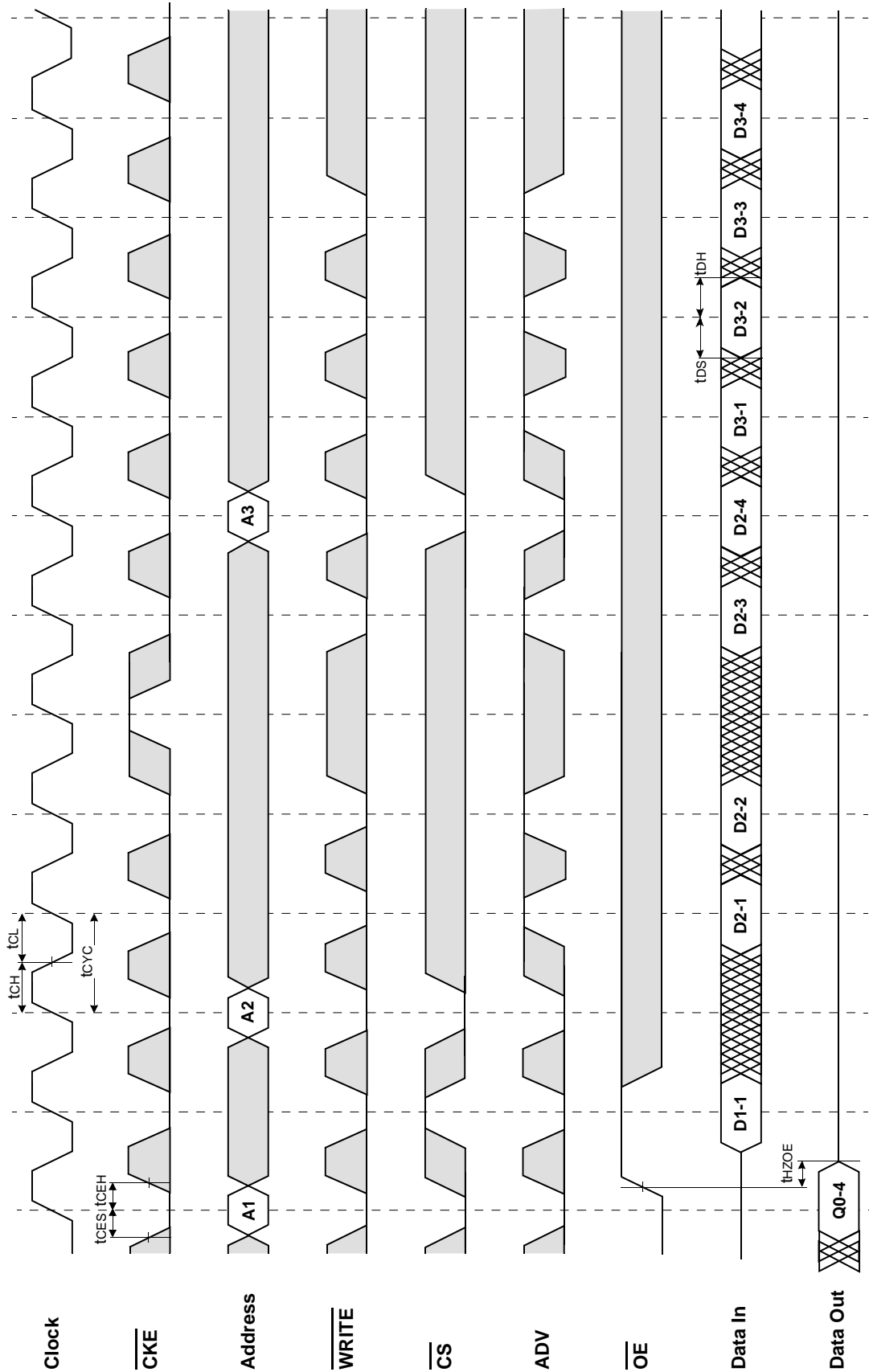
TIMING WAVEFORM OF READ CYCLE



□ Don't Care
 ⊠ Undefined

NOTES : $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS1} = L$, $\overline{CS2} = H$ and $\overline{CS2} = L$
 $\overline{CS} = H$ means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $\overline{CS2} = H$, or $\overline{CS1} = L$, and $\overline{CS2} = L$

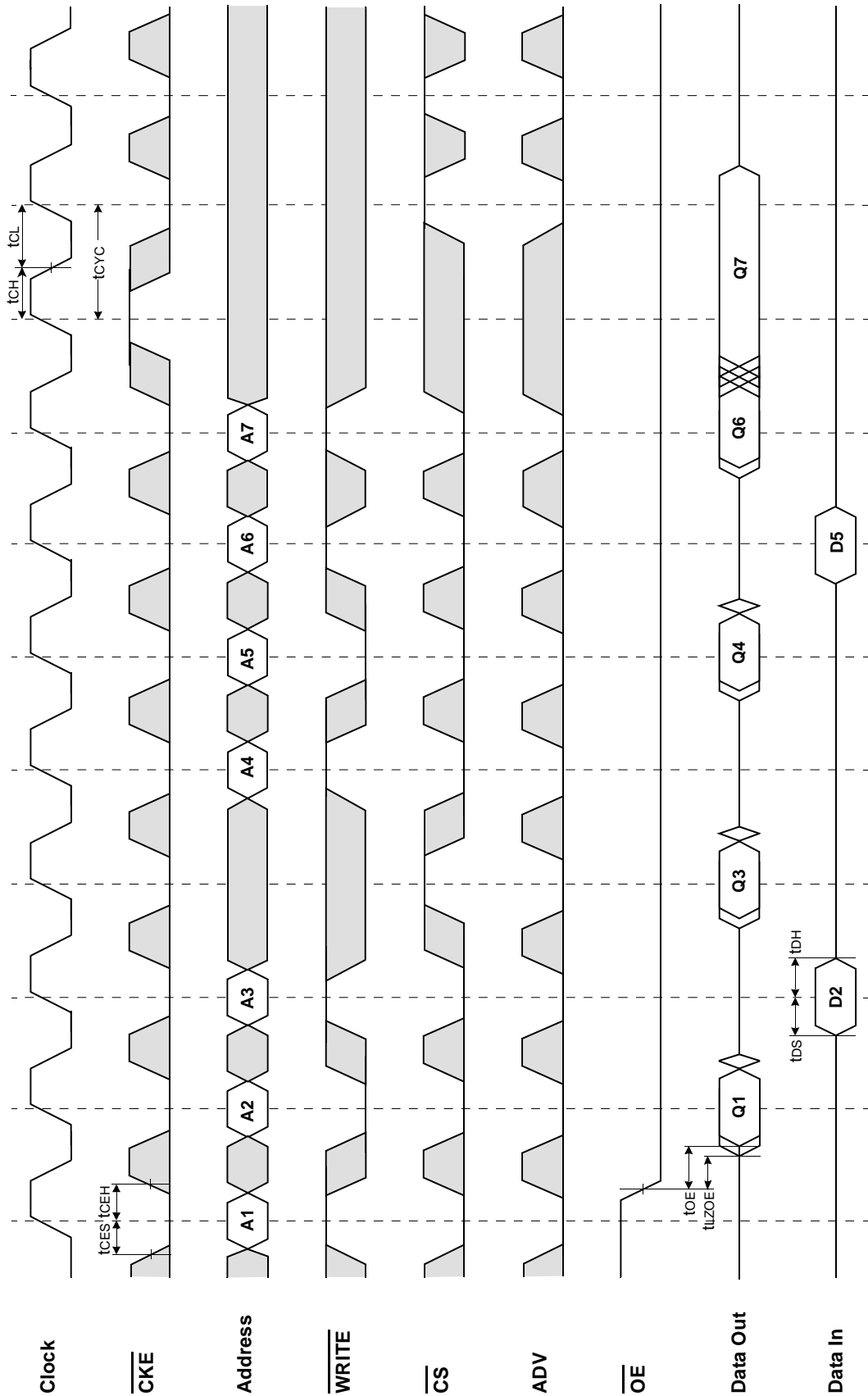
TIMING WAVEFORM OF WRTE CYCLE



□ Don't Care
 ⊗ Undefined

NOTES: $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS1} = L$, $\overline{CS2} = H$ and $\overline{CS2} = L$
 $\overline{CS} = H$ means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $\overline{CS2} = H$, or $\overline{CS1} = L$, and $\overline{CS2} = L$

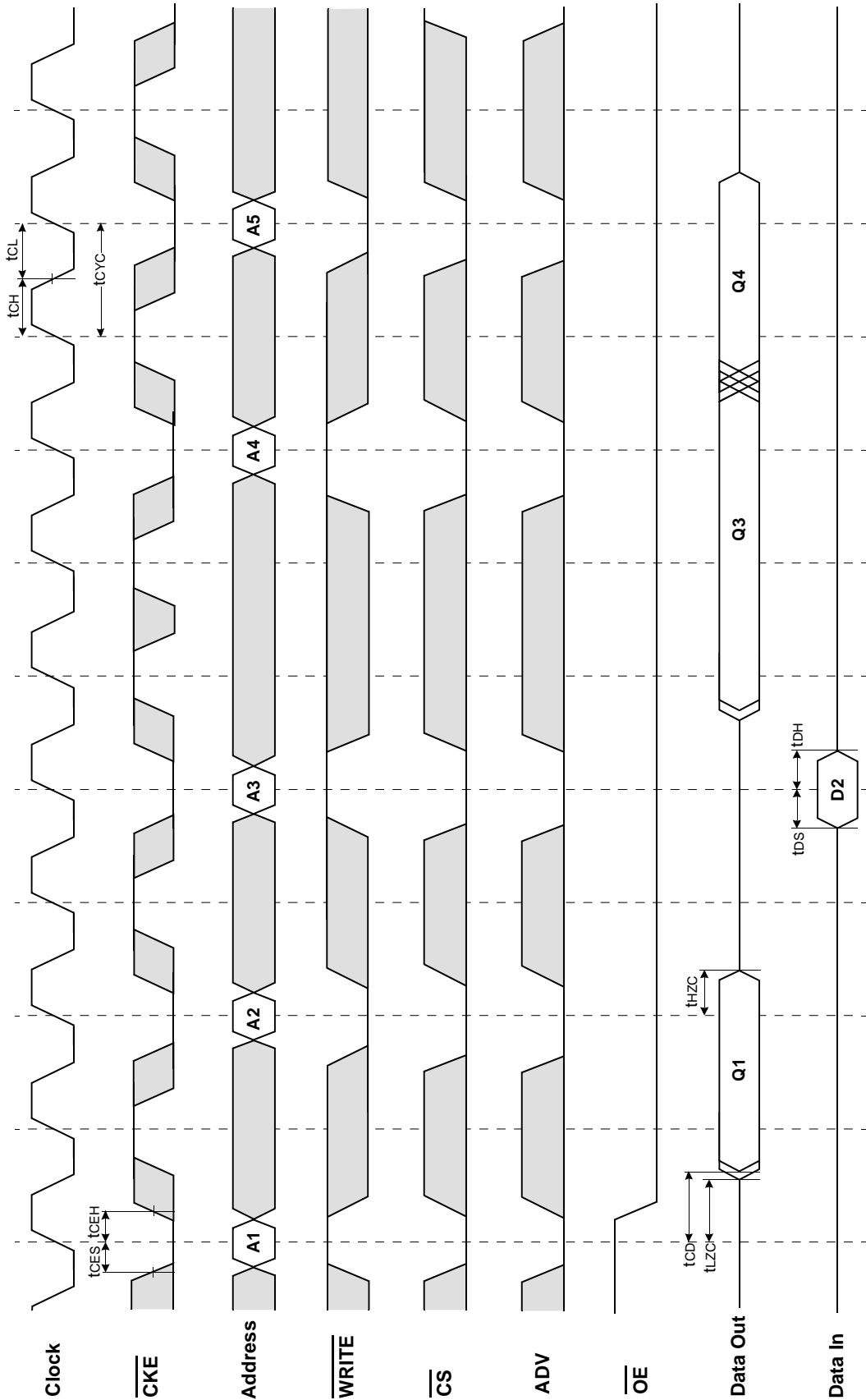
TIMING WAVEFORM OF SINGLE READWRITE



Don't Care
 Undefined

NOTES: $\overline{WRITE} = L$ means $\overline{WE} = L$, and $\overline{BWx} = L$
 $\overline{CS} = L$ means $\overline{CS1} = L$, $\overline{CS2} = H$ and $\overline{CS2} = L$
 $\overline{CS} = H$ means $\overline{CS1} = H$, or $\overline{CS1} = L$ and $\overline{CS2} = H$, or $\overline{CS1} = L$, and $\overline{CS2} = L$

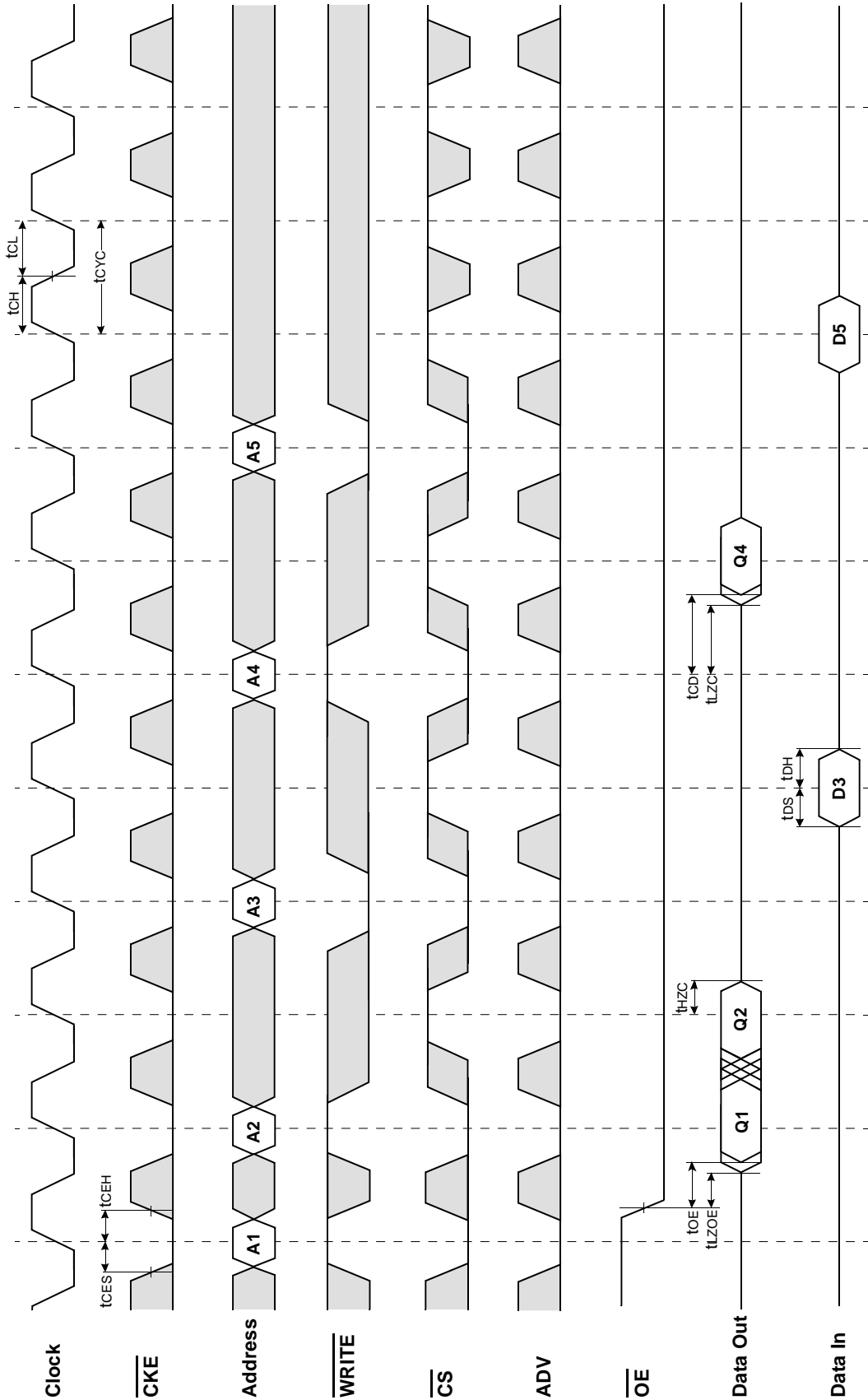
TIMING WAVEFORM OF CKE OPERATION



Don't Care
 Undefined

NOTES : WRITE = L means WE = L, and BWx = L
CS = L means CS1 = L, CS2 = H and CS2 = L
CS = H means CS1 = H, or CS1 = L and CS2 = H, or CS1 = L, and CS2 = L

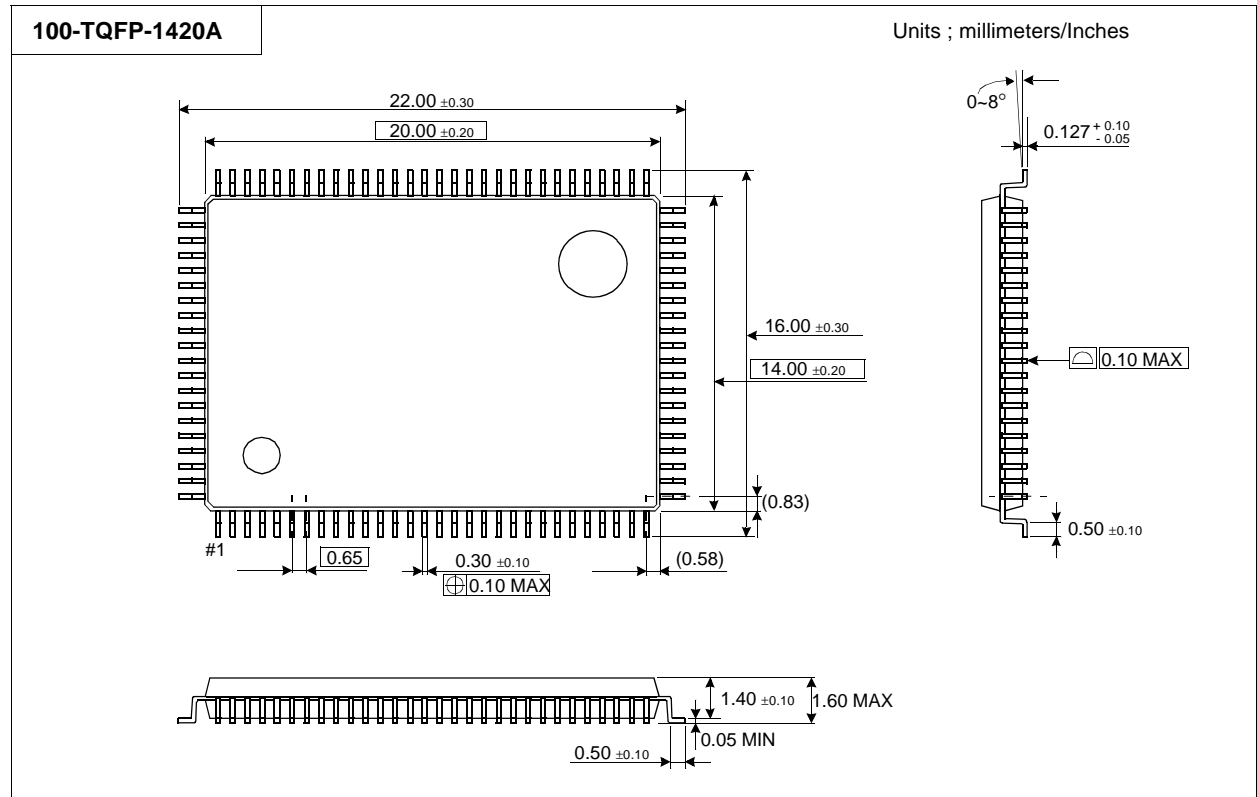
TIMING WAVEFORM OF CS OPERATION



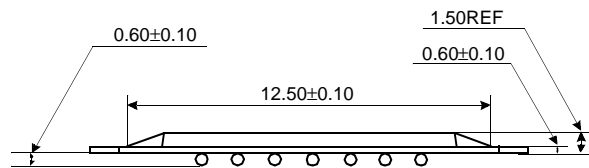
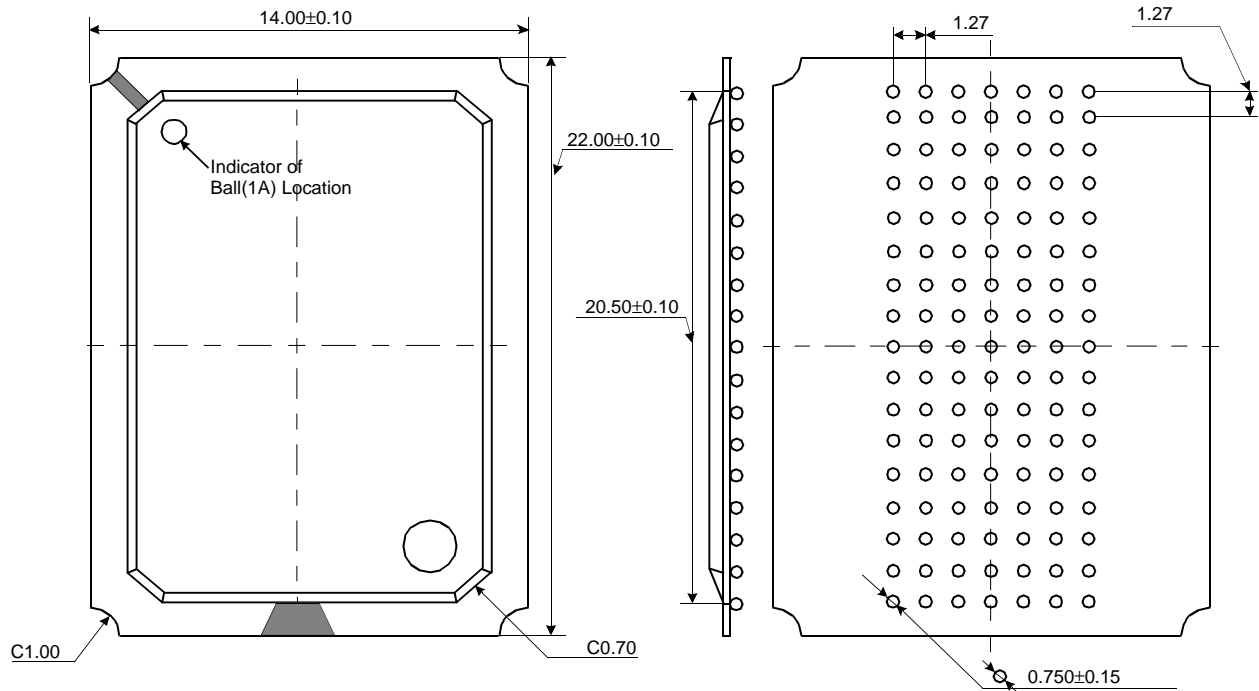
Don't Care
 Undefined

NOTES : WRITE = L means WE = L, and BWx = L
CS = L means CS₁ = L, CS₂ = H and CS₂ = L
CS = H means CS₁ = H, or CS₁ = L and CS₂ = H, or CS₁ = L, and CS₂ = L

PACKAGE DIMENSIONS



119BGA PACKAGE DIMENSIONS



Notes

1. All Dimensions are in Millimeters.
2. Solder Ball to PCB Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.