# 1-of-8 Decoder/Demultiplexer with Address Latch

## High–Performance Silicon–Gate CMOS

The MC74HC137 is identical in pinout to the LS137. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

The HC137 decodes a three–bit Address to one–of–eight active–low outputs. The device has a transparent latch for storage of the Address. Two Chip Selects, one active–low and one active–high, are provided to facilitate the demultiplexing, cascading, and chip–selecting functions.

The demultiplexing function is accomplished by using the Address inputs to select the desired device output, and then by using one of the Chip Selects as a data input while holding the other one active.

The HC137 is the inverting version of the HC237.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2 to 6 V
- Low Input Current: 1 µA
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
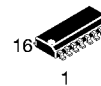- Chip Complexity: 152 FETs or 38 Equivalent Gates
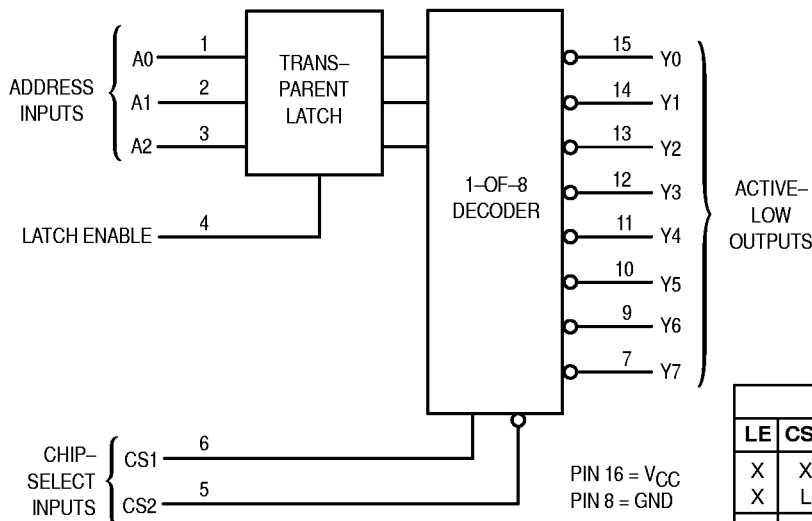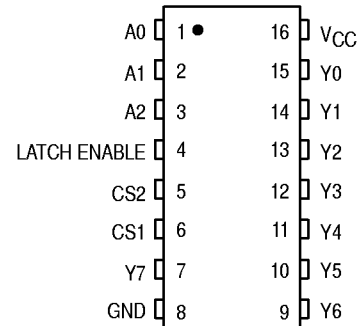
**MC74HC137**
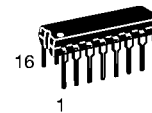
**N SUFFIX**
PLASTIC PACKAGE
CASE 648–08

**D SUFFIX**
SOIC PACKAGE
CASE 751B–05

**ORDERING INFORMATION**

| | |
|---|---|
| MC74HCXXXN | Plastic |
| MC74HCXXXD | SOIC |

**PIN ASSIGNMENT**

| | | | | |
|---|---|---|---|---|
| A0 | 1 | • | 16 | $V_{CC}$ |
| A1 | 2 | | 15 | Y0 |
| A2 | 3 | | 14 | Y1 |
| LATCH ENABLE | 4 | | 13 | Y2 |
| CS2 | 5 | | 12 | Y3 |
| CS1 | 6 | | 11 | Y4 |
| Y7 | 7 | | 10 | Y5 |
| GND | 8 | | 9 | Y6 |

## LOGIC DIAGRAM

ADDRESS INPUTS: A0 (1), A1 (2), A2 (3) → TRANS–PARENT LATCH

LATCH ENABLE (4)

1–OF–8 DECODER

ACTIVE–LOW OUTPUTS: Y0 (15), Y1 (14), Y2 (13), Y3 (12), Y4 (11), Y5 (10), Y6 (9), Y7 (7)

CHIP–SELECT INPUTS: CS1 (6), CS2 (5)

PIN 16 = $V_{CC}$
PIN 8 = GND

## FUNCTION TABLE

| Inputs | | | | | | Outputs | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| LE | CS1 | CS2 | A2 | A1 | A0 | Y0 | Y1 | Y2 | Y3 | Y4 | Y5 | Y6 | Y7 |
| X | X | H | X | X | X | H | H | H | H | H | H | H | H |
| X | L | X | X | X | X | H | H | H | H | H | H | H | H |
| L | H | L | L | L | L | L | H | H | H | H | H | H | H |
| L | H | L | L | L | H | H | L | H | H | H | H | H | H |
| L | H | L | L | H | L | H | H | L | H | H | H | H | H |
| L | H | L | L | H | H | H | H | H | L | H | H | H | H |
| L | H | L | H | L | L | H | H | H | H | L | H | H | H |
| L | H | L | H | L | H | H | H | H | H | H | L | H | H |
| L | H | L | H | H | L | H | H | H | H | H | H | L | H |
| L | H | L | H | H | H | H | H | H | H | H | H | H | L |
| H | H | L | X | X | X | | | | | * | | | |

\* = Depends upon the Address previously applied while LE was at a low level.

# MC74HC137

## MAXIMUM RATINGS*

| Symbol | Parameter | Value | Unit |
|--------|-----------|-------|------|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | − 0.5 to + 7.0 | V |
| $V_{in}$ | DC Input Voltage (Referenced to GND) | − 1.5 to $V_{CC}$ + 1.5 | V |
| $V_{out}$ | DC Output Voltage (Referenced to GND) | − 0.5 to $V_{CC}$ + 0.5 | V |
| $I_{in}$ | DC Input Current, per Pin | ± 20 | mA |
| $I_{out}$ | DC Output Current, per Pin | ± 25 | mA |
| $I_{CC}$ | DC Supply Current, $V_{CC}$ and GND Pins | ± 50 | mA |
| $P_D$ | Power Dissipation in Still Air        Plastic DIP†<br>SOIC Package† | 750<br>500 | mW |
| $T_{stg}$ | Storage Temperature | − 65 to + 150 | °C |
| $T_L$ | Lead Temperature, 1 mm from Case for 10 Seconds<br>(Plastic DIP or SOIC Package) | 260 | °C |

\* Maximum Ratings are those values beyond which damage to the device may occur.
  Functional operation should be restricted to the Recommended Operating Conditions.
†Derating  — Plastic DIP: − 10 mW/°C from 65° to 125°C
              SOIC Package: − 7 mW/°C from 65° to 125°C
For high frequency or heavy load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

## RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min | Max | Unit |
|--------|-----------|-----|-----|------|
| $V_{CC}$ | DC Supply Voltage (Referenced to GND) | 2.0 | 6.0 | V |
| $V_{in}$, $V_{out}$ | DC Input Voltage, Output Voltage (Referenced to GND) | 0 | $V_{CC}$ | V |
| $T_A$ | Operating Temperature, All Package Types | − 55 | + 125 | °C |
| $t_r$, $t_f$ | Input Rise and Fall Time        $V_{CC}$ = 2.0 V<br>(Figure 2)        $V_{CC}$ = 4.5 V<br>        $V_{CC}$ = 6.0 V | 0<br>0<br>0 | 1000<br>500<br>400 | ns |

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

| Symbol | Parameter | Test Conditions | $V_{CC}$ V | Guaranteed Limit − 55 to 25°C | ≤ 85°C | ≤ 125°C | Unit |
|--------|-----------|-----------------|-----------|-------------------------------|--------|---------|------|
| $V_{IH}$ | Minimum High–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$|I_{out}|$ ≤ 20 µA | 2.0<br>4.5<br>6.0 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | 1.5<br>3.15<br>4.2 | V |
| $V_{IL}$ | Maximum Low–Level Input Voltage | $V_{out}$ = 0.1 V or $V_{CC}$ − 0.1 V<br>$|I_{out}|$ ≤ 20 µA | 2.0<br>4.5<br>6.0 | 0.3<br>0.9<br>1.2 | 0.3<br>0.9<br>1.2 | 0.3<br>0.9<br>1.2 | V |
| $V_{OH}$ | Minimum High–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$|I_{out}|$ ≤ 20 µA | 2.0<br>4.5<br>6.0 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | 1.9<br>4.4<br>5.9 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$   $|I_{out}|$ ≤ 4.0 mA<br>$|I_{out}|$ ≤ 5.2 mA | 4.5<br>6.0 | 3.98<br>5.48 | 3.84<br>5.34 | 3.70<br>5.20 | |
| $V_{OL}$ | Maximum Low–Level Output Voltage | $V_{in}$ = $V_{IH}$ or $V_{IL}$<br>$|I_{out}|$ ≤ 20 µA | 2.0<br>4.5<br>6.0 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | 0.1<br>0.1<br>0.1 | V |
| | | $V_{in}$ = $V_{IH}$ or $V_{IL}$   $|I_{out}|$ ≤ 4.0 mA<br>$|I_{out}|$ ≤ 5.2 mA | 4.5<br>6.0 | 0.26<br>0.26 | 0.33<br>0.33 | 0.40<br>0.40 | |
| $I_{in}$ | Maximum Input Leakage Current | $V_{in}$ = $V_{CC}$ or GND | 6.0 | ± 0.1 | ± 1.0 | ± 1.0 | µA |
| $I_{CC}$ | Maximum Quiescent Supply Current (per Package) | $V_{in}$ = $V_{CC}$ or GND<br>$I_{out}$ = 0 µA | 6.0 | 8 | 80 | 160 | µA |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

## AC ELECTRICAL CHARACTERISTICS ($C_L$ = 50 pF, Input $t_r$ = $t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | − 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{PLH}$ | Maximum Propagation Delay, Input A to Output Y (Figures 1 and 6) | 2.0 4.5 6.0 | 170 34 29 | 215 43 37 | 255 51 43 | ns |
| $t_{PHL}$ | | 2.0 4.5 6.o | 240 48 41 | 300 60 51 | 360 72 61 | |
| $t_{PLH}$ | Maximum Propagation Delay, CS1 or CS2 to Output Y (Figures 2, 3 and 6) | 2.0 4.5 6.0 | 150 30 26 | 190 38 33 | 225 45 38 | ns |
| $t_{PHL}$ | | 2.0 4.5 6.0 | 195 39 33 | 245 49 42 | 295 59 50 | |
| $t_{PLH}$ | Maximum Propagation Delay, Latch Enable to Output Y (Figures 4 and 6) | 2.0 4.5 6.0 | 175 35 30 | 220 44 37 | 265 53 45 | ns |
| $t_{PHL}$ | | 2.0 4.5 6.0 | 250 50 43 | 315 63 54 | 375 75 64 | |
| $t_{TLH}$, $t_{THL}$ | Maximum Output Transition Time, Any Output (Figures 2 and 6) | 2.0 4.5 6.0 | 75 15 13 | 95 19 16 | 110 22 19 | ns |
| $C_{in}$ | Maximum Input Capacitance | — | 10 | 10 | 10 | pF |

NOTES:
1. For propagation delays with loads other than 50 pF, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).
2. Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

| | | Typical @ 25°C, $V_{CC}$ = 5.0 V | |
|---|---|---|---|
| $C_{PD}$ | Power Dissipation Capacitance (Per Package)* | 100 | pF |

* Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$. For load considerations, see Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

## TIMING REQUIREMENTS (Input $t_r$ = $t_f$ = 6 ns)

| Symbol | Parameter | $V_{CC}$ V | Guaranteed Limit | | | Unit |
|---|---|---|---|---|---|---|
| | | | − 55 to 25°C | ≤ 85°C | ≤ 125°C | |
| $t_{su}$ | Minimum Setup Time, Input A to Latch Enable (Figure 5) | 2.0 4.5 6.0 | 100 20 17 | 125 25 21 | 150 30 26 | ns |
| $t_h$ | Minimum Hold Time, Latch Enable to Input A (Figure 5) | 2.0 4.5 6.0 | 50 10 9 | 65 13 11 | 75 15 13 | ns |
| $t_w$ | Minimum Pulse Width, Latch Enable (Figure 4) | 2.0 4.5 6.0 | 80 16 14 | 100 20 17 | 120 24 20 | ns |
| $t_r$, $t_f$ | Maximum Input Rise and Fall Times (Figure 2) | 2.0 4.5 6.0 | 1000 500 400 | 1000 500 400 | 1000 500 400 | ns |

NOTE: Information on typical parametric values can be found in Chapter 2 of the Motorola High–Speed CMOS Data Book (DL129/D).

# PIN DESCRIPTIONS

## ADDRESS INPUTS

### A0, A1, A2 (Pins 1, 2, 3)

Address inputs. These inputs, when the chip is enabled, determine which of the eight outputs is selected.

## CONTROL INPUTS

### CS1, CS2 (Pins 6, 5)

Chip–Select inputs. For CS1 at a high level and CS2 at a low level, the chip is enabled and the outputs follow the address inputs (Latch Enable = L). For any other combination of CS1 and CS2, the outputs are at a high level.

### Latch Enable (Pin 4)

Latch–Enable input. A high level at this input latches the Address. A low level at this input allows the outputs to follow the data at the Address pins (CS1 = H and CS2 = L).

## OUTPUTS

### Y0 – Y7

Active–low outputs. One of these eight outputs is selected when the chip is enabled (CS1 = H and CS2 = L) and the data on the A0, A1, and A2 inputs correspond to that particular output. The selected output is at a low level while all others remain at a high level.

## SWITCHING WAVEFORMS
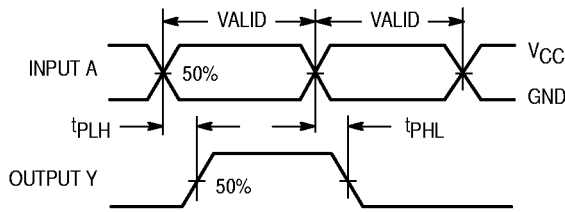


**Figure 1.**
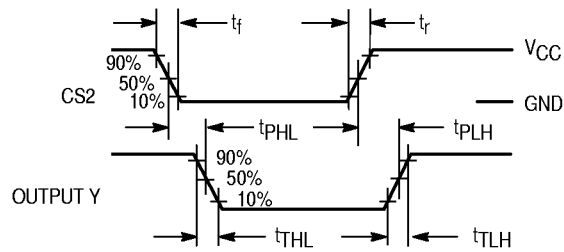


**Figure 2.**
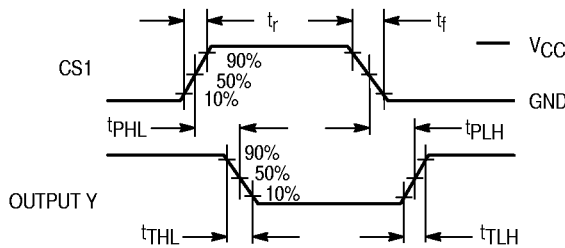


**Figure 3.**
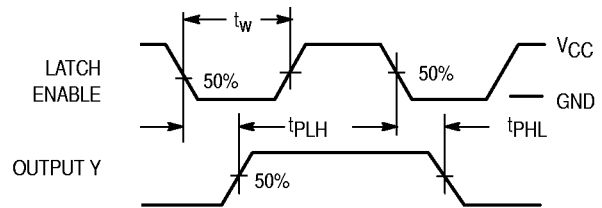


**Figure 4.**
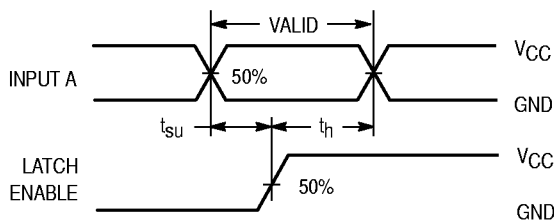


**Figure 5.**
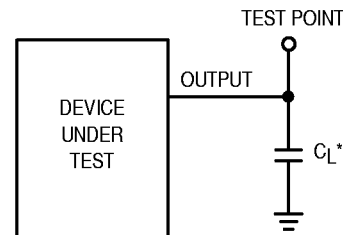


* Includes all probe and jig capacitance

**Figure 6. Test Circuit**

**EXPANDED LOGIC DIAGRAM**
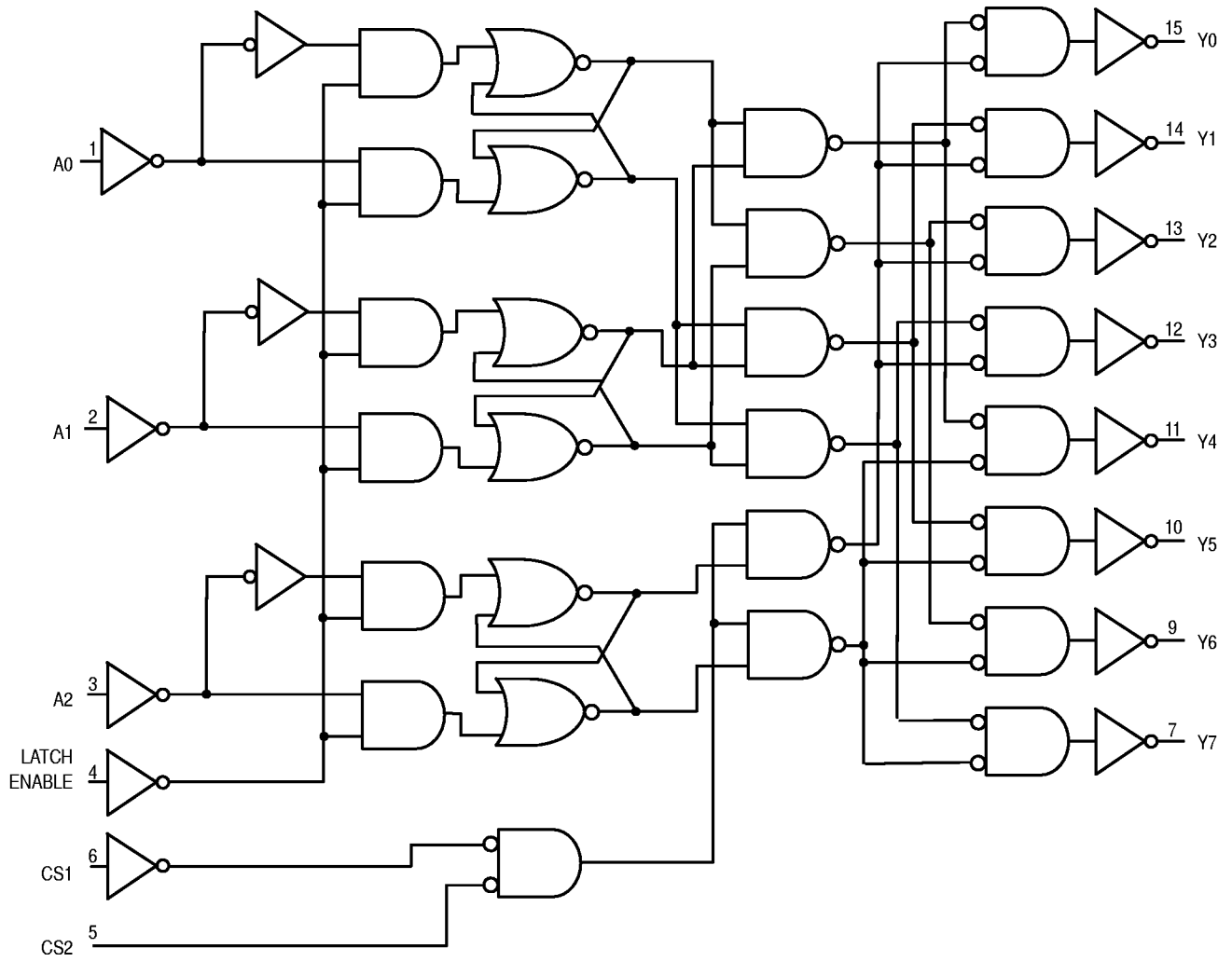
# OUTLINE DIMENSIONS

**N SUFFIX**
PLASTIC PACKAGE
CASE 648–08
ISSUE R
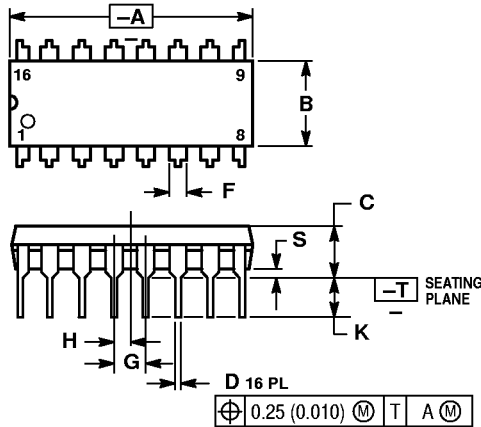
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

| DIM | INCHES | | MILLIMETERS | |
|-----|--------|--------|-------------|--------|
| | MIN | MAX | MIN | MAX |
| A | 0.740 | 0.770 | 18.80 | 19.55 |
| B | 0.250 | 0.270 | 6.35 | 6.85 |
| C | 0.145 | 0.175 | 3.69 | 4.44 |
| D | 0.015 | 0.021 | 0.39 | 0.53 |
| F | 0.040 | 0.070 | 1.02 | 1.77 |
| G | 0.100 BSC | | 2.54 BSC | |
| H | 0.050 BSC | | 1.27 BSC | |
| J | 0.008 | 0.015 | 0.21 | 0.38 |
| K | 0.110 | 0.130 | 2.80 | 3.30 |
| L | 0.295 | 0.305 | 7.50 | 7.74 |
| M | 0° | 10° | 0° | 10° |
| S | 0.020 | 0.040 | 0.51 | 1.01 |

⊕ | 0.25 (0.010) Ⓜ | T | A Ⓜ

**D SUFFIX**
PLASTIC SOIC PACKAGE
CASE 751B–05
ISSUE J
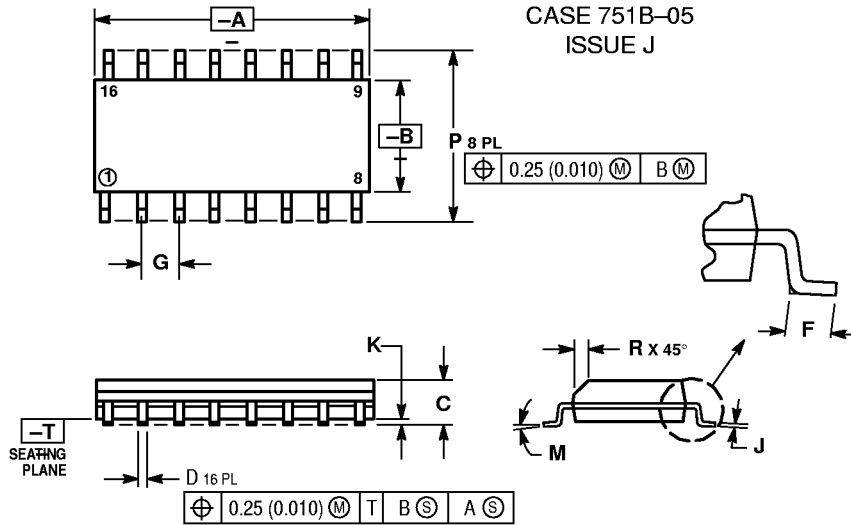
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

⊕ | 0.25 (0.010) Ⓜ | B Ⓜ

| DIM | MILLIMETERS | | INCHES | |
|-----|-------------|--------|--------|--------|
| | MIN | MAX | MIN | MAX |
| A | 9.80 | 10.00 | 0.386 | 0.393 |
| B | 3.80 | 4.00 | 0.150 | 0.157 |
| C | 1.35 | 1.75 | 0.054 | 0.068 |
| D | 0.35 | 0.49 | 0.014 | 0.019 |
| F | 0.40 | 1.25 | 0.016 | 0.049 |
| G | 1.27 BSC | | 0.050 BSC | |
| J | 0.19 | 0.25 | 0.008 | 0.009 |
| K | 0.10 | 0.25 | 0.004 | 0.009 |
| M | 0° | 7° | 0° | 7° |
| P | 5.80 | 6.20 | 0.229 | 0.244 |
| R | 0.25 | 0.50 | 0.010 | 0.019 |

⊕ | 0.25 (0.010) Ⓜ | T | B Ⓢ | A Ⓢ

Ⓜ **MOTOROLA**

◇ CODELINE