High-Speed CMOS 16Kx4 SRAM with Output Enable

QS8886A
Preliminary

- High Speed Access and Cycle times
- 8ns/10ns/12ns/15ns Commercial
- 10ns/12ns/15ns/20ns Military
- Output Enable feature
- Low power, high-speed QCMOS™ technology
- Military product compliant to MIL-STD-883, Class B
- 6-Transistor cell for high reliability
- TTL Compatible I/O
- Available in PDIP,CERDIP, LCC, SOJ, and 150 mil QSOP packages
- Low Standby current
- JEDEC standard pinout

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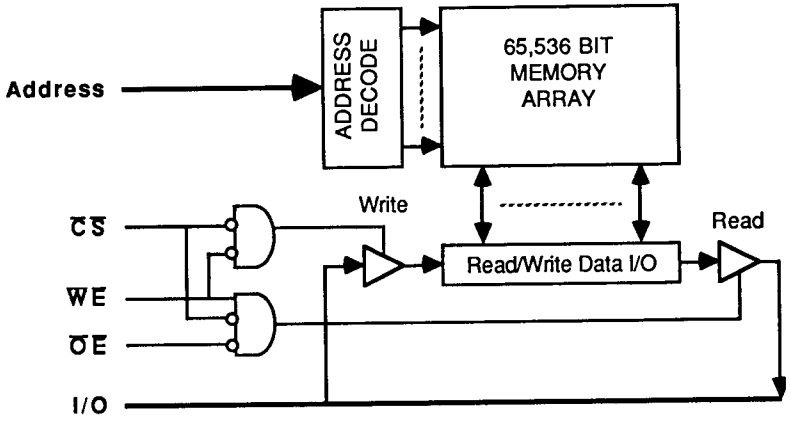
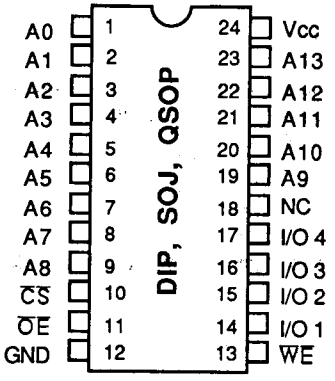
DESCRIPTION

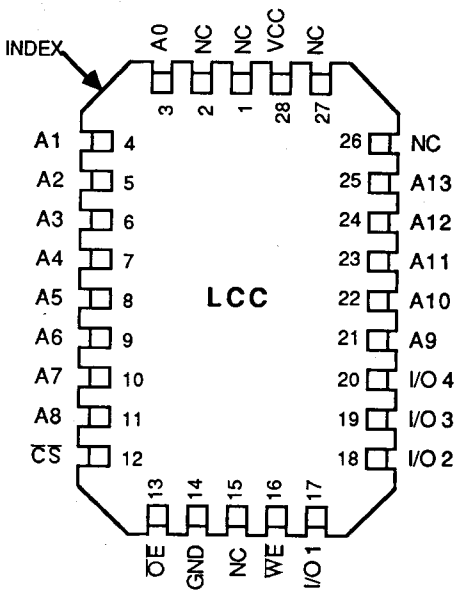
The QS8886A is a high-speed 64K SRAM organized as 16Kx4. The 8886 is manufactured in a high-performance CMOS process, and is based on a 6-transistor cell design for high reliability and radiation tolerance. High-speed access time makes the 8886A useful for cache data RAM, cache tag RAMs, high-speed scratchpad memories, and look-up tables. Low operating power and excellent latch-up and ESD protection are provided. The QS8886A is offered in a variety of packages, including the 150 mil QSOP which provides the smallest footprint of any SRAM.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATIONS





ALL PINS TOP VIEW

PIN DESCRIPTION

Pin Name	I/O	Function
A	I	Address
I/O 1-4	I/O	Data
$\overline{CS}$	I	Chip Select
$\overline{WE}$	I	Write Enable
$\overline{OE}$	I	Output Enable

FUNCTION TABLE

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	I/O	Power	Function
H	X	X	High Z	Standby	Deselect
L	H	L	Data Out	Active	Read
L	L	X	Data In	Active	Write
L	X	H	High Z	Active	Tri-State

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground..... -0.5V to +7.0V
DC Output Voltage V_O ..... -0.5V to V_{CC} + 0.5V DC
Input Voltage V_I ..... -0.5V to V_{CC} + 0.5V
AC Input Voltage (for a pulse width ≤20 ns)..... -3.0V
DC Output Current Max. sink current/pin..... 50 mA
DC Output Current Max. source current/pin..... 30 mA
T_{BIAS} Temperature Under Bias, COM..... -65° to +125°C
T_{STG} Storage Temperature, COM..... -65° to +125°C
T_{BIAS} Temperature Under Bias, MIL..... -65° to +135°C
T_{STG} Storage Temperature, MIL..... -65° to +155°C

Note: Stresses above those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to the maximum ratings for extended periods may affect reliability.

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RECOMMENDED OPERATING RANGES

Parameter		Commercial		Military		Units
		Min	Max	Min	Max	
Ta	Ambient Operating Temperature	0	70	-55	125	deg
Vcc	Supply voltage	4.5	5.5	4.5	5.5	V
Vcc	Supply voltage (8 ns coml. only)	4.75	5.25			V

CAPACITANCE

Ta=+25°C, f=1 MHz

Name	Description	Package	Typ	Max	Unit
Cin	Input Capacitance Vin = 0 V	PDIP	3	6	pF
		SOJ	2.5	5	pF
		QSOP		4	pF
Cout	Output Capacitance Vout = 0 V	PDIP		7	pF
		SOJ		7	pF
		QSOP		6	pF

Note: Capacitance is measured at characterization but not tested at final production.

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	Test Conditions	Commercial		Military		Unit
			Min	Max	Min	Max	
Vih	Input HIGH Voltage	Logic High for All Inputs	2.2	6.0	2.2	6.0	Volts
Vil	Input LOW Voltage (1)	Logic Low for All Inputs		0.8		0.8	
Voh	Output HIGH Voltage	Ioh = -4 mA, Vcc = MIN	2.4		2.4		
Vol	Output LOW Voltage	Iol = 8 mA, Vcc = MIN		0.4		0.4	
| Ili |	Input Leakage	Vcc = MAX, Vin = GND to Vcc		5		10	µA
| Ilo |	Output Leakage	Vcc = MAX, Vout = GND to Vcc		5		10	

Notes:
1. Transient inputs with Vil not more negative than -3.0 volts are permitted for pulse widths < 20 ns.

POWER SUPPLY CHARACTERISTICS

Vlc = 0.2 V, Vhc = Vcc - 0.2V At f = 0, no input lines switch; At f = f MAX, RAM is cycling at 1 / t RC

Symbol	Parameter	-8	-10		-12		15		-20		Unit
			C	M	C	M	C	M	C	M	
Icc	Dynamic Operating Current, Vcc = MAX Outputs open CS ≤ Vil, f = f MAX		145	165	135	155	125	145	120	140	mA
Isb	TTL Standby Current, Vcc = MAX Outputs open CS ≥ Vih, f = f MAX		60	70	60	70	60	70	60	70	
Isb1	Full Standby Current, Vcc = MAX Outputs open CS ≥ Vhc, f = 0 Vin ≤ Vlc or Vin ≥ Vhc		15	20	15	20	15	20	15	20	

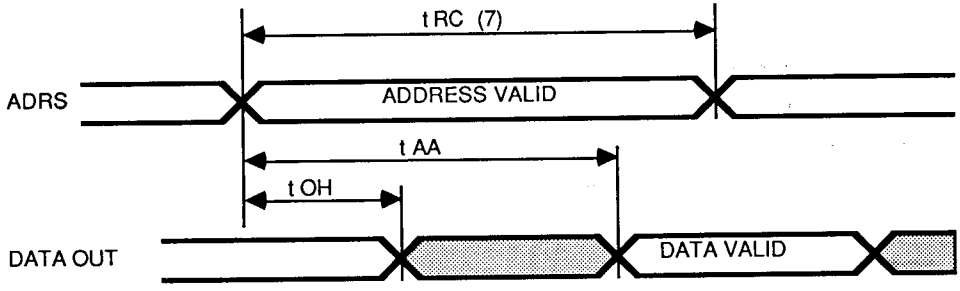
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Symbol	Parameter	-8		-10		-12		-15		-20	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
READ											
t RC	Read Cycle Time (1)	8		10		12		15		19	
t AA	Address Access Time		8		10		12		15		19
t ACS	Chip Select Access Time		8		10		12		15		19
t OH	Output Hold fromAddress Change	1.5		2		2		2		3	
t CLZ	Chip Select to Output in Low Z (2)	1.5		2		2		2		2	
t CHZ	Chip Select to Output in High Z (2,3)		4		4		5		7		8
t OE	Output Enable to Data Valid		4		5		6		6		8
t OLZ	Output Enable to Output in Low Z (2)	1.5		2		2		2		2	
t OHZ	Output Enable to Output in High Z (2,3)		4		4		4		5		7
t PU	Chip Select to Power Up Time (2)	0		0		0		0		0	
t PD	Chip Select to Power Down Time (2)	8		10		12		15		19	

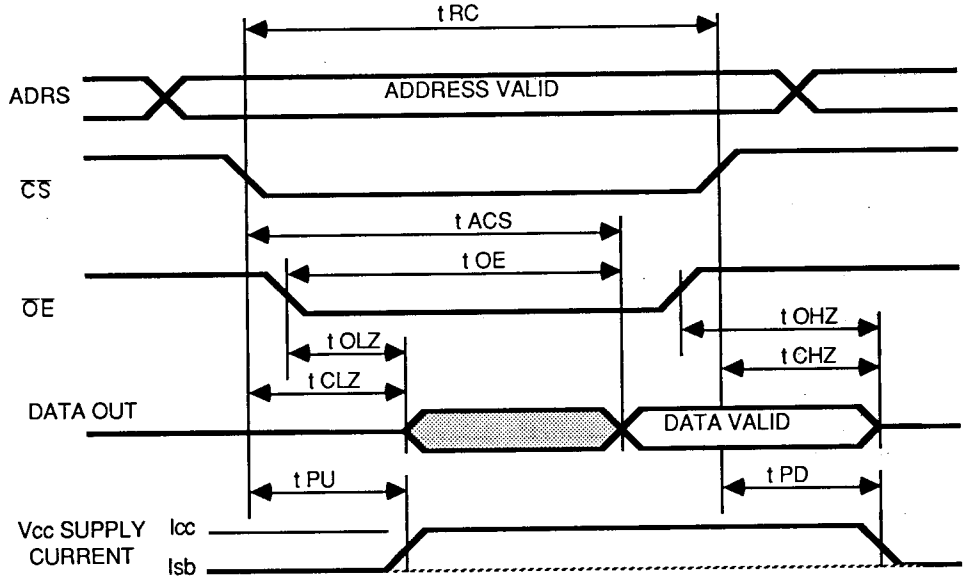
Notes:
1) See Test Circuit and Waveforms. Minimums guaranteed but not tested.
2) This parameter is guaranteed by design but not tested.
3) Transition to Hi-Z is measured ± 200 mV change from the prior steady state voltage.

Symbol	Parameter	-8		-10		-12		-15		-20	
		Min	Max	Min	Max	Min	Max	Min	Max	Min	Max
WRITE CYCLE											
t WC	Write Cycle Time	8		10		12		15		19	
t CW	Chip Select Valid to End of Write	7		8		10		13		17	
t AW	Address Valid to End of Write	7		8		10		13		17	
t AS	Address Setup Time	0		0		0		0		0	
t WP	Write Pulse width	7		8		10		12		16	
t WR	Write Recovery Time	0		0		0		0		0	
t DW	Data Valid to End of Write	4		5		6		8		10	
t DH	Data Hold Time	0		0		0		0		0	
t WZ	Write Enable to Output in High Z (2,3)		3		4		5		6		7
t OW	Write Enable to Output in Low Z (2)	1.5		2		2		2		2	

TIMING WAVEFORMS - READ CYCLE NO. 1 (4, 5)



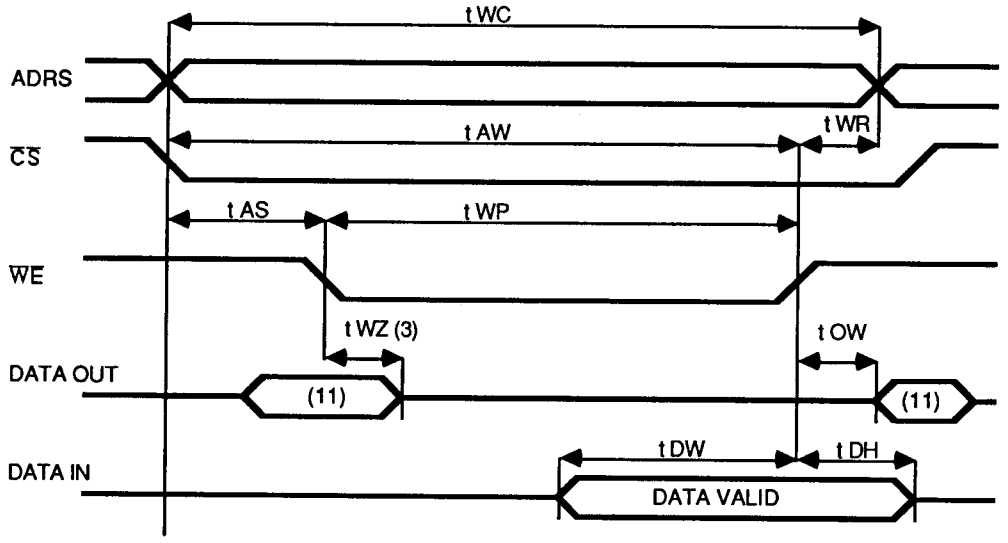
TIMING WAVEFORMS - READ CYCLE NO. 2 (4, 6)



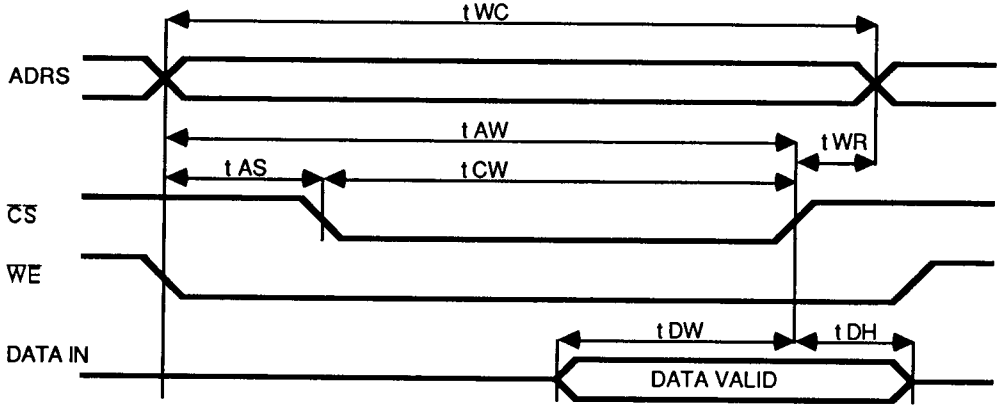
Notes:

4. WE is high for Read cycle.
5. CS is low for Read cycle #1.
6. Address is valid prior to or coincident with CS transition time for Read Cycle #2.
7. All read timings are referenced from the last valid address to the first transitioning address.

TIMING WAVEFORMS-WRITE CYCLE No. 1 (8,9,10 $\overline{WE}$ controlled timing)



TIMING WAVEFORMS-WRITE CYCLE No. 2 (8,9,10,12 $\overline{CS}$ controlled timing)



Notes:
8. $\overline{WE}$ or $\overline{CS}$ must be high during address transitions.
9. A write occurs during the overlap of a low $\overline{CS}$ and a low $\overline{WE}$. Either signal going high will terminate the write.
10. t WR is measured from the earlier of $\overline{CS}$ and $\overline{WE}$ going high to end of the write cycle.
11. During this period the I/O pins are in the output state and input signals must not be applied.
12. If the $\overline{CS}$ low transition occurs simultaneously with or after the $\overline{WE}$ low transition, the output remains in the high impedance state.