

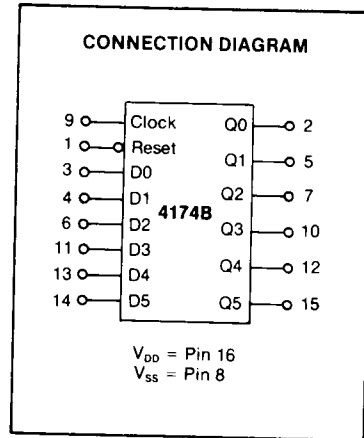
# CMOS HEX TYPE D FLIP-FLOP

**FEATURES:**

- **Static Operation**
- **All Inputs and Outputs Buffered**
- **Diode Protection on All Inputs**
- **Supply Voltage Range = 3.0 Vdc to 18 Vdc**
- **Output Compatible with Two HTL Loads, Two Low-Power TTL Loads or One Low-Power Schottky TTL Load**
- **Functional Equivalent to TTL 74174**

**DESCRIPTION:**

The 4174B hex type D flip-flop is constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. Data on the D inputs which meets the setup time requirements is transferred to the Q outputs on the positive edge of the clock pulse. All six flip-flops share common clock and reset inputs. The reset is active low, and independent of the clock.



**MAXIMUM RATINGS** (Voltages referenced to V<sub>SS</sub>)

Rating	Symbol	Value	Unit
DC Supply Voltage	V <sub>DD</sub>	-0.5 to +18	Vdc
Input Voltage, All Inputs	V <sub>in</sub>	-0.5 to V <sub>DD</sub> +0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range—C, D, F, H E	T <sub>a</sub>	-55 to +125 -40 to +85	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V<sub>in</sub> and V<sub>out</sub> be constrained to the range V<sub>SS</sub> < (V<sub>in</sub> or V<sub>out</sub>) < V<sub>DD</sub>.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V<sub>SS</sub> or V<sub>DD</sub>).

**TRUTH TABLE  
(Positive Logic)**

Clock	INPUTS		OUTPUT
	Data	Reset	Q
	0	1	0
	1	1	1
	X	1	Q
X	X	0	0

No Change

X = Don't Care

SWITCHING CHARACTERISTICS\* ( $C_L = 50 \text{ pF}$ ,  $T_A = 25^\circ\text{C}$ )

Characteristic	Symbol	$V_{DD}$ Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise and Fall Time	$t_r, t_f$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Propagation Delay Time—Clock to Q	$t_{PLH}, t_{PHL}$	5.0	—	150	300	ns
		10	—	70	140	
		15	—	50	100	
Propagation Delay Time—Reset to Q	$t_{PHL}$	5.0	—	250	500	ns
		10	—	100	200	
		15	—	75	150	
Minimum Clock Pulse Width	$PW_C$	5.0	—	75	150	ns
		10	—	45	90	
		15	—	35	70	
Minimum Reset Pulse Width	$PW_R$	5.0	—	100	200	ns
		10	—	50	100	
		15	—	40	80	
Maximum Clock Pulse Frequency	PRF	5.0	2.0	7.0	—	MHz
		10	5.0	12.0	—	
		15	6.5	15.5	—	
Maximum Clock Pulse Rise and Fall Time	$t_r, t_f$	5.0	15	—	—	$\mu\text{s}$
		10	15	—	—	
		15	15	—	—	
Data Setup Time	$t_{setup}$	5.0	—	20	40	ns
		10	—	10	20	
		15	—	0	15	
Data Hold Time	$t_{hold}$	5.0	—	40	80	ns
		10	—	20	40	
		15	—	15	30	
Reset Removal Time**	$t_{rem}$	5.0	—	125	250	ns
		10	—	50	100	
		15	—	40	80	

\*The formulas given are for the typical characteristics only.

\*\*The reset signal must be high prior to a positive-going transition of the clock.

STATIC CHARACTERISTICS<sup>1</sup>

PARAMETER	$V_{DD}$ (Vdc)	CONDITIONS	$T_{LOW}$ <sup>2</sup>		+25°C			$T_{HIGH}$ <sup>2</sup>		Units
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
QUIESCENT DEVICE CURRENT	$I_{DD}$	$V_{IN} = V_{SS}$ or $V_{DD}$ All valid input combinations	—	5	—	0.005	5	—	150	$\mu\text{A}_{dc}$
			—	10	—	0.010	10	—	300	
			—	20	—	0.015	20	—	600	

NOTES: <sup>1</sup> Remaining Static Electrical Characteristics are listed under "4000B Series Family Specifications".

<sup>2</sup>  $T_{LOW} = -55^\circ\text{C}$  for C, D, H device.

=  $-40^\circ\text{C}$  for E device.

$T_{HIGH} = +125^\circ\text{C}$  for C, D, F, H device.

=  $+85^\circ\text{C}$  for E device.

