PERICOM®

PI74FCT162374T

# Fast CMOS 16-Bit Registers (3-State)

Features

- High-speed, low power device with high current drive.
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Supports Hot Insertion
- Balanced output drivers: ±24 mA
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) < 0.6V
  at $V_{CC} = 5V$, $T_A = 25°C$
- Packages available:
  - 48-pin 240 mil wide plastic TSSOP (A)
  - 48-pin 300 mil wide plastic SSOP (V)

Description

Pericom Semiconductor's PI74FCT162374T is a 16-bit octal registers designed with 16 D-type flip-flops with a buffered common clock and 3-state outputs. The Output Enable (x$\overline{OE}$) and clock (xCLK) controls are organized to operate as two 8-bit registers or one 16-bit register. When $\overline{OE}$ is HIGH, the outputs are in the high impedance state. Input data meeting the setup and hold time requirements of the D inputs is transferred to the O outputs on the LOW-to-HIGH transition of the clock input.

The PI74FCT162374T has ±24 mA balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

Block Diagram
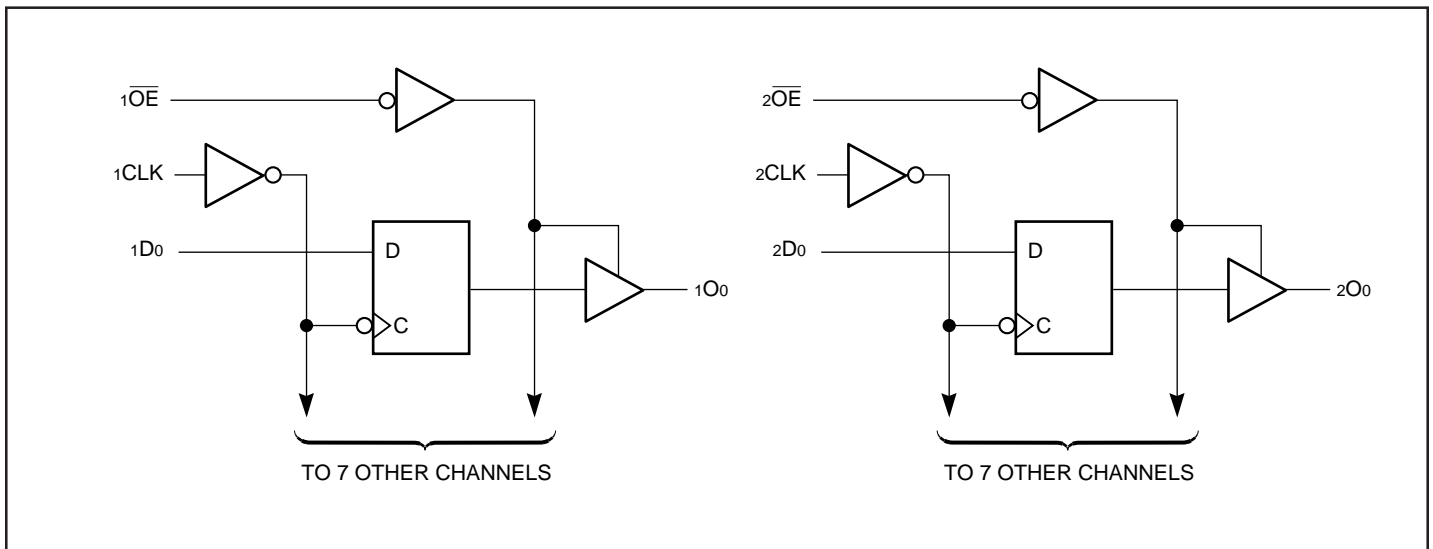
Pin Description

Pin Name	Description
x$\overline{OE}$	3-State Output Enable Inputs (Active LOW)
xCLK	Clock Inputs
xDx	Inputs[1]
xOx	3-State Outputs
GND	Ground
V_{CC}	Power

Note: 1. For the PI74FCT162H374T, these pins have "Bus Hold." All other pins are standard, outputs, or I/Os.

Pin Configuration

```
        ┌──────────────────┐
 1OE  ──┤ 1 ○         48   ├── 1CLK
 1O0  ──┤ 2           47   ├── 1D0
 1O1  ──┤ 3           46   ├── 1D1
 GND  ──┤ 4           45   ├── GND
 1O2  ──┤ 5           44   ├── 1D2
 1O3  ──┤ 6           43   ├── 1D3
 VCC  ──┤ 7           42   ├── VCC
 1O4  ──┤ 8           41   ├── 1D4
 1O5  ──┤ 9           40   ├── 1D5
 GND  ──┤ 10          39   ├── GND
 1O6  ──┤ 11          38   ├── 1D6
 1O7  ──┤ 12          37   ├── 1D7
 2O0  ──┤ 13          36   ├── 2D0
 2O1  ──┤ 14          35   ├── 2D1
 GND  ──┤ 15          34   ├── GND
 2O2  ──┤ 16          33   ├── 2D2
 2O3  ──┤ 17          32   ├── 2D3
 VCC  ──┤ 18          31   ├── VCC
 2O4  ──┤ 19          30   ├── 2D4
 2O5  ──┤ 20          29   ├── 2D5
 GND  ──┤ 21          28   ├── GND
 2O6  ──┤ 22          27   ├── 2D6
 2O7  ──┤ 23          26   ├── 2D7
 2OE  ──┤ 24          25   ├── 2CLK
        └──────────────────┘
```

Truth Table[1]

Function	Inputs			Outputs
	xDx	**xCLK**	**x$\overline{OE}$**	**xOx**
High-Z	X	L	H	Z
	X	H	H	Z
Load Register	L	↑	L	L
	H	↑	L	H
	L	↑	H	Z
	H	↑	H	Z

Note:
1. H = High Voltage Level
    L = Low Voltage Level
    X = Don't Care
    Z = High Impedance
    ↑ = LOW-to-HIGH transition
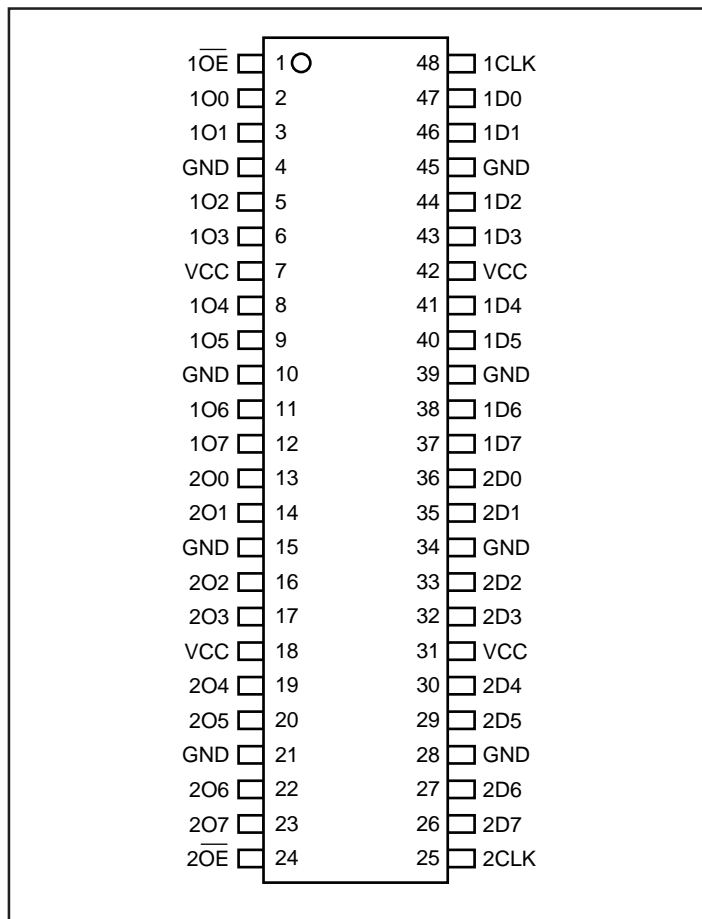
Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .... –65°C to +150°C

Ambient Temperature with Power Applied .... –40°C to +85°C

Supply Voltage to Ground Potential (Inputs & Vcc Only) .... –0.5V to +7.0V

Supply Voltage to Ground Potential (Outputs & D/O Only) .... –0.5V to +7.0V

DC Input Voltage .... –0.5V to +7.0V

DC Output Current .... 120 mA

Power Dissipation 1.0W

Note:
Stresses greater than those listed under MAXI-MUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V_{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I_{IH}	Input HIGH Current	Standard Input, V_{CC} = Max.	$V_{IN} = V_{CC}$			1	μA
I_{IH}	Input HIGH Current	Standard I/O, V_{CC} = Max.	$V_{IN} = V_{CC}$			1	μA
I_{IH}	Input HIGH Current	Bus Hold Input[4], V_{CC} = Max.	$V_{IN} = V_{CC}$			±100	μA
I_{IH}	Input HIGH Current	Bus Hold I/O[4], V_{CC} = Max.	$V_{IN} = V_{CC}$			±100	μA
I_{IL}	Input LOW Current	Standard Input, V_{CC} = Min.	$V_{IN} = GND$			–1	μA
I_{IL}	Input LOW Current	Standard I/O, V_{CC} = Min.	$V_{IN} = GND$			–1	μA
I_{IL}	Input LOW Current	Bus Hold Input[4], V_{CC} = Min.	$V_{IN} = GND$			±100	μA
I_{IL}	Input LOW Current	Bus Hold I/O[4], V_{CC} = Min.	$V_{IN} = GND$			±100	μA
I_{BHH}	Bus Hold	Bus Hold Input[4], V_{CC} = Min.	$V_{IN} = 2.0V$	–50			μA
I_{BHL}	Sustain Current		$V_{IN} = 0.8V$	+50			
I_{OZH}[5]	High Impedance	V_{CC} = Max.	$V_{OUT} = 2.7V$			1	μA
I_{OZL}[5]	Output Current	V_{CC} = Max.	$V_{OUT} = 0.5V$			–1	μA
V_{IK}	Clamp Diode Voltage	V_{CC} = Min., I_{IN} = –18 mA			–0.7	–1.2	V
I_{OS}	Short Circuit Current	V_{CC} = Max.[3], V_{OUT} = GND		–80	–140	–200	mA
I_O	Output Drive Current	V_{CC} = Max.[3], V_{OUT} = 2.5V		–50		–180	mA
V_H	Input Hysteresis				100		mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. This specification does not apply to bi-directional functionalities with Bus Hold.

Power Supply Characteristics

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
I_{CC}	Quiescent Power Supply Current	V_{CC} = Max.	V_{IN} = GND or V_{CC}		0.1	500	μA
ΔI_{CC}	Supply Current per Input @ TTL HIGH	V_{CC} = Max.	V_{IN} = 3.4V[3]		0.5	1.5	mA
I_{CCD}	Supply Current per Input per MHz[4]	V_{CC} = Max., Outputs Open $x\overline{OE}$ = GND One Bit Toggling 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND		60	100	μA/ MHz
I_C	Total Power Supply Current[6]	V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $x\overline{OE}$ = GND f_I = 5 MHz 50% Duty Cycle One Bit Toggling	$V_{IN} = V_{CC}$ V_{IN} = GND		0.6	1.5[5]	mA
			V_{IN} = 3.4V V_{IN} = GND		1.1	3.0[5]	
		V_{CC} = Max., Outputs Open f_{CP} = 10 MHz 50% Duty Cycle $x\overline{OE}$ = GND 16 Bits Toggling f_I = 2.5 MHz 50% Duty Cycle	$V_{IN} = V_{CC}$ V_{IN} = GND		3.0	5.5[5]	
			V_{IN} = 3.4V V_{IN} = GND		7.5	19.0[5]	

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device.
2. Typical values are at Vcc = 5.0V, +25°C ambient.
3. Per TTL driven input (V_{IN} = 3.4V); all other inputs at Vcc or GND.
4. This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
5. Values for these conditions are examples of the Icc formula. These limits are guaranteed but not tested.
6. I_C = $I_{QUIESCENT}$ + I_{INPUTS} + $I_{DYNAMIC}$
   I_C = I_{CC} + ΔI_{CC} $D_H N_T$ + I_{CCD} (f_{CP}/2 + $f_I N_I$)
   I_{CC} = Quiescent Current
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_I = Input Frequency
   N_I = Number of Inputs at f_I
   All currents are in milliamps and all frequencies are in megahertz.

Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions[1]		Min.	Typ[2]	Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OH} = −24.0 mA	2.4	3.3		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., V_{IN} = V_{IH} or V_{IL}	I_{OL} = 24 mA		0.3	0.55	V
I_{ODL}	Output LOW Current	V_{CC} = 5V, V_{IN} = V_{IH} OR V_{IL}, V_{OUT} = 1.5V[3]		60	115	150	mA
I_{ODH}	Output HIGH Current	V_{CC} = 5V, V_{IN} = V_{IH} OR V_{IL}, V_{OUT} = 1.5V[3]		−60	−115	−150	mA

Capacitance (T_A = 25°C, f = 1 MHz)

Parameters[4]	Description	Test Conditions	Typ	Max.	Units
C_{IN}	Input Capacitance	V_{IN} = 0V	4.5	6	pF
C_{OUT}	Output Capacitance	V_{OUT} = 0V	5.5	8	pF

Notes:
1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at Vcc = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Switching Characteristics over Operating Range

|			162374T		162374AT		162374CT		
			Com.		Com.		Com.		
Parameters	Description	Conditions[1]	Min	Max	Min	Max	Min	Max	Unit
t_{PLH} t_{PHL}	Propagation Delay xCLKx to xOx	C_L = 50 pF R_L = 500Ω	2.0	10.0	2.0	6.5	2.0	5.2	ns
t_{PZH} t_{PZL}	Output Enable Time xOE to xOx		1.5	12.5	1.5	6.5	1.5	5.5	ns
t_{PHZ} t_{PLZ}	Output Disable Time[3] xOE to xOx		1.5	8.0	1.5	5.5	1.5	5.0	ns
t_{SU}	Setup Time HIGH or LOW, xDx to xCLK		2.0	—	2.0	—	2.0	—	ns
t_H	Hold Time HIGH or LOW, xDx to xCLK		1.5	—	1.5	—	1.5	—	ns
t_W	xCLK Pulse Width HIGH or LOW[3]		7.0	—	5.0	—	5.0	—	ns
$t_{SK(o)}$	Output Skew[4]		—	0.5	—	0.5	—	0.5	ns

Notes:
1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162374T
16-Bit Register (3-State)

Packaging Mechanical: 48-pin 240-mil wide plastic TSSOP (A)
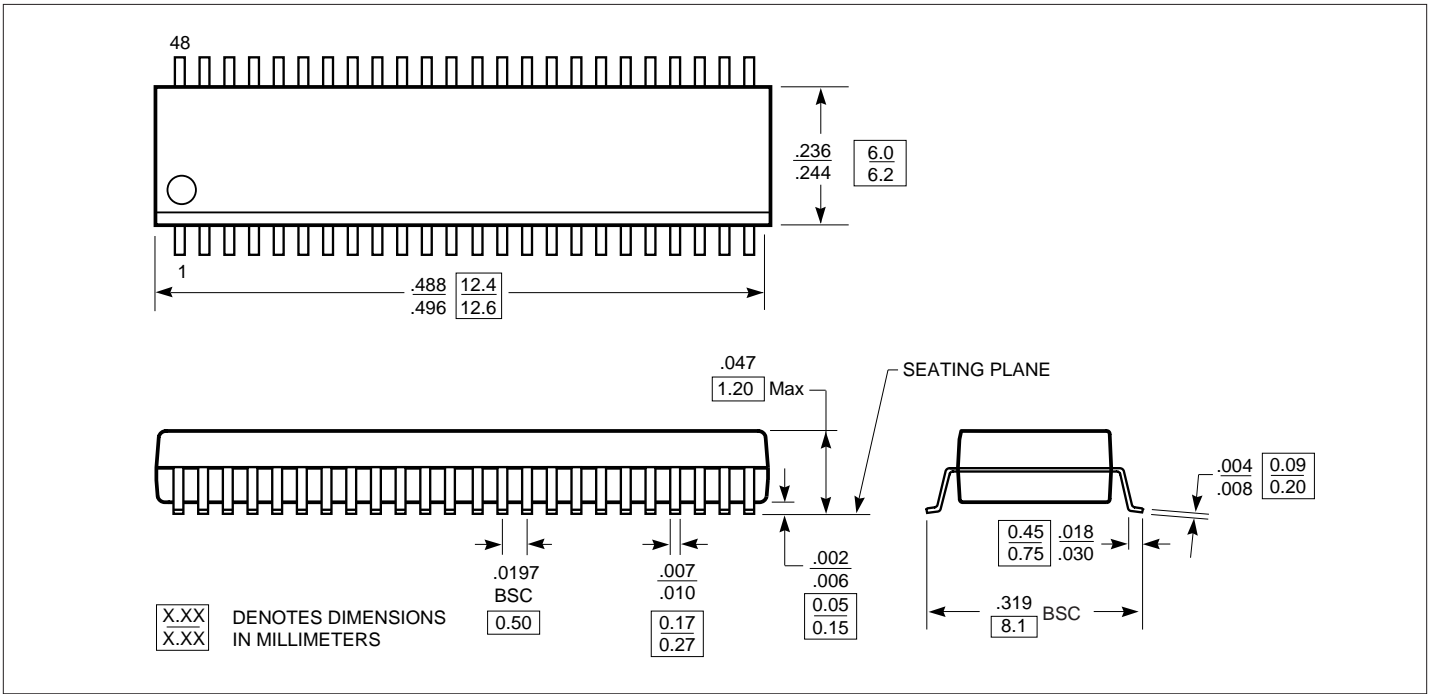
Packaging Mechanical: 48-pin 300-mil wide plastic SSOP (V)

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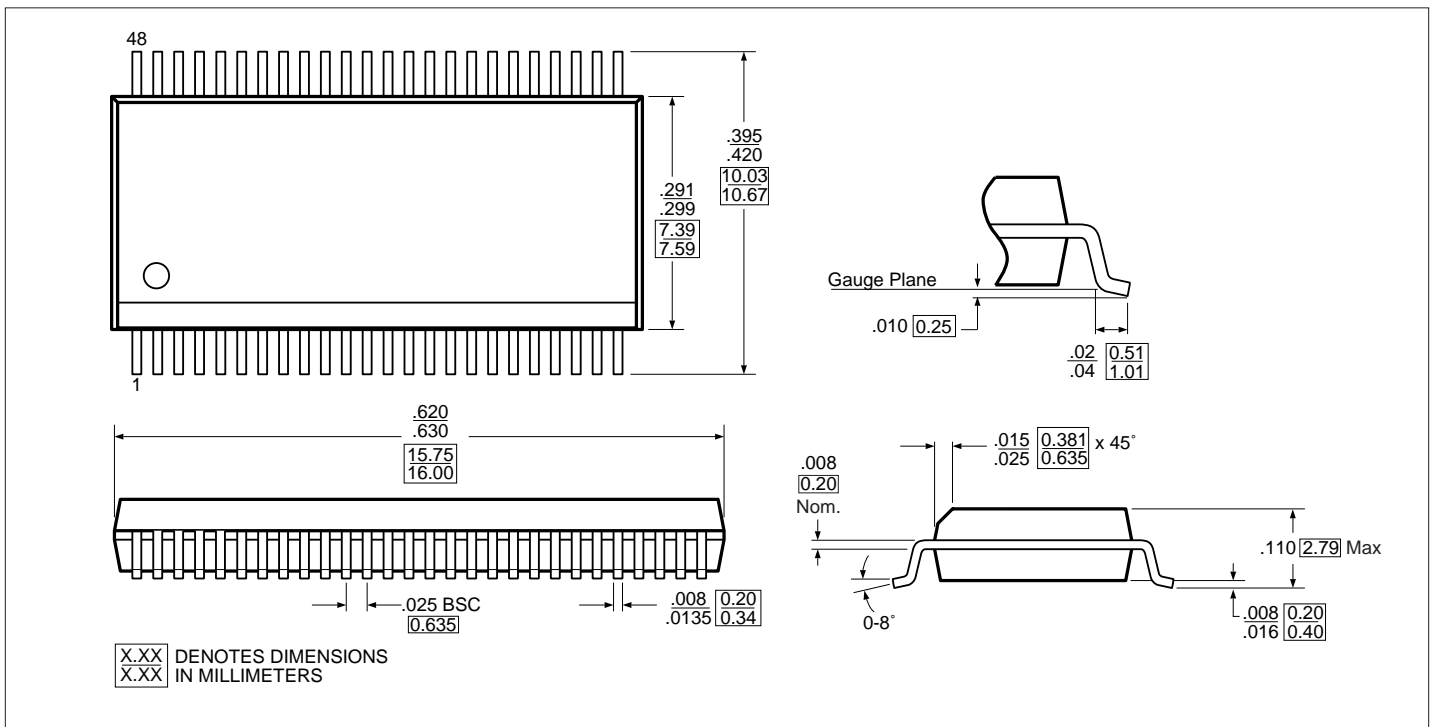
Ordering Information

Ordering Code	Package Code	Speed Grade	Package Type
PI74FCT162373TA	A	Blank	48-pin TSSOP
PI74FCT162373TV	V	Blank	48-pin SSOP
PI74FCT162373ATA	A	A	48-pin TSSOP
PI74FCT162373ATV	V	A	48-pin SSOP
PI74FCT162373CTA	A	C	48-pin TSSOP
PI74FCT162373CTV	V	C	48-pin SSOP

Notes:

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

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