National Semiconductor

DM54192/DM74192, DM54193/DM74193 Synchronous Up/Down Counters with Dual Clock

General Description

These circuits are synchronous up/down counters; the 192 circuit is a BCD counter and the 193 is a 4-bit binary counter. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change together when so instructed by the steering logic. This mode of operation eliminates the output counting spikes normally associated with asynchronous (ripple-clock) counters.

The outputs of the four master-slave flip-flops are triggered by a low-to-high level transition of either count (clock) input. The direction of counting is determined by which count input is pulsed, while the other count input is held high.

All four counters are fully programmable; that is, each output may be preset to either level by entering the desired data at the inputs while the load input is low. The output will change independently of the count pulses. This feature allows the counters to be used as modulo-N dividers by simply modifying the count length with the preset inputs.

A clear input has been provided which, when taken to a high level, forces all outputs to the low level; independent of the count and load inputs. The clear, count, and load inputs are buffered to lower the drive requirements of clock drivers, etc., required for long words.

These counters were designed to be cascaded without the need for external circuitry. Both borrow and carry outputs are available to cascade both the up and down counting functions. The borrow output produces a pulse equal in width to the count down input when the counter underflows. Similarly, the carry output produces a pulse equal in width to the count down input when an overflow condition exists. The counters can then be easily cascaded by feeding the borrow and carry outputs to the count down and count up inputs respectively of the succeeding counter.

Features

- Fully independent clear input
- Synchronous operation
- Cascading circuitry provided internally
- Individual preset each flip-flop
- Typical count frequency 25 MHz
- Typical power dissipation 325 mW

Absolute Maximum Ratings (Note 1)

Supply Voltage	7V
Input Voltage	5.5V
Storage Temperature Range	−65°C to 150°C

Note 1: The "Absolute Maximum Ratings" are those values beyond which the safety of the device can not be guaranteed. The device should not be operated at these limits. The parametric values defined in the "Electrical Characteristics" table are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

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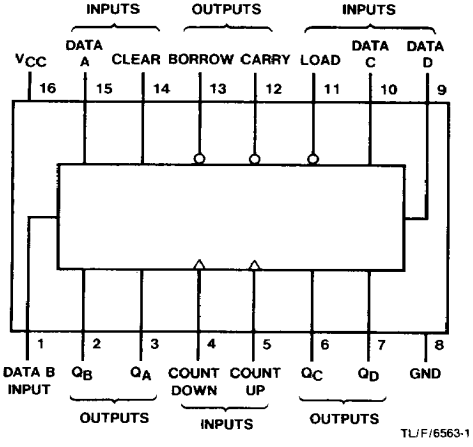
Connection Diagram

Dual-In-Line Package



54192 (J) **74192 (N)**
54193 (J) **74193 (N)**

Note: Low input to load sets Q_A = A, Q_B = B, Q_C = C, and Q_D = D.

Recommended Operating Conditions

Sym	Parameter		DM54192			DM74192			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	25	20	0	25	20	MHz
t_W	Pulse Width	Clock Low	30			30			ns
		Clock, Clear High Load Low	20			20			
t_{SU}	Data Setup Time		20			20			ns
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'192 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	89	mA
			DM74		65	102	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

'192 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Count Up to Carry		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Up to Carry		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Down to Borrow		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Down to Borrow		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count to Q		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count to Q		31	47	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Q		27	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Q		29	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		22	35	ns

Recommended Operating Conditions

Sym	Parameter		DM54193			DM74193			Units
			Min	Nom	Max	Min	Nom	Max	
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High Level Input Voltage		2			2			V
V_{IL}	Low Level Input Voltage				0.8			0.8	V
I_{OH}	High Level Output Current				−0.4			−0.4	mA
I_{OL}	Low Level Output Current				16			16	mA
f_{CLK}	Clock Frequency		0	25	20	0	25	20	MHz
t_W	Pulse Width	Clock Low	30			30			ns
		Clock, Clear High Load Low	20			20			
t_{SU}	Data Setup Time		20			20			ns
t_H	Hold Time		0			0			ns
T_A	Free Air Operating Temperature		−55		125	0		70	°C

'193 Electrical Characteristics

over recommended operating free air temperature (unless otherwise noted)

Sym	Parameter	Conditions		Min	Typ (Note 1)	Max	Units
V_I	Input Clamp Voltage	V_{CC} = Min, I_I = −12 mA				−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = Max V_{IL} = Max, V_{IH} = Min		2.4			V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = Max V_{IH} = Min, V_{IL} = Max				0.4	V
I_I	Input Current @ Max Input Voltage	V_{CC} = Max, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V				40	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.4V				−1.6	mA
I_{OS}	Short Circuit Output Current	V_{CC} = Max (Note 2)	DM54	−20		−55	mA
			DM74	−18		−55	
I_{CC}	Supply Current	V_{CC} = Max (Note 3)	DM54		65	89	mA
			DM74		65	102	

Note 1: All typicals are at V_{CC} = 5V, T_A = 25°C.

Note 2: Not more than one output should be shorted at a time.

Note 3: I_{CC} is measured with all outputs open, CLEAR and LOAD inputs grounded, and all other inputs at 4.5V.

'193 Switching Characteristics at $V_{CC} = 5V$ and $T_A = 25°C$

(See Section 1 for Test Waveforms and Output Load)

Parameter	From (Input) To (Output)	$R_L = 400\Omega$, $C_L = 15$ pF			Units
		Min	Typ	Max	
f_{MAX} Maximum Clock Frequency		20	25		MHz
t_{PLH} Propagation Delay Time Low to High Level Output	Count Up to Carry		17	26	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Up to Carry		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Count Down to Borrow		16	24	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Count Down to Borrow		16	24	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Either Count to Q		25	38	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Either Count to Q		31	47	ns
t_{PLH} Propagation Delay Time Low to High Level Output	Load to Q		27	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Load to Q		29	40	ns
t_{PHL} Propagation Delay Time High to Low Level Output	Clear to Q		22	35	ns

Logic Diagrams

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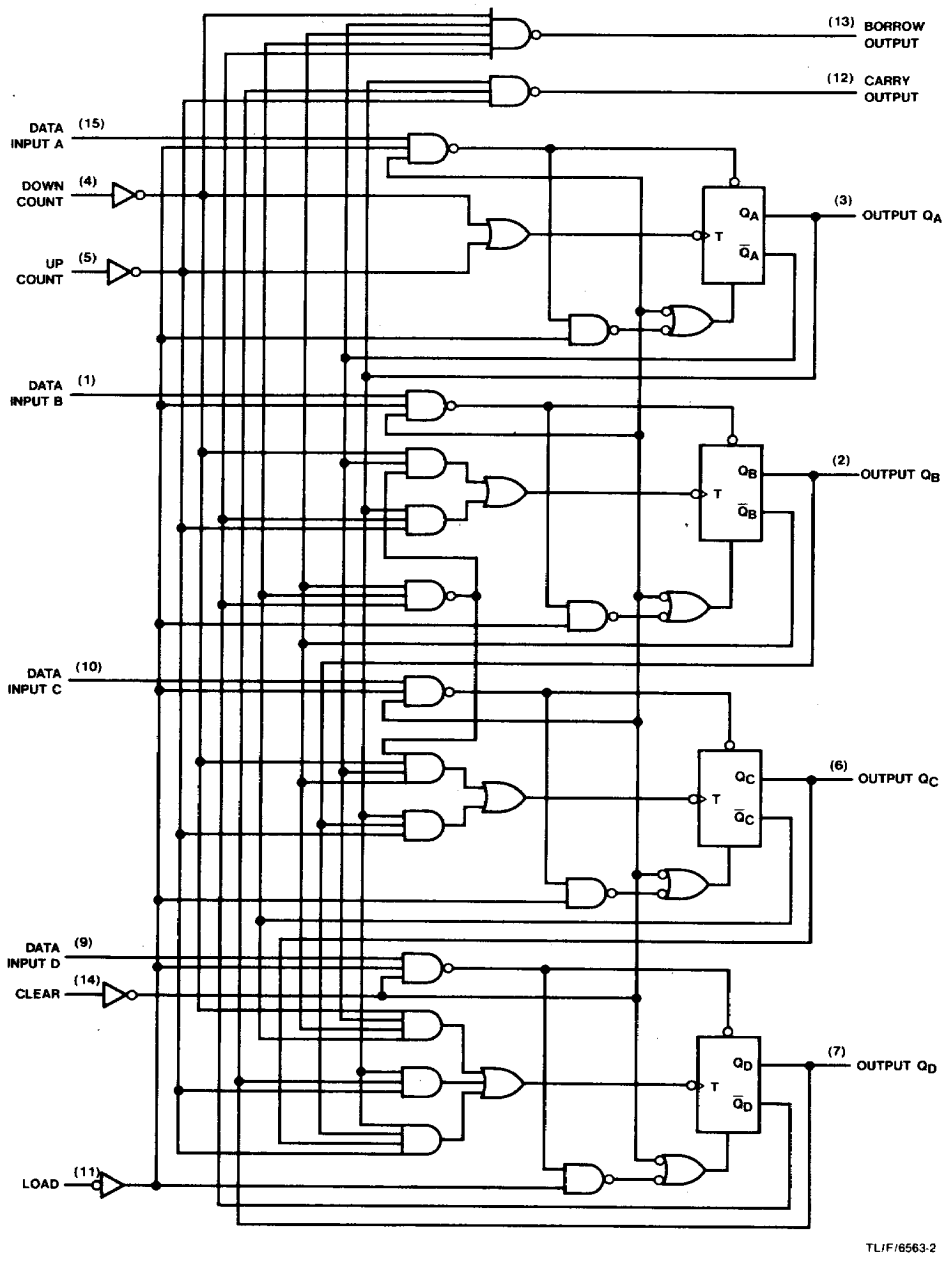
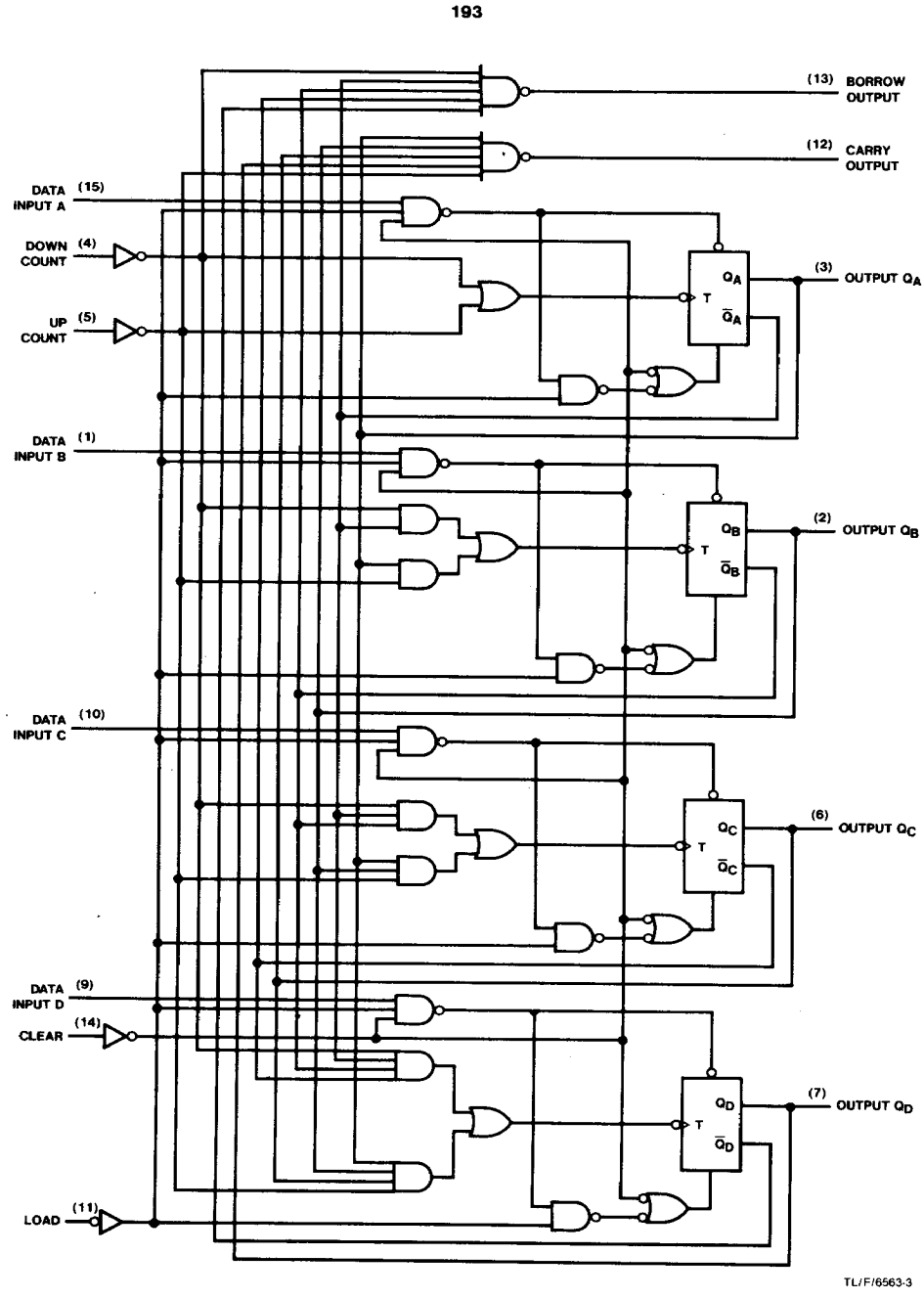
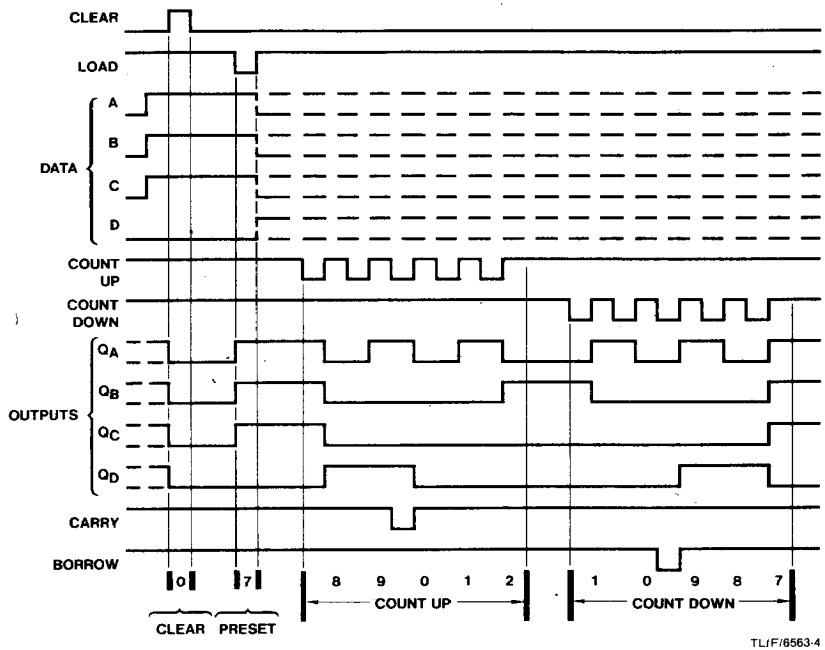


Logic Diagrams (Continued)



Timing Diagrams

192 DECADE COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



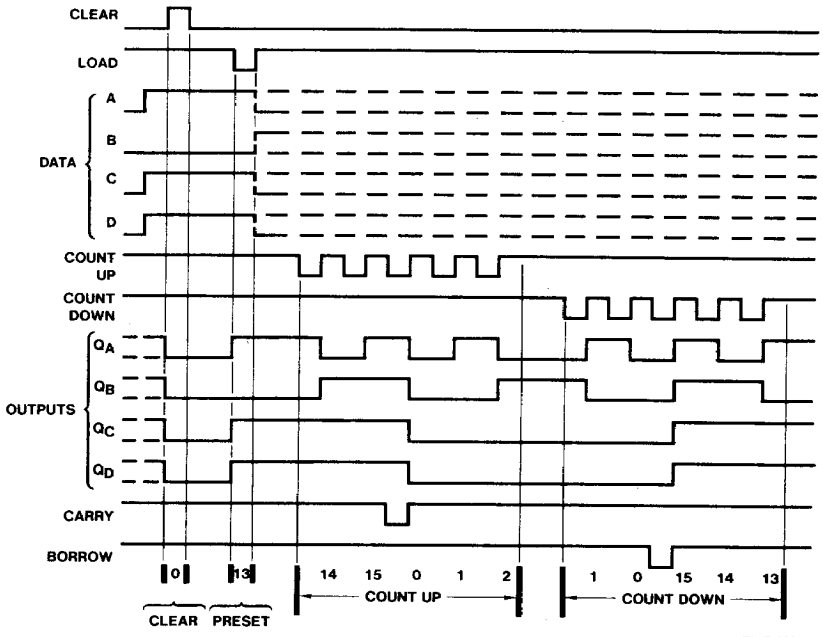
TL/F/6563-4

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to BCD seven.
(3) Count up to eight, nine, carry, zero, one, and two.
(4) Count down to one, zero, borrow, nine, eight, and seven.

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

Timing Diagrams (Continued)

193 BINARY COUNTERS
TYPICAL CLEAR, LOAD, AND COUNT SEQUENCES



TL/F/6563-5

Sequence:
(1) Clear outputs to zero.
(2) Load (preset) to binary thirteen.
(3) Count up to fourteen, fifteen, carry, zero, one, and two.
(4) Count down to one, zero, borrow, fifteen, fourteen, and thirteen.

Note A: Clear overrides load, data, and count inputs.
Note B: When counting up, count-down input must be high; when counting down, count-up input must be high.

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