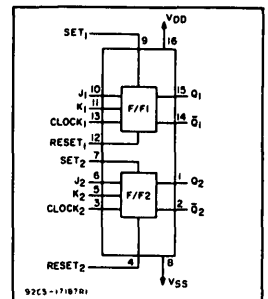
CD4027A Typ s

COS/MOS Dual J-K Master-Slave Flip-Flop

The RCA-CD4027A is a single monolithic chip integrated circuit containing two identical complementary-symmetry J-K master-slave flip-flops. Each flip-flop has provisions for individual J, K, Set, Reset, and Clock input signals. Buffered Q and $\overline{Q}$ signals are provided as outputs. This input-output arrangement provides for compatible operation with the RCA-CD4013A dual D-type flip-flop.

The CD4027A is useful in performing control, register, and toggle functions. Logic levels present at the J and K inputs along with internal self-steering control the state of each flip-flop; changes in the flip-flop state are synchronous with the positive-going transition of the clock pulse. Set and reset functions are independent of the clock and are initiated when a high level signal is present at either the Set or Reset input.



CD4027A
FUNCTIONAL DIAGRAM

MAXIMUM RATINGS, *Absolute-Maximum Values:*

STORAGE-TEMPERATURE RANGE (T_{stg}) . . . . . -65 to +150°C

OPERATING-TEMPERATURE RANGE (T_A):

PACKAGE TYPES D, F, H . . . . . -55 to +125°C

PACKAGE TYPE E . . . . . -40 to +85°C

DC SUPPLY-VOLTAGE RANGE, (V_{DD})

(Voltages referenced to V_{SS} Terminal): . . . . . -0.5 to +15 V

POWER DISSIPATION PER PACKAGE (P_D):

FOR T_A = -40 to +60°C (PACKAGE TYPE E) . . . . . 500 mW

FOR T_A = +60 to +85°C (PACKAGE TYPE E) . . . . . Derate Linearly at 12 mW/°C to 200 mW

FOR T_A = -55 to +100°C (PACKAGE TYPES D, F) . . . . . 500 mW

FOR T_A = +100 to +125°C (PACKAGE TYPES D, F) . . . . Derate Linearly at 12 mW/°C to 200 mW

DEVICE DISSIPATION PER OUTPUT TRANSISTOR

FOR T_A = FULL PACKAGE-TEMPERATURE RANGE (ALL PACKAGE TYPES) . . . . . 100 mW

INPUT VOLTAGE RANGE, ALL INPUTS . . . . . -0.5 to V_{DD} +0.5 V

LEAD TEMPERATURE (DURING SOLDERING):

At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

RECOMMENDED OPERATING CONDITIONS *at T_A = 25°C, Except as Noted.*
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

CHARACTERISTIC	V_{DD} (V)	LIMITS				UNITS
		D, F, H PACKAGES		E PACKAGE		
		MIN.	MAX.	MIN.	MAX.	
Supply-Voltage Range (For T_A = Full Package-Temperature Range)		3	12	3	12	V
Data Setup Time, t_S	5	150	—	200	—	ns
	10	50	—	75	—	
Clock Pulse Width, t_W	5	330	—	500	—	ns
	10	110	—	165	—	
Clock Input Frequency (Toggle Mode) f_{CL}	5	dc	1.5	dc	1	MHz
	10		4.5		3	
Clock Rise or Fall Time, t_rCL,* t_fCL	5	—	15	—	15	μs
	10	—	5	—	5	
Set or Reset Pulse Width, t_W	5	200	—	300	—	ns
	10	80	—	120	—	

*If more than one unit is cascaded in a parallel clocked operation, t_fCL should be made less than or equal to the sum of the fixed propagation delay time at 15 pF and the transition time of the output driving stage for the estimated capacitive load.

These types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic package (E suffix), 16-lead ceramic flat package (K suffix), and in chip form (H suffix).

Features:

- Set-Reset capability
- Static flip-flop operation—retains state indefinitely with clock level either "high" or "low"
- Medium-speed operation—10 MHz (typ.) clock toggle rate at 10V
- Quiescent current specified to 15 V
- Maximum input leakage of 1 μA at 15 V (full package-temperature range)
- 1-V noise margin (full package-temperature range)

Applications

- Registers, counters, control circuits

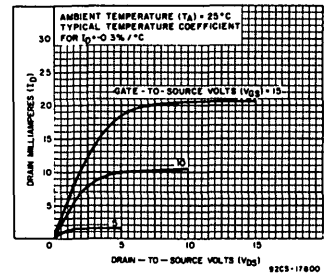
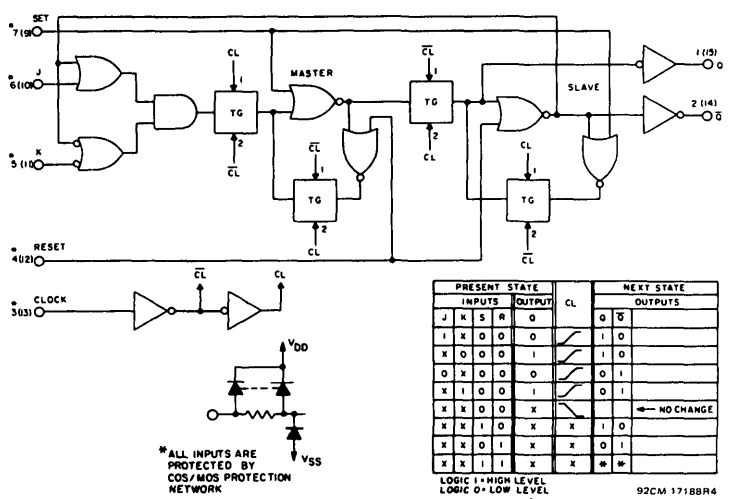


Fig. 1 — Typical n-channel drain characteristics.

STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTICS	CONDITIONS V_O (V)	CONDITIONS V_{IN} (V)	CONDITIONS V_{DD} (V)	LIMITS AT INDICATED TEMPERATURES (°C) D, F, H PACKAGES -55	+25 TYP.	+25 LIMIT	+125	E PACKAGE -40	+25 TYP.	+25 LIMIT	+85	UNITS
Quiescent Device Current, I_L Max.			5	1	0.005	1	60	10	0.01	10	140	
			10	2	0.005	2	120	20	0.05	20	280	μA
			15	25	0.5	25	1000	250	2.5	250	2500	
Output Voltage: Low Level, V_{OL}	–	0 5	5	0 Typ , C 05 Max								
	–	0.10	10	0 Typ., 0.05 Max								
High Level V_{OH}	–	0.5	5	5 Typ , 4.95 Min								V
	–	0 10	10	10 Typ., 9.95 Min								
Noise Immunity: Inputs Low, V_{NL}	4.2	–	5	2 25 Typ., 1 5 Min								
	9	–	10	4 5 Typ., 3 Min								
Inputs High V_{NH}	0.8	–	5	2.25 Typ.; 1.5 Min.								V
	1	–	10	4.5 Typ.; 3 Min.								
Noise Margin: Inputs Low, V_{NML}	4.5	–	5	1 Min								
	9	–	10	1 Min.								
Inputs High, V_{NMH}	0.5	–	5	1 Min								V
	1	–	10	1 Min.								
Output Drive Current. N Channel (Sink), I_DN Min.	0.5	–	5	0.65	1	0 5	0.35	0.35	1	0 3	0 24	
	0 5	–	10	1.25	2 5	1	0 75	0 72	2.5	0 6	0 5	mA
P-Channel (Source) I_DP Min.	4 5	–	5	–0 31	–0.5	–0.25	–0 175	–0.17	-0.5	–0 14	–0 12	
	9.5	–	10	–0.8	–1 3	–0.65	–0.45	–0.4	–1.3	–0.33	–0.27	
Input Leakage Current, I_{IL}, I_{IH}	Any Input		15	$\pm 10^{-5}$ Typ., ±1 Max								μA



PRESENT STATE INPUTS J	K	S	R	OUTPUT Q	CL	NEXT STATE OUTPUTS Q	$\overline{Q}$	
1	X	0	0	0		1	0	
X	0	0	0	1		1	0	
0	X	0	0	0		0	1	
X	1	0	0	1		0	1	
X	X	0	0	X	X			← NO CHANGE
X	X	1	0	X	X	1	0	
X	X	0	1	X	X	0	1	
X	X	1	1	X	X	*	*	

LOGIC 1 = HIGH LEVEL
LOGIC 0 = LOW LEVEL
X = DON'T CARE

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Fig. 2 — Logic diagram & truth table for CD4027A (one of two identical J-K flip flops).

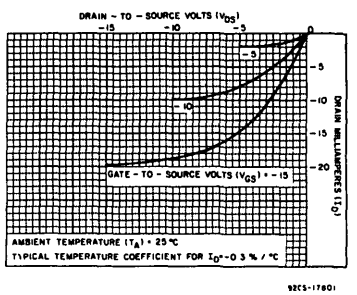

Fig. 3 — Typical p-channel drain characteristics.

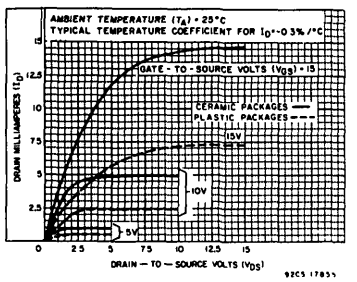

Fig. 4 — Minimum n-channel drain characteristics.

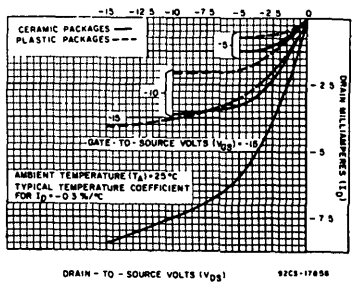

Fig. 5 — Minimum p-channel drain characteristics.

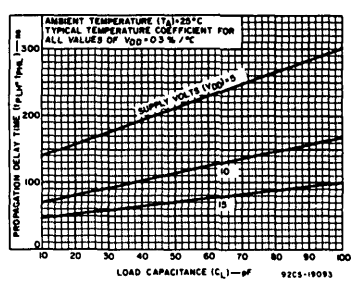

Fig. 6 — Typical propagation delay time vs. C_L.

DYNAMIC ELECTRICAL CHARACTERISTICS
at T_A = 25°C, Input t_r, t_f = 20 ns, C_L = 15 pF, R_L = 200 kΩ

CHARACTERISTIC	V_{DD} (V)	LIMITS						UNITS
		D, F, H PACKAGES			E PACKAGE			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Propagation Delay Time: Clock to Q or $\overline{Q}$ Outputs t_{PHL}, t_{PLH}	5	–	200	400	–	150	400	ns
	10	–	100	200	–	75	150	
Set to Q or Reset to $\overline{Q}$, t_{PLH}	5	–	175	225	–	175	350	ns
	10	–	75	110	–	75	150	
Set to $\overline{Q}$ or Reset to Q, t_{PHL}	5	–	175	225	–	175	350	ns
	10	–	75	110	–	75	150	
Transition Time t_{THL}, t_{TLH}	5	–	75	125	–	75	250	ns
	10	–	50	70	–	50	140	
Maximum Clock Input Frequency (Toggle Mode) f_{CL}	5	1.5	3	–	1	3	–	MHz
	10	4.5	8	–	3	8	–	
Minimum Clock Pulse Width, t_W	5	–	165	330	–	165	500	ns
	10	–	65	110	–	65	165	
Minimum Set or Reset Pulse Width, t_W	5	–	125	200	–	125	300	ns
	10	–	50	80	–	50	120	
Minimum Data Setup Time, t_S	5	–	70	150	–	70	200	ns
	10	–	25	50	–	25	75	
Clock Rise or Fall Time, t_{rCL}, t_{fCL}	5	–	–	15	–	–	15	us
	10	–	–	5	–	–	5	
Average Input Capacitance, C_I	Any Input	–	5	–	–	5	–	pF

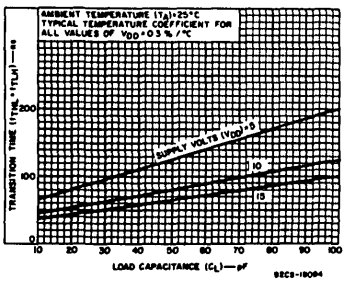

Fig.7 – Typical transition time vs. C_L.

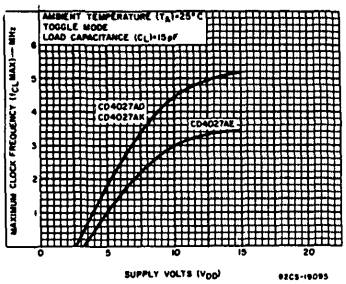

Fig.8 – Typical maximum clock input frequency vs. supply voltage.

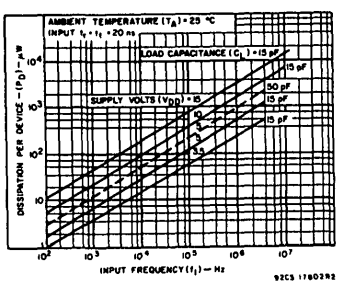

Fig.9 – Typical dissipation characteristics.

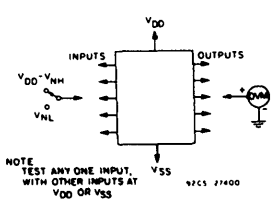

Fig. 10 – Noise immunity test circuit.

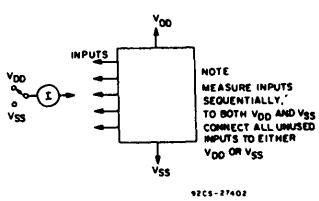

Fig. 11 – Input leakage current test circuit.

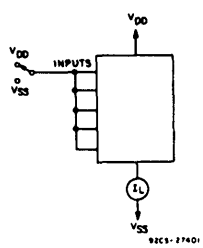

Fig. 12 – Quiescent device current test circuit.