

P-channel enhancement mode vertical D-MOS transistor

BSP250

FEATURES

- High speed switching
- No secondary breakdown
- Very low on-resistance.

APPLICATIONS

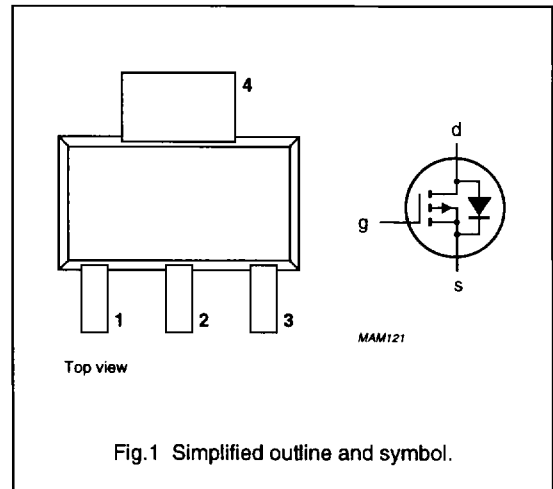
- Low-loss motor and actuator drivers, power switching, etc.

DESCRIPTION

P-channel enhancement mode vertical D-MOS transistor in a SOT223 plastic SMD package.

PINNING - SOT223

PIN	SYMBOL	DESCRIPTION
1	g	gate
2	d	drain
3	s	source
4	d	drain



CAUTION

The device is supplied in an antistatic package. The gate-source input must be protected against static discharge during transport or handling.

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		–	–30	V
V_{SD}	source-drain diode forward voltage	$I_S = -1.25$ A	–	–1.6	V
V_{GSO}	gate-source voltage (DC)	open drain	–	± 20	V
V_{GSth}	gate-source threshold voltage	$I_D = -1$ mA; $V_{DS} = V_{GS}$	–1	–2.8	V
I_D	drain current (DC)		–	–3	A
R_{DSon}	drain-source on-state resistance	$I_D = -1$ A; $V_{GS} = -10$ V	–	0.25	Ω
P_{tot}	total power dissipation	up to $T_{amb} = 25$ °C	–	1.65	W

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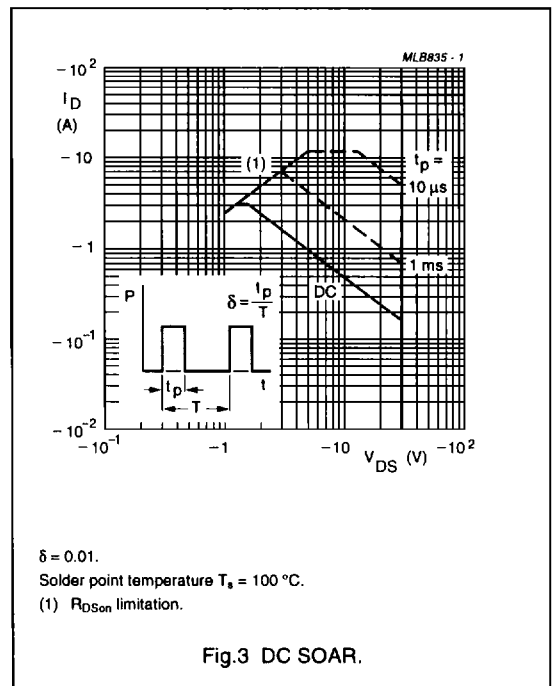
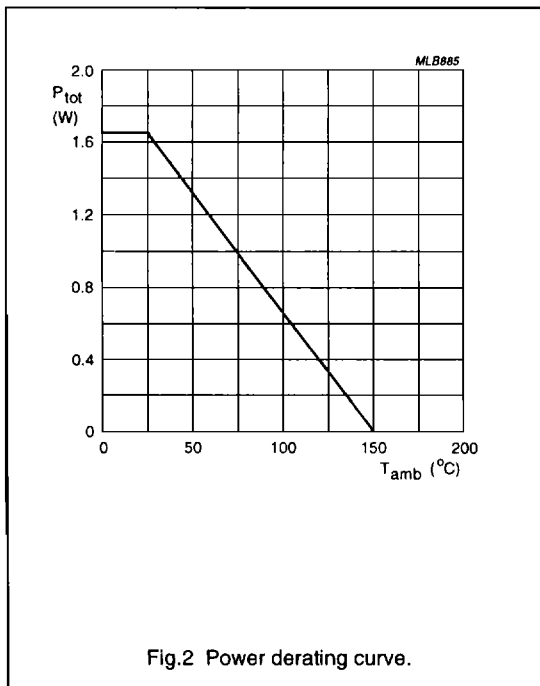
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage (DC)		-	-30	V
V_{GSO}	gate-source voltage (DC)	open drain	-	± 20	V
I_D	drain current (DC)	$T_s \leq 100^\circ\text{C}$	-	-3	A
I_{DM}	peak drain current	note 1	-	-12	A
P_{tot}	total power dissipation	up to $T_s = 100^\circ\text{C}$	-	5	W
		up to $T_{amb} = 25^\circ\text{C}$; note 2	-	1.65	W
T_{stg}	storage temperature		-65	+150	$^\circ\text{C}$
T_j	operating junction temperature		-	150	$^\circ\text{C}$
Source-drain diode					
I_S	source current (DC)	$T_s \leq 100^\circ\text{C}$	-	-1.5	A
I_{SM}	peak pulsed source current	note 1	-	-6	A

Notes

1. Pulse width and duty cycle limited by maximum junction temperature.
2. Device mounted on an epoxy printed-circuit board, $40 \times 40 \times 1.5$ mm; mounting pad for drain lead minimum 6 cm^2 .



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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	note 1	75	K/W
$R_{th\ j-s}$	thermal resistance from junction to soldering point		10	K/W

Note

- Device mounted on an epoxy printed-circuit board, $40 \times 40 \times 1.5$ mm; mounting pad for drain lead minimum 6 cm^2 .

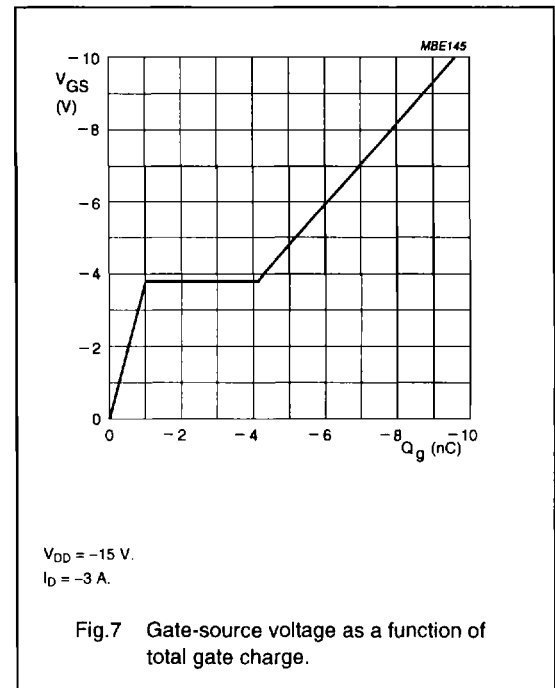
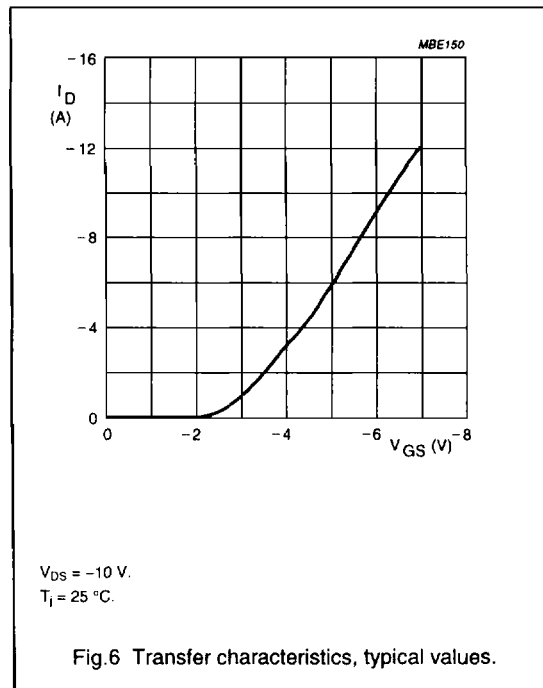
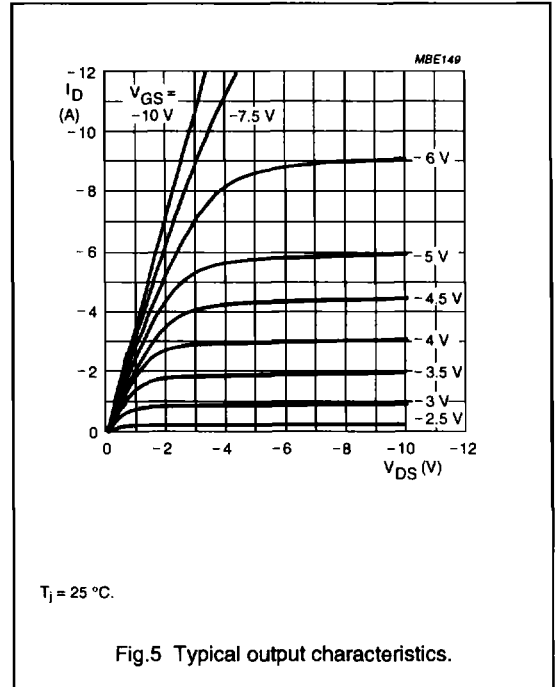
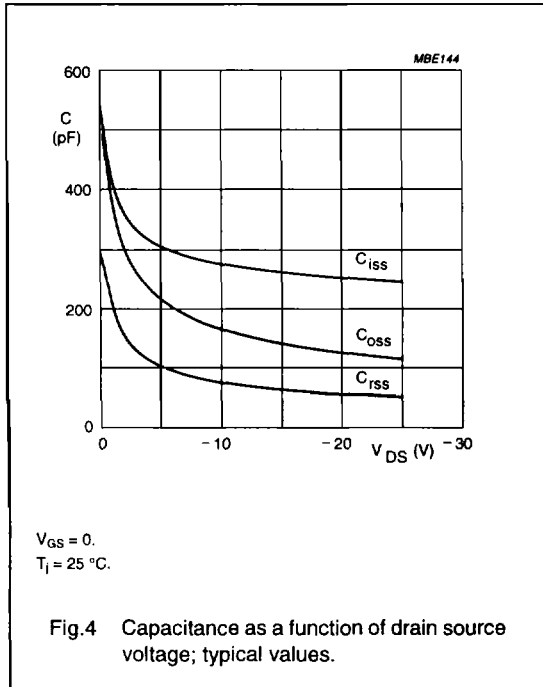
CHARACTERISTICS

$T_j = 25\text{ °C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0; I_D = -10\ \mu\text{A}$	-30	-	-	V
V_{GSth}	gate-source threshold voltage	$V_{GS} = V_{DS}; I_D = -1\ \text{mA}$	-1	-	-2.8	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0; V_{DS} = -24\ \text{V}$	-	-	-100	nA
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}; V_{DS} = 0$	-	-	± 100	nA
I_{Don}	on-state drain current	$V_{GS} = -10\ \text{V}; V_{DS} = -1\ \text{V}$	-3	-	-	A
		$V_{GS} = -4.5\ \text{V}; V_{DS} = -5\ \text{V}$	-1	-	-	A
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\ \text{V}; I_D = -0.5\ \text{A}$	-	0.33	0.4	Ω
		$V_{GS} = -10\ \text{V}; I_D = -1\ \text{A}$	-	0.22	0.25	Ω
$ y_{fs} $	forward transfer admittance	$V_{DS} = -20\ \text{V}; I_D = -1\ \text{A}$	1	2	-	S
C_{iss}	input capacitance	$V_{GS} = 0; V_{DS} = -20\ \text{V}; f = 1\ \text{MHz}$	-	250	-	pF
C_{oss}	output capacitance	$V_{GS} = 0; V_{DS} = -20\ \text{V}; f = 1\ \text{MHz}$	-	140	-	pF
C_{rfs}	reverse transfer capacitance	$V_{GS} = 0; V_{DS} = -20\ \text{V}; f = 1\ \text{MHz}$	-	50	-	pF
Q_g	total gate charge	$V_{GS} = -10\ \text{V}; V_{DS} = -15\ \text{V};$ $I_D = -2.3\ \text{A}$	-	10	25	nC
Q_{gs}	gate-source charge	$V_{GS} = -10\ \text{V}; V_{DS} = -15\ \text{V};$ $I_D = -2.3\ \text{A}$	-	1	-	nC
Q_{gd}	gate-drain charge	$V_{GS} = -10\ \text{V}; V_{DS} = -15\ \text{V};$ $I_D = -2.3\ \text{A}$	-	3	-	nC
t_{on}	turn-on time	$V_{GS} = 0\ \text{to}\ -10\ \text{V}; V_{DD} = -20\ \text{V};$ $I_D = -1\ \text{A}; R_L = 20\ \Omega$	-	20	80	ns
t_{off}	turn-off time	$V_{GS} = -10\ \text{to}\ 0\ \text{V}; V_{DD} = -20\ \text{V};$ $I_D = -1\ \text{A}; R_L = 20\ \Omega$	-	50	140	ns
Source-drain diode						
V_{SD}	source-drain diode forward voltage	$V_{GS} = 0; I_S = -1.25\ \text{A}$	-	-	-1.6	V
t_{rr}	reverse recovery time	$I_S = -1.25\ \text{A}; di/dt = 100\ \text{A}/\mu\text{s}$	-	150	200	ns

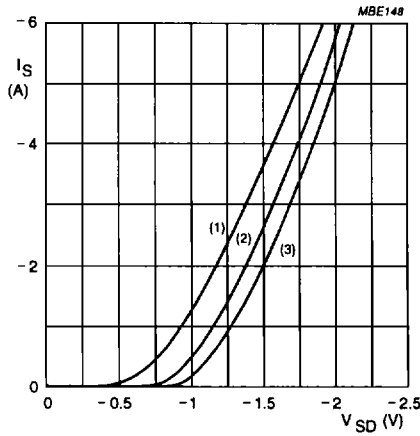
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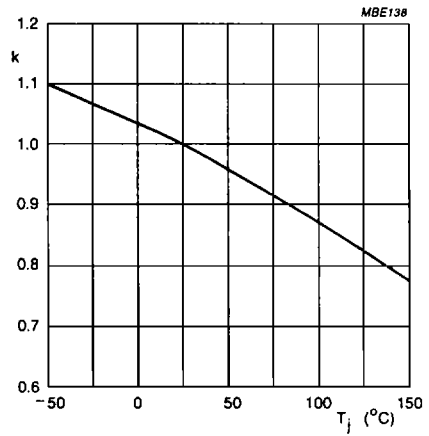
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$V_{GD} = 0$.

- (1) $T_j = 150^\circ\text{C}$.
- (2) $T_j = 25^\circ\text{C}$.
- (3) $T_j = -55^\circ\text{C}$.

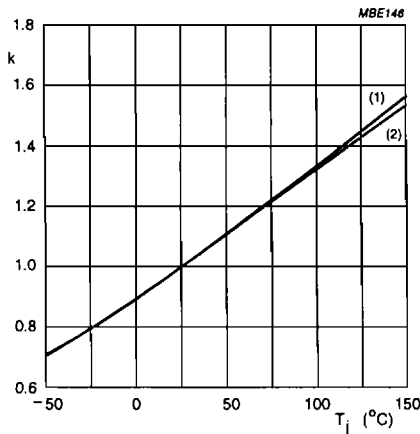
Fig.8 Source current as a function of source-drain diode forward voltage.



$$k = \frac{V_{GSth} \text{ at } T_j}{V_{GSth} \text{ at } 25^\circ\text{C}}$$

Typical V_{GSth} at $I_D = -1 \text{ mA}$; $V_{DS} = V_{GS} = V_{th}$.

Fig.9 Temperature coefficient of gate-source threshold voltage.



$$k = \frac{R_{DSon} \text{ at } T_j}{R_{DSon} \text{ at } 25^\circ\text{C}}$$

Typical R_{DSon} at:

- (1) $I_D = -1 \text{ A}$; $V_{GS} = -10 \text{ V}$.
- (2) $I_D = -0.5 \text{ A}$; $V_{GS} = -4.5 \text{ V}$.

Fig.10 Temperature coefficient of drain-source on-resistance.

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