Signetics

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Status	Product Specification
FAST Products	

FAST 74F646, 74F646A 74F648, 74F648A Transceivers/Registers

74F646/646A Octal Transceiver/Register, Non-Inverting (3-State)
74F648/648A Octal Transceivers/Register, Inverting (3-State)

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F646/648	115MHz	140mA
74F646A/648A	185MHz	105mA

FEATURES

- **Combines 'F245 and two 'F374 type functions in one chip**
- **High impedance base inputs for reduced loading (70µA in High and Low states)**
- **Independent registers for A and B buses**
- **Multiplexed real-time and stored data**
- **Choice of non-inverting and inverting data paths**
- **Controlled ramp outputs for 'F646A/'F648A**
- **3-state outputs**
- **300 mil wide 24-pin Slim Dip package**

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
24-Pin Plastic Slim DIP (300mil)	N74F646N, N74F646AN, N74F648N, N74F648AN
24-Pin Plastic SOL[1]	N74F646D, N74F646AD, N74F648D, N74F648AD

NOTE 1: Thermal mounting techniques are recommended except for N74F646A/N74F648A. See SMD Process Applications (page 17) for a discussion of thermal consideration for surface mounted devices.

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
A_0 - A_7, B_0 - B_7	A and B inputs	3.5/0.166	70µA/70µA
CPAB	A-to-B clock input	1.0/0.033	20µA/20µA
CPBA	B-to-A clock input	1.0/0.033	20µA/20µA
SAB	A-to-B select input	1.0/0.033	20µA/20µA
SBA	B-to-A select input	1.0/0.033	20µA/20µA
DIR	Data flow Directional control enable input	1.0/0.033	20µA/20µA
$\overline{OE}$	Output Enable input	1.0/0.033	20µA/20µA
A_0 - A_7, B_0 - B_7	Outputs for 'F646A/'F648A	750/80	15mA/48mA
A_0 - A_7, B_0 - B_7	Outputs 'F646/'F648	750/106.7	15mA/64mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

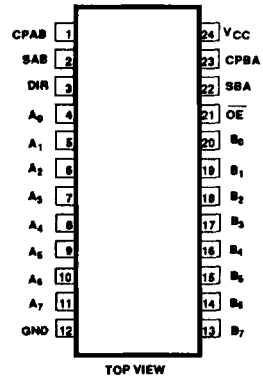
DESCRIPTION

The 74F646/646A and 74F648/648A Transceivers/Registers consist of bus transceiver circuits with 3-state outputs, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the input bus or from the internal registers. Data on the A or B bus will be clocked into the registers as the appropriate clock pin goes High. Output Enable ($\overline{OE}$) and DIR pins are provided to control the transceiver function. In the transceiver mode, data present at the high impedance port may be stored in either the A or B register or both.

The select (SAB, SBA) pins determine whether data is stored or transfered through the device in real-time. The DIR determines which bus will receive data when the $\overline{OE}$ is active Low. In the isolation mode ($\overline{OE}$ = High), data from Bus A may be stored in the B register and/or data from Bus B may be stored in the A register. When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two busses , A or B may be driven at a time. The following examples demonstrate the four fundamental bus-management functions that can be performed with the 'F646/646A and 'F648/648A.

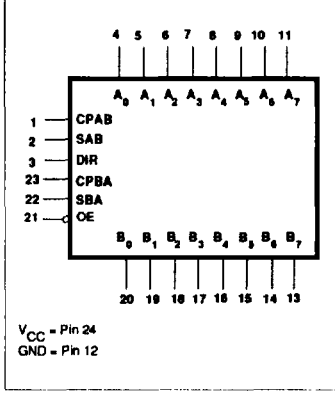
PIN CONFIGURATION

'F646/646A



LOGIC SYMBOL

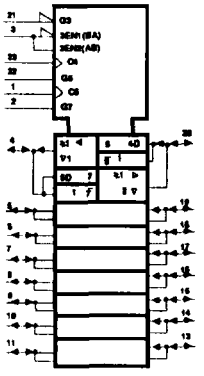
'F646/646A



V_{CC} = Pin 24
GND = Pin 12

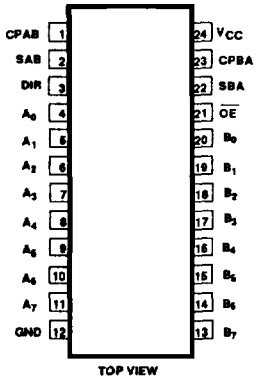
LOGIC SYMBOL(IEEE/IEC)

'F646/646A



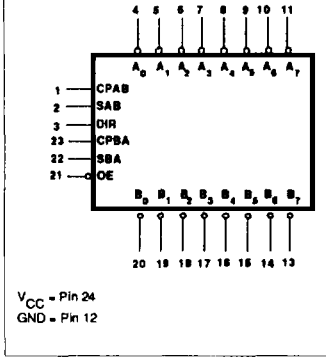
PIN CONFIGURATION

'F648/648A



LOGIC SYMBOL

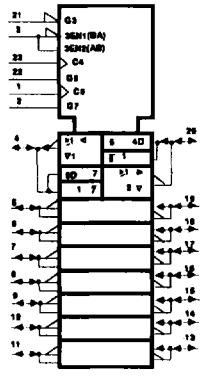
'F648/648A



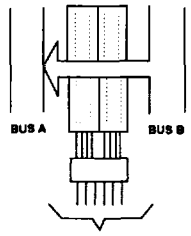
V_{CC} = Pin 24
GND = Pin 12

LOGIC SYMBOL(IEEE/IEC)

'F648/648A

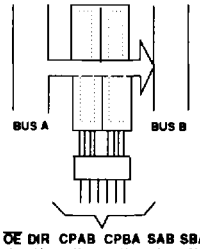


REAL TIME BUS TRANSFER BUS B TO BUS A



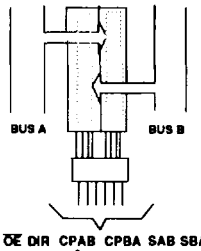
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	X	X	L

REAL TIME BUS TRANSFER BUS A TO BUS B



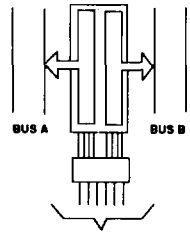
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	H	X	X	L	X

STORAGE FROM A, B, OR A AND B



$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
X	X	↑	X	X	X
X	X	X	↑	X	X
H	X	↑	↑	X	X

TRANSFER STORED DATA TO A OR B



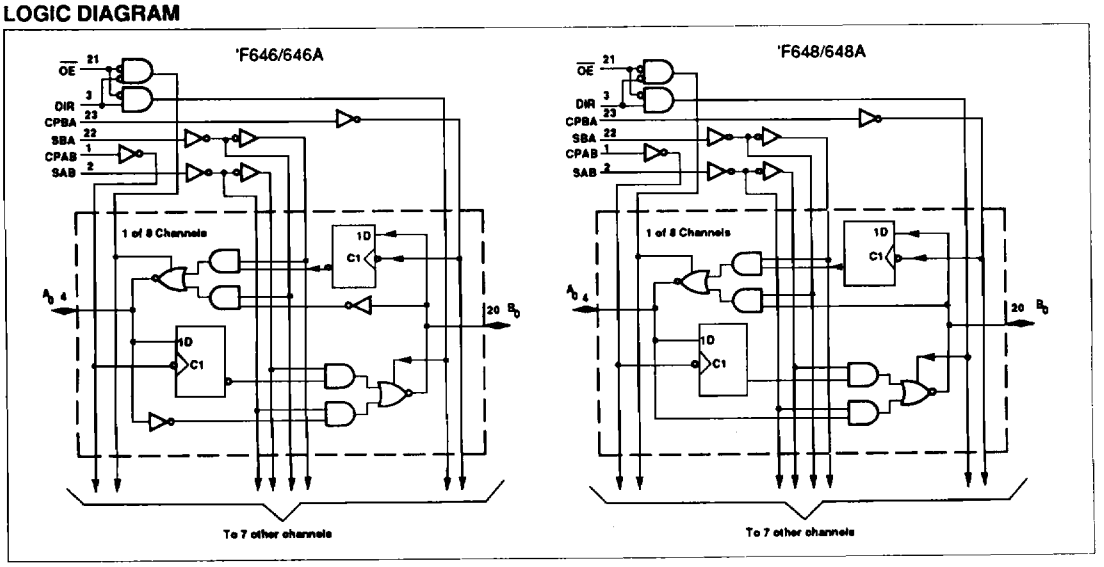
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA
L	L	X	H or L	X	H
L	H	H or L	X	H	X

FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE	
$\overline{OE}$	DIR	CPAB	CPBA	SAB	SBA	A_0-A_7	B_0-B_7	'F646/646A	'F648/648A
H	X	↑	X	X	X	Input	Unspecified*	Store A, B unspecified*	Store A, B unspecified*
H	X	X	↑	X	X	Unspecified*	Input	Store B, A unspecified*	Store B, A unspecified*
H H	X X	↑ H or L	↑ H or L	X X	X X	Input	Input	Store A and B data Isolation, hold storage	Store A and B data Isolation, hold storage
L L	L L	X X	X H or L	X X	L H	Output	Input	Real time B data to A bus Stored B data to A bus	Real time $\overline{B}$ data to A bus Stored $\overline{B}$ data to A bus
L L	H H	X H or L	X X	L H	X X	Input	Output	Real time A data to B bus Stored A data to B bus	Real time $\overline{A}$ data to B bus Stored $\overline{A}$ data to B bus

H= High voltage level
L= Low voltage level
X=Don't care
↑ =Low-to-High clock transition
*= The data output function may be enabled or disabled by various signals at the $\overline{OE}$ and DIR inputs. Data input functions are always enable, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER		RATING	UNIT
V_{CC}	Supply voltage		-0.5 to +7.0	V
V_{IN}	Input voltage		-0.5 to +7.0	V
I_{IN}	Input current		-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state		-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	74F646A, 74F648A	72	mA
		74F646, 74F648	128	mA
T_A	Operating free-air temperature range		0 to +70	°C
T_{STG}	Storage temperature		-65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER		LIMITS			UNIT
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5.0	5.5	V
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				-18	mA
I_{OH}	High-level output current				-15	mA
I_{OL}	Low-level output current	74F646A, 74F648A			48	mA
		74F646, 74F648			64	mA
T_A	Operating free-air temperature range		0		70	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]			LIMITS			UNIT
						Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OH}=-3mA	±10%V_{CC}	2.4			V
					±5%V_{CC}	2.7	3.4		V
				I_{OH}=-15mA	±10%V_{CC}	2.0			V
V_{OL}	Low-level output voltage	All	V_{CC} = MIN, V_{IL} = MAX, V_{IH} = MIN	I_{OL}= 48mA	±10%V_{CC}		0.38	0.55	V
		'F646 and 'F648 only		I_{OL}= 64mA	±5%V_{CC}		0.42	0.55	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}				-0.73	-1.2	V
I_I	Input current at maximum input voltage	others	V_{CC} = 0.0V, V_I = 7.0V					100	µA
		A_0-A_7, B_0-B_7	V_{CC} = MAX, V_I = 5.5V					1	mA
I_{IH}	High-level input current	$\overline{OE}$, DIR CPAB, CPBA SAB, SBA	V_{CC} = MAX, V_I = 2.7V					20	µA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.5V					-20	µA
I_{OZH} + I_{IH}	Off-state output current, High-level voltage applied	A_0-A_7, B_0-B_7	V_{CC} = MAX, V_O = 2.7V					70	µA
I_{OZL} + I_{IL}	Off-state output current, Low-level voltage applied		V_{CC} = MAX, V_O = 0.5V					-70	µA
I_{OS}	Short-circuit output current[3]	'F646, 'F648	V_{CC} = MAX			-100		-225	mA
I_O	Output current[4]	'F646A, 'F648A	V_{CC} = MAX, V_O = 2.25V			-60		-150	mA
I_{CC}	Supply current (total)	'F646 'F648	I_{CCH}	V_{CC} = MAX			125	165	mA
			I_{CCL}				160	210	mA
			I_{CCZ}				135	160	mA
		'F646A 'F648A	I_{CCH}				100	145	mA
			I_{CCL}				110	155	mA
			I_{CCZ}				105	155	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. The output condition has been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

AC ELECTRICAL CHARACTERISTICS for 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.5 5.5	7.5 8.0	10.0 10.0	5.0 5.0	11.5 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	4.0 4.0	6.0 6.5	9.0 8.0	4.0 4.0	10.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	5.0 5.0	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	5.0 6.5	7.0 8.5	10.0 11.0	4.5 6.0	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	6.5 8.5	9.0 11.0	4.0 5.5	10.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.5 6.5	9.0 9.0	11.5 11.5	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.5 5.5	8.5 8.5	11.0 11.0	4.5 5.0	13.0 12.5	ns

AC SETUP REQUIREMENTS for 74F646

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.5 4.5			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	4.0 6.0			4.0 6.0		ns

AC ELECTRICAL CHARACTERISTICS for 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.0	7.0 7.5	9.5 9.5	4.5 4.5	11.0 11.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 3	3.0 4.0	6.0 6.0	8.5 8.5	2.5 3.5	9.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	4.5 4.5	7.0 6.5	8.5 8.5	4.5 4.5	10.5 9.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.5 5.5	11.0 12.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	4.5 6.0	7.0 8.5	10.0 11.0	4.0 5.5	11.0 12.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	6.0 6.0	9.0 8.5	11.5 12.0	6.0 6.0	12.5 13.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	5.0 5.0	9.0 9.0	12.5 12.5	4.5 5.0	14.0 14.0	ns

AC SETUP REQUIREMENTS for 74F648

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			5.0 5.0		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 6.5			4.0 7.0		ns

AC ELECTRICAL CHARACTERISTICS for 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	165	185		150		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.5 4.5	7.0 7.0	10.0 9.5	4.5 4.0	11.0 10.0	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 2	4.0 2.0	6.0 5.0	9.0 8.0	3.5 2.0	10.0 8.0	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	4.5 3.5	6.5 8.0	9.5 10.0	4.0 3.0	10.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	3.0 3.0	5.5 5.5	9.0 9.0	2.5 2.5	10.0 10.0	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	3.0 3.5	5.0 6.0	8.0 8.5	3.0 3.0	8.5 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	1.5 2.5	4.0 5.5	6.5 8.0	1.0 2.0	8.0 9.5	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	2.0 3.0	4.5 5.0	7.5 8.0	1.5 2.0	8.5 8.5	ns

AC SETUP REQUIREMENTS for 74F646A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	3.5 4.0			4.0 4.5		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 3.5			4.5 4.0		ns

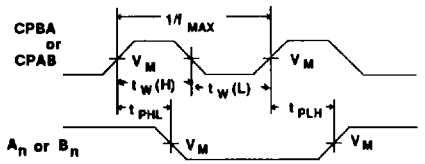
AC ELECTRICAL CHARACTERISTICS for 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	160	185		135		MHz
t_{PLH} t_{PHL}	Propagation delay CPAB or CPBA to A_n or B_n	Waveform 1	5.0 5.5	7.0 7.5	9.5 10.0	4.5 4.5	10.5 10.5	ns
t_{PLH} t_{PHL}	Propagation delay A_n to B_n or B_n to A_n	Waveform 3	2.5 4.0	4.5 6.0	7.5 8.5	2.0 4.0	8.5 9.5	ns
t_{PLH} t_{PHL}	Propagation delay SAB or SBA to A_n or B_n	Waveform 2, 3	4.0 4.5	7.0 7.0	9.5 9.5	3.5 4.5	11.5 10.0	ns
t_{PZH} t_{PZL}	Output Enable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	3.5 4.5	6.5 6.5	10.0 10.0	3.5 4.0	11.0 11.5	ns
t_{PZH} t_{PZL}	Output Enable time DIR to A_n or B_n	Waveform 5 Waveform 6	3.5 4.0	5.5 6.5	8.5 9.5	3.0 4.0	9.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time $\overline{OE}$ to A_n or B_n	Waveform 5 Waveform 6	2.5 4.0	4.0 6.5	6.5 9.0	2.0 3.5	8.0 10.0	ns
t_{PHZ} t_{PLZ}	Output Disable time DIR to A_n or B_n	Waveform 5 Waveform 6	2.5 2.5	5.0 5.0	8.5 8.0	2.0 2.5	9.0 9.0	ns

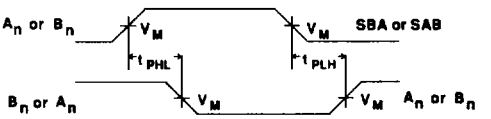
AC SETUP REQUIREMENTS for 74F648A

SYMBOL	PARAMETER	TEST CONDITION	LIMITS					UNIT
			T_A = +25°C V_{CC} = 5V C_L = 50pF R_L = 500Ω			T_A = 0°C to +70°C V_{CC} = 5V ±10% C_L = 50pF R_L = 500Ω		
			Min	Typ	Max	Min	Max	
t_s(H) t_s(L)	Setup time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	4.0 4.0			4.5 4.5		ns
t_h(H) t_h(L)	Hold time, High or Low A_n or B_n to CPAB or CPBA	Waveform 4	0 0			0 0		ns
t_w(H) t_w(L)	Pulse width, High or Low CPAB or CPBA	Waveform 1	3.5 3.5			4.0 3.5		ns

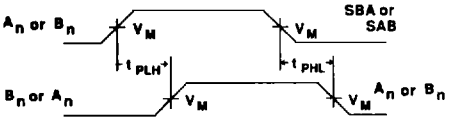
AC WAVEFORMS



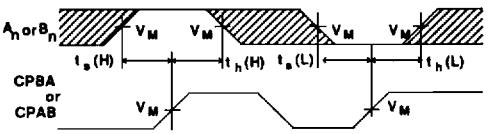
Waveform 1. Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



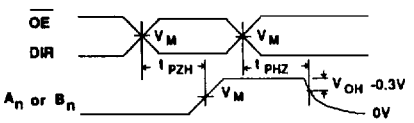
Waveform 2. Propagation Delay, An to Bn or Bn to An and SBA or SAB to An or Bn



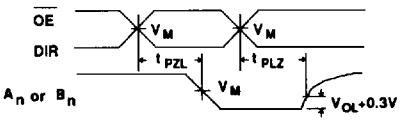
Waveform 3. Propagation Delay, An to Bn or Bn to An and SBA or SAB to An or Bn



Waveform 4. Data Setup And Hold Times



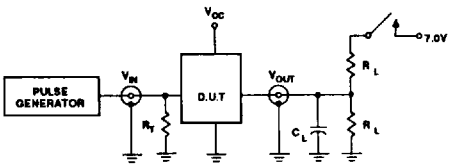
Waveform 5. 3-State Output Enable Time To High Level And Output Disable Time From High Level



Waveform 6. 3-State Output Enable Time To Low Level And Output Disable Time From Low Level

NOTE: For all waveforms, V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

TEST CIRCUIT AND WAVEFORMS



Test Circuit For 3-State Outputs

SWITCH POSITION

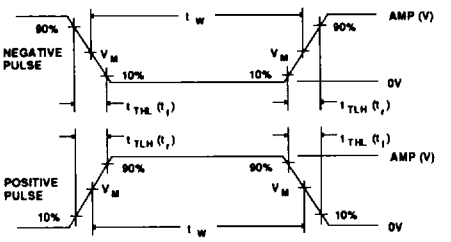
TEST	SWITCH
t_{PLZ}	closed
t_{PZL}	closed
All other	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.



V_M = 1.5V

Input Pulse Definition

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns