

F100163

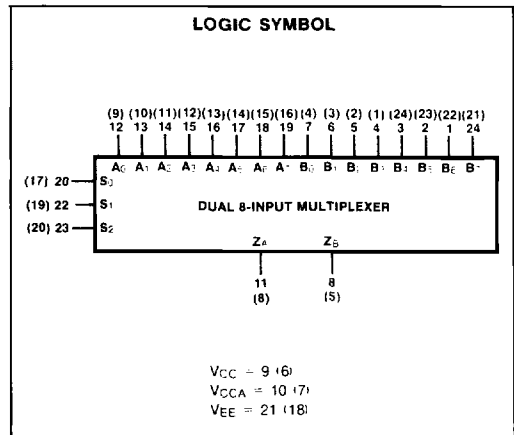
DUAL 8-INPUT MULTIPLEXER

F100K SERIES ECL

DESCRIPTION — The F100163 is a dual 8-Input Multiplexer. The Data Select (S_n) inputs determine which bit (A_n and B_n) will be presented at the Outputs (Z_A and Z_B respectively). The same bit (0-7) will be selected for both the Z_A and Z_B output.

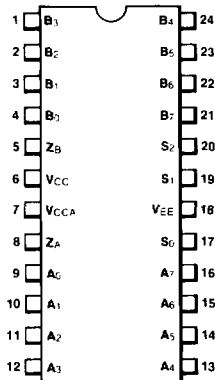
PIN NAMES

Z_n	Data Outputs
S_n	Data Selects
A_n, B_n	Data Inputs

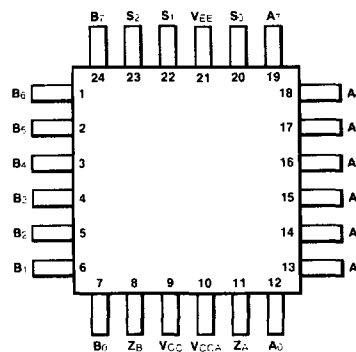


CONNECTION DIAGRAMS

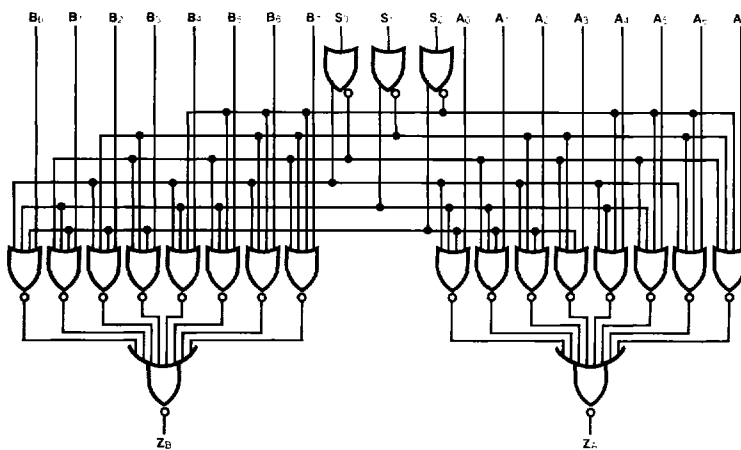
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



PARTIAL TRUTH TABLE

INPUTS											OUTPUT	
ADDRESS			DATA								Z _A	Z _B
S ₂	S ₁	S ₀	A ₇ B ₇	A ₆ B ₆	A ₅ B ₅	A ₄ B ₄	A ₃ B ₃	A ₂ B ₂	A ₁ B ₁	A ₀ B ₀		
L	L	L								L	L	
L	L	L								H	H	
L	L	H							L		L	
L	L	H						H			L	
L	H	L						L			L	
L	H	L						H			L	
L	H	H									L	
L	H	H									L	
H	L	L				L					L	
H	L	L				H					L	
H	L	H			L						L	
H	L	H			H						L	
H	H	L		L							L	
H	H	L		H							L	
H	H	H	L								L	
H	H	H	H								L	

H = High Level
 L = Low Level
 Blank = X = Irrelevant

DC CHARACTERISTICS: $V_{EE} = -4.5\text{ V}$, $V_{CC} = \text{GND}$, $T_A = 0^\circ\text{C} + 85^\circ\text{C}$

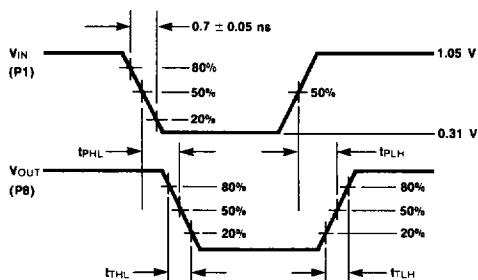
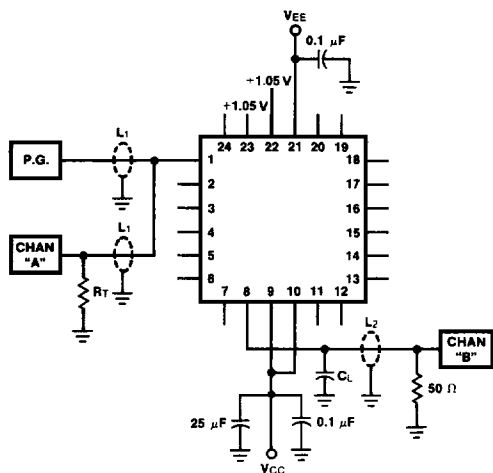
SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
I_{IH}	Input Current HIGH S_n A_n, B_n			265 340	μA	$V_{IN} = V_{IHA}$
C_i	Input Capacitance S_n A_n, B_n			4.0 6.0	pF	
I_{EE}	Supply Current	-153	-109	-76	mA	Inputs Open

AC CHARACTERISTICS: $T_A = 25^\circ\text{C}$, $V_{EE} = -4.5\text{V}$, $V_{CC} = \text{GND}$

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS
		B	TYP	A		
t_{PHL}	Propagation Delay, Data to Output	0.08	1.30	1.70	ns	Figure 1
t_{PLH}	Propagation Delay Select to Output	1.50	1.95	2.60	ns	
t_{TLH}	Transition Time 20% to 80%, 80% to 20%	0.70	1.20	1.70	ns	
t_{THL}						

NOTE: These limits apply to the flatpak. Add 200 ps to maximum limit propagation delays for the DIP package.

SWITCHING TEST CIRCUIT AND WAVEFORMS



L_1 and L_2 = equal length 50 Ω impedance lines
 R_T equal 50 Ω termination of scope
 Decoupling 0.1 μF from GND to V_{CC} and V_{EE}
 All outputs are loaded with 50 Ω to GND
 C_L = Jig and stray capacitance ≤ 3 pF

Fig 1