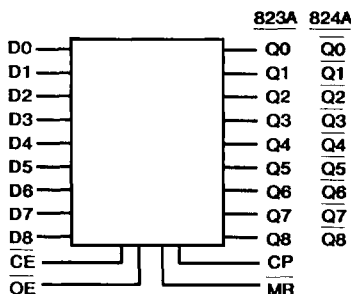


CD54/74FCT823A, CD54/74FCT823BT CD54/74FCT824A, CD54/74FCT824BT

July 1990



9-Bit D-Type Flip-Flops, 3-State Positive-Edge-Triggered

CD54/74FCT823A, CD54/74FCT823BT - Non-Inverting
CD54/74FCT824A, CD54/74FCT824BT - Inverting

Type Features:

- Buffered inputs
- Typical propagation delay:
7.5ns @ VCC = 5V, TA = 25°C, CL = 50pF (FCT823A, FCT824A)

FUNCTIONAL DIAGRAM

The CD54/74FCT823A, 823BT, 824A and 824BT 9-bit, D-type, 3-state, positive-edge-triggered flip-flops use a small-geometry BICMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0 to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The nine flip-flops enter data into their registers on the LOW-to-HIGH transition of the clock (CP). The Output Enable (\overline{OE}) controls the 3-state outputs and is independent of the register operation. These 9-bit-wide buffered registers with Clock Enable (\overline{CE}) and Master Reset (\overline{MR}) inputs are ideal for parity bus interfacing in high-performance microprogrammed systems.

The CD54/74FCT823A, 823BT, 824A and 824BT are supplied in 24-lead dual-in-line narrow-body plastic packages (EN suffix) and in 24-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT823A and 824A are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- SCR-latchup-resistant BICMOS process and circuit design
- FCTXXXA - Speed of bipolar FAST*/AS/S;
FCTXXXBT - 30% faster than FAST/AS/S with significantly reduced power consumption
- 48/32-mA output sink current (commercial/extended industrial)
- Output voltage swing limited to 3.7V @ VCC = 5V
- Controlled output-edge rates
- Input/output isolation to VCC
- BICMOS technology with low quiescent power

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

INPUTS					Q OUTPUTS		FUNCTION
\overline{OE}	\overline{MR}	\overline{CE}	D	CP	823A/BT	824A/BT	
H	X	L	L	\uparrow	Z	Z	High Z
H	X	L	H	\uparrow	Z	Z	
H	L	X	X	X	Z	Z	Reset
L	L	X	X	X	L	L	
H	H	H	X	X	Z	Z	Hold
L	H	H	X	X	NC	NC	
H	H	L	L	\uparrow	Z	Z	Load
H	H	L	H	\uparrow	Z	Z	
L	H	L	L	\uparrow	L	H	
L	H	L	H	\uparrow	H	L	

H = HIGH, L = LOW, X = Don't Care, NC = No Change,
 \uparrow = LOW-to-HIGH transition, Z = High Impedance

4
TECHNICAL DATA

MAXIMUM RATINGS, Absolute-Maximum Values:

DC SUPPLY-VOLTAGE (VCC)	-0.5V to 6V
DC INPUT DIODE CURRENT, I _{IK} (for V _I < -0.5V)	-20mA
DC OUTPUT DIODE CURRENT, I _{OK} (for V _O < -0.5V)	-50mA
DC OUTPUT SINK CURRENT per Output Pin, I _O	+70mA
DC OUTPUT SOURCE CURRENT per Output Pin, I _O	-30mA
DC VCC CURRENT (I _{CC})	234mA
DC GROUND CURRENT (I _{GND})	453mA
POWER DISSIPATION PER PACKAGE (PD):	
For TA = -55°C to +100°C (PACKAGE TYPE E)	500mW
For TA = +100°C to +125°C (PACKAGE TYPE E)	Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M)	400mW
For TA = +70°C to +125°C (PACKAGE TYPE M)	Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):	
PACKAGE TYPE E, M	-55°C to +125°C
STORAGE TEMPERATURE (T_{stg})	
-65°C to +150°C	
LEAD TEMPERATURE (DURING SOLDERING):	
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum	+265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only	+300°C

RECOMMENDED OPERATING CONDITIONS:

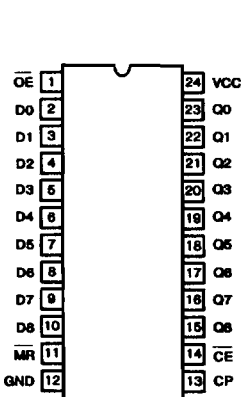
The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

CHARACTERISTIC	LIMITS		UNITS
	MIN	MAX	
Supply-Voltage Range, VCC*: CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, V _I	0	VCC	V
DC Output Voltage, V _O	0	≤ VCC	V
Operating Temperature, TA	-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv	0	10	ns/V

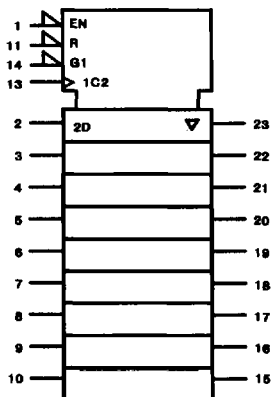
* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT823A, CD54/74FCT823BT TYPES

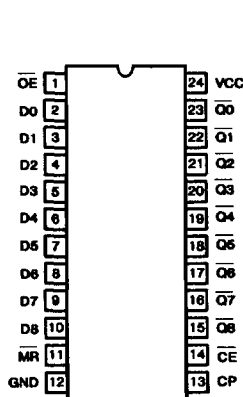
CD54/74FCT824A, CD54/74FCT824BT TYPES



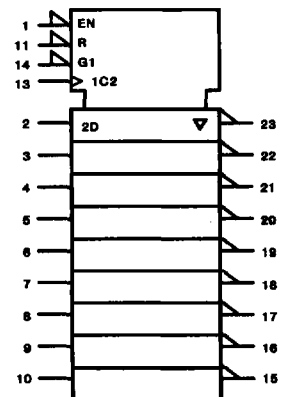
TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL



TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V

54FCT Extended Industrial Temperature Range, -55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS			AMBIENT TEMPERATURE (TA)						UNITS
		VI (V)	IO (mA)	VCC (V)	+25°C		0°C to +70°C		-55°C to +125°C		
					MIN	MAX	MIN	MAX	MIN	MAX	
High-Level Input Voltage	VIH			4.5 to 5.5	2	-	2	-	2	-	V
Low-Level Input Voltage	VIL			4.5 to 5.5	-	0.8	-	0.8	-	0.8	V
High-Level Output Voltage	VOH	VIH or	-24	MIN	2.4	-	2.4	-	-	-	V
		VIL	-20	MIN	2.4	-	-	-	2.4	-	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	-	0.55	-	0.55	-	-	V
		VIL	32	MIN	-	0.55	-	-	-	0.55	V
High-Level Input Current	I _{IH}	VCC		MAX	-	0.1	-	1	-	1	μA
Low-Level Input Current	I _{IL}	GND		MAX	-	-0.1	-	-1	-	-1	μA
3-State Leakage Current	IOZH	VCC		MAX	-	0.5	-	10	-	10	μA
	IOZL	GND		MAX	-	-0.5	-	-10	-	-10	μA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	-75	-	-75	-	-75	-	mA
Input Clamp Voltage	V _{IK}	VCC or GND	-18	MIN	-	-1.2	-	-1.2	-	-1.2	V
Quiescent Supply Current, MS ¹	ICC	VCC or GND	0	MAX	-	8	-	80	-	500	μA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V †		MAX	-	1.6	-	1.6	-	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.

† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	VCC (V)	CD54/74FCT823A, 824A				CD54/74FCT823BT, 824BT				UNITS		
			AMBIENT TEMPERATURE (T _A)										
			+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C			-55°C to +125°C	
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX		MIN	MAX
Pulse Width - Clock, \overline{MR}	t _W	5†		7	-	7	-					-	ns
Setup Time - Data to Clock, \overline{CE} to Clock	t _{SU}	5		4	-	4	-					-	ns
Hold Time - Data, \overline{CE}	t _H	5		2	-	2	-					-	ns
Master Reset Recovery Time	t _{REC}	5		7	-	7	-					-	ns
Maximum Clock Frequency	f _{MAX}	5		70	-	60	-					-	MHz

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

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SWITCHING CHARACTERISTICS

FCT Series: t_r, t_f = 2.5ns, CL = 50pF, RL - See Figure 4

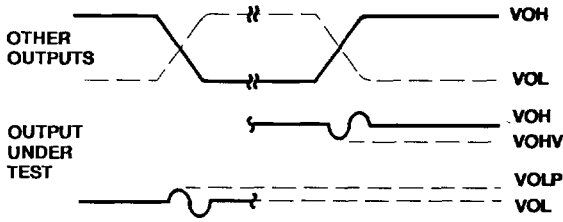
CHARACTERISTICS	SYMBOL	VCC (V)	CD54/74FCT823A, 824A				CD54/74FCT823BT, 824BT				UNITS		
			AMBIENT TEMPERATURE (T _A)										
			+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C			-55°C to +125°C	
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX		MIN	MAX
Propagation Delays:													
Clock to Q FCT823A/BT	t _{PLH} , t _{PHL}	5†	7.5	1.5	10	1.5	11.5						ns
Clock to \overline{Q} FCT824A/BT	t _{PLH} , t _{PHL}	5	7.5	1.5	10	1.5	11.5						ns
\overline{MR} to Q	t _{PHL}	5	10.5	1.5	14	1.5	15						ns
Output Enable FCT823A/BT to Q	t _{PZL} , t _{PZH}	5	9	1.5	12	1.5	13						ns
Output Disable FCT823A/BT to Q	t _{PLZ} , t _{PHZ}	5	6	1.5	8	1.5	9						ns
Output Enable FCT824A/BT to \overline{Q}	t _{PZL} , t _{PZH}	5	9	1.5	12	1.5	13						ns
Output Disable FCT824A/BT to \overline{Q}	t _{PLZ} , t _{PHZ}	5	6	1.5	8	1.5	9						ns
Power Dissipation Capacitance	CPD§	-											pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)	VOHV See Figure 1	5	0.5 Typical @ +25°C								V		
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)	VOLP See Figure 1	5	1 Typical @ +25°C								V		
Input Capacitance	CI	-	-	-	10	-	10	-	-	10	-	10	pF
3-State Output Capacitance	CO	-	-	-	15	-	15	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ. is @ 5V

§CPD, measured per flip-flop, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC² fi CPD + VO² to CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

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PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: $PRR \leq 1\text{MHz}$, $t_r = 2.5\text{ns}$, $t_f = 2.5\text{ns}$, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with $0.1\mu\text{F}$ capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

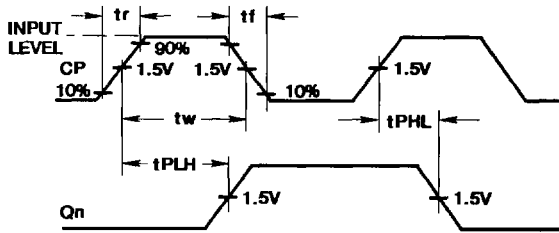


Figure 2 - Propagation delay times.

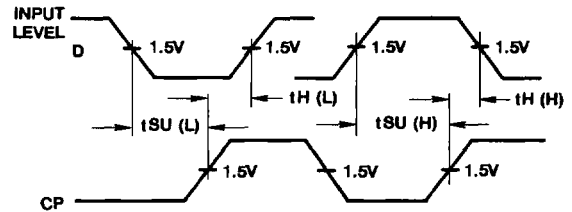
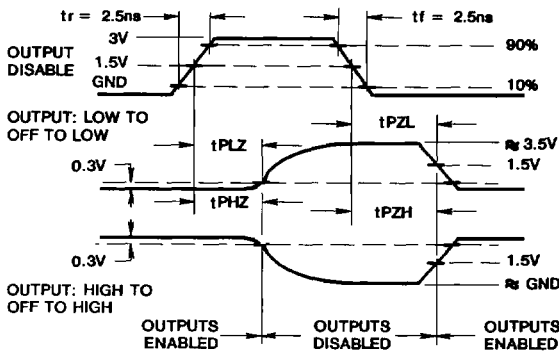


Figure 3 - Setup and hold times.



TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.