

Description

The GM71V18160A is the new generation dynamic RAM organized 1,048,576 words x 16 bits. GM71V18160A has realized higher density, higher performance and various functions by utilizing advanced CMOS process technology. The GM71V18160A offers Fast Page Mode as a high speed access mode. Multiplexed address inputs permit the GM71V18160A to be packaged in standard 400 mil 42 pin plastic SOJ, standard 400 mil 44 (50) pin plastic TSOP II. The package size provides high system bit densities and is compatible with widely available automated testing and insertion equipment.

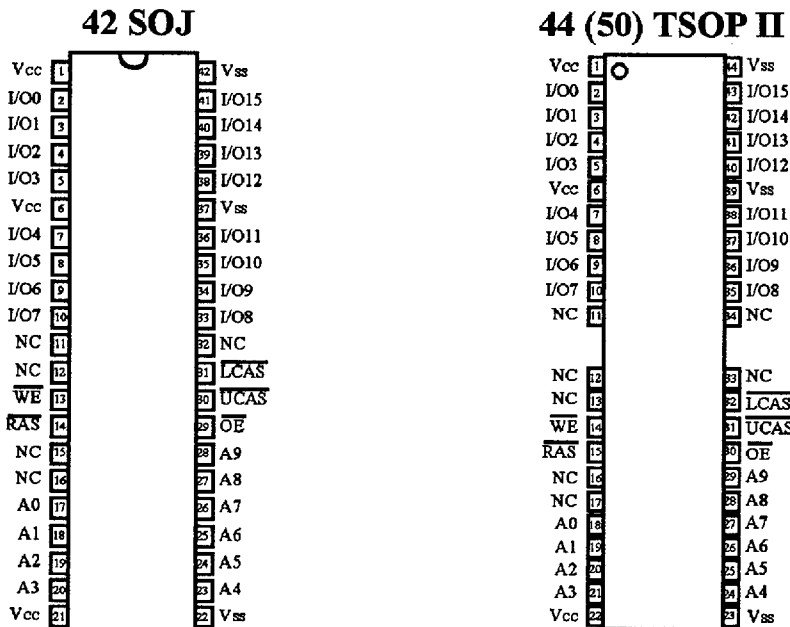
Features

- 1,048,576 Words x 16 Bit Organization
- Fast Page Mode Capability
- Single Power Supply (3.3V ± 0.3V)
- Fast Access Time & Cycle Time (Unit: ns)

| | t _{rac} | t _{cac} | t _{rc} | t _{pc} |
|---------------|------------------|------------------|-----------------|-----------------|
| GM71V18160A-6 | 60 | 15 | 110 | 40 |
| GM71V18160A-7 | 70 | 18 | 130 | 45 |
| GM71V18160A-8 | 80 | 20 | 150 | 50 |

- Low Power
Active : 612/ 540/468mW (MAX)
Standby : 7.2mW (CMOS level : MAX)
0.54mW (L-series : MAX)
- $\overline{\text{RAS}}$ Only Refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh, Hidden Refresh Capability
- Self Refresh Operation (L-series)
- All inputs and outputs TTL Compatible
- 1024 Refresh Cycles/16ms
- 1024 Refresh Cycles/128ms (L-series)
- Battery Back Up Operation (L-series)
- 2 $\overline{\text{CAS}}$ byte Control

Pin Configuration



(Top View)

Pin Description

| Pin | Function | Pin | Function |
|------------------------------------|------------------------|-----------------|-------------------|
| A0-A9 | Address Inputs | \overline{WE} | Read/Write Enable |
| A0-A9 | Refresh Address Inputs | \overline{OE} | Output Enable |
| I/O0-I/O15 | Data-In/Out | V _{cc} | Power (+3.3V) |
| \overline{RAS} | Row Address Strobe | V _{ss} | Ground |
| $\overline{UCAS}, \overline{LCAS}$ | Column Address Strobe | NC | No Connection |

Ordering Information

| Type No. | Access Time | Package |
|--|----------------------|---|
| GM71V18160AJ-6 GM71V18160AJ-7 GM71V18160AJ-8 | 60ns 70ns 80ns | 400 Mil 42 Pin Plastic SOJ |
| GM71V18160AT-6 GM71V18160AT-7 GM71V18160AT-8 | 60ns 70ns 80ns | 400 Mil 44 (50) Pin Plastic TSOP II |
| GM71VS18160ALJ-6 GM71VS18160ALJ-7 GM71VS18160ALJ-8 | 60ns 70ns 80ns | 400 Mil 42 Pin Plastic SOJ |
| GM71VS18160ALT-6 GM71VS18160ALT-7 GM71VS18160ALT-8 | 60ns 70ns 80ns | 400 Mil 44 (50) Pin Plastic TSOP II |

Absolute Maximum Ratings*

| Symbol | Parameter | Rating | Unit |
|-----------------------------------|--|---|------|
| T _A | Ambient Temperature under Bias | 0 ~ 70 | °C |
| T _{STG} | Storage Temperature (Plastic) | -55 ~ 125 | °C |
| V _{IN} /V _{OUT} | Voltage on any Pin Relative to V _{SS} | -0.5 ~ V _{CC} +0.5 (≤4.6V(max)) | V |
| V _{CC} | Voltage on V _{CC} Relative to V _{SS} | -0.5 ~ +4.6 | V |
| I _{OUT} | Short Circuit Output Current | 50 | mA |
| P _D | Power Dissipation | 1.0 | W |

*Note: Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

Recommended DC Operating Conditions (T_A = 0 ~ 70°C)

| Symbol | Parameter | Min | Typ | Max | Unit |
|-----------------|--------------------|------|-----|----------------------|------|
| V _{CC} | Supply Voltage | 3.0 | 3.3 | 3.6 | V |
| V _{IH} | Input High Voltage | 2.0 | - | V _{CC} +0.3 | V |
| V _{IL} | Input Low Voltage | -0.3 | - | 0.8 | V |

*Note: All voltage referred to V_{SS}.

Truth Table

| $\overline{\text{RAS}}$ | $\overline{\text{LCAS}}$ | $\overline{\text{UCAS}}$ | $\overline{\text{WE}}$ | $\overline{\text{OE}}$ | I/O0-I/O7 | I/O8-I/O15 | Operation | Notes |
|-------------------------|--------------------------|--------------------------|------------------------|------------------------|------------------|------------------|-----------------------------------|-------|
| H | H | H | H | H | High-Z | High-Z | Standby | 1,3 |
| L | H | H | H | H | High-Z | High-Z | Refresh | 1,3 |
| L | L | H | H | L | D _{OUT} | High-Z | Lower Byte Read | 1,3 |
| L | H | L | H | L | High-Z | D _{OUT} | Upper Byte Read | 1,3 |
| L | L | L | H | L | D _{OUT} | D _{OUT} | Word Read | 1,3 |
| L | L | H | L | H | D _{IN} | Don't Care | Lower Byte Write | 1,2,3 |
| L | H | L | L | H | Don't Care | D _{IN} | Upper Byte Write | 1,2,3 |
| L | L | L | L | H | D _{IN} | D _{IN} | Word Write | 1,2,3 |
| L | L | L | H | H | High-Z | High-Z | | 1,3 |
| H to L | L | H | - | - | High-Z | High-Z | CBR Refresh or Self Refresh | 1,3 |
| H to L | H | L | - | - | High-Z | High-Z | | |
| H to L | L | L | - | - | High-Z | High-Z | | |

*Note : 1. H: High(inactive), L: Low(active)

2. twcs ≥ 0ns: Early write cycle, twcs ≤ 0ns: Delayed write cycle

3. Mode is determined by the OR function of the $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$. (Mode is set by the earliest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ active edge and reset by the latest of $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ inactive edge.)

However write OPERATION and output High-Z control are done independently by each $\overline{\text{UCAS}}$, $\overline{\text{LCAS}}$.

ex) if $\overline{\text{RAS}}=\text{H to L}$, $\overline{\text{LCAS}}=\text{L}$, $\overline{\text{UCAS}}=\text{H}$, then $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ refresh cycle is selected.

DC Electrical Characteristics ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 0 \sim 70^\circ C$)

| Symbol | Parameter | Min | Max | Unit | Note | |
|-----------|---|-------|----------|---------|------|------|
| V_{OH} | Output Level Output "H" Level Voltage ($I_{OUT} = -2mA$) | 2.4 | V_{CC} | V | | |
| V_{OL} | Output Level Output "L" Level Voltage ($I_{OUT} = 2mA$) | 0 | 0.4 | V | | |
| I_{CC1} | Operating Current Average Power Supply Operating Current (\overline{RAS} , \overline{UCAS} or \overline{LCAS} Cycling: $t_{RC} = t_{RC\ min}$) | 60 ns | - | 170 | mA | 1, 2 |
| | | 70 ns | - | 150 | | |
| | | 80 ns | - | 130 | | |
| I_{CC2} | Standby Current (TTL) Power Supply Standby Current (\overline{RAS} , \overline{UCAS} , $\overline{LCAS} = V_{IH}$, $D_{OUT} = High-Z$) | - | 2 | mA | | |
| I_{CC3} | \overline{RAS} Only Refresh Current Average Power Supply Current \overline{RAS} Only Refresh Mode ($t_{RC} = t_{RC\ min}$) | 60 ns | - | 170 | mA | 2 |
| | | 70 ns | - | 150 | | |
| | | 80 ns | - | 130 | | |
| I_{CC4} | Fast Page Mode Current Average Power Supply Current Fast Page Mode ($t_{RC} = t_{RC\ min}$) | 60 ns | - | 170 | mA | 1, 3 |
| | | 70 ns | - | 150 | | |
| | | 80 ns | - | 130 | | |
| I_{CC5} | Standby Current (CMOS) Power Supply Standby Current (\overline{RAS} , \overline{UCAS} or $\overline{LCAS} \geq V_{CC} - 0.2V$, $D_{OUT} = High-Z$) | - | 1 | mA | | |
| | | - | 0.15 | mA | 4 | |
| I_{CC6} | \overline{CAS} -before- \overline{RAS} Refresh Current ($t_{RC} = t_{RC\ min}$) | 60 ns | - | 170 | mA | |
| | | 70 ns | - | 150 | | |
| | | 80 ns | - | 130 | | |
| I_{CC7} | Battery Back Up Operating Current (Standby with CBR Refresh) ($t_{RC} = 31.3\ \mu s$, $t_{RAS} \leq 0.3\ \mu s$, $D_{OUT} = High-Z$) | - | 0.4 | mA | 4 | |
| I_{CC8} | Standby Current $\overline{RAS} = V_{IH}$ \overline{UCAS} , $\overline{LCAS} = V_{IL}$ $D_{OUT} = Enable$ | - | 5 | mA | 1 | |
| I_{CC9} | Self-Refresh Mode Current (\overline{RAS} , \overline{UCAS} or $\overline{LCAS} \leq 0.2V$, $D_{OUT} = High-Z$) | - | 200 | μA | 4 | |
| $I_{(I)}$ | Input Leakage Current Any Input ($0V \leq V_{IN} \leq 4.6V$) | -10 | 10 | μA | | |
| $I_{(O)}$ | Output Leakage Current (D_{OUT} is Disabled, $0V \leq V_{OUT} \leq 4.6V$) | -10 | 10 | μA | | |

Note: 1. I_{CC} depends on output load condition when the device is selected. $I_{CC(max)}$ is specified at the output open condition.

2. Address can be changed once or less while $\overline{RAS} = V_{IL}$.

3. Address can be changed once or less while \overline{LCAS} and $\overline{UCAS} = V_{IH}$.

4. L-Series & Self-refresh series.

Capacitance ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 25^\circ C$)

| Symbol | Parameter | Min | Max | Unit | Note |
|-----------|----------------------------------|-----|-----|------|------|
| C_{I1} | Input Capacitance (Address) | - | 5 | pF | 1 |
| C_{I2} | Input Capacitance (Clocks) | - | 7 | pF | 1 |
| $C_{I/O}$ | Output Capacitance (Data-In/Out) | - | 7 | pF | 1, 2 |

Note: 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. \overline{LCAS} and $\overline{UCAS} = V_{IH}$ to disable D_{OUT} .

AC Characteristics ($V_{CC} = 3.0V \pm 0.3V$, $T_A = 0 \sim 70^\circ C$, Notes 1, 2, 3, 19)

Test Conditions

Input rise and fall times : 5 ns

Output load : 2TTL gate + CL (100 pF)

Input timing reference levels : 0.8V, 2.0V

(Including scope and jig)

Output timing reference levels : 0.8V, 2.0V

Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameters)

| Symbol | Parameter | GM71V(S)18160 A/AL-6 | | GM71V(S)18160 A/AL-7 | | GM71V(S)18160 A/AL-8 | | Unit | Note |
|-----------|---|-------------------------|--------|-------------------------|--------|-------------------------|--------|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| t_{RC} | Random Read or Write Cycle Time | 110 | - | 130 | - | 150 | - | ns | |
| t_{RP} | \overline{RAS} Precharge Time | 40 | - | 50 | - | 60 | - | ns | |
| t_{CP} | \overline{CAS} Precharge Time | 10 | - | 10 | - | 10 | - | ns | 24 |
| t_{RAS} | \overline{RAS} Pulse Width | 60 | 10,000 | 70 | 10,000 | 80 | 10,000 | ns | |
| t_{CAS} | \overline{CAS} Pulse Width | 15 | 10,000 | 18 | 10,000 | 20 | 10,000 | ns | |
| t_{ASR} | Row Address Set up Time | 0 | - | 0 | - | 0 | - | ns | |
| t_{RAH} | Row Address Hold Time | 10 | - | 10 | - | 10 | - | ns | |
| t_{ASC} | Column Address Set-up Time | 0 | - | 0 | - | 0 | - | ns | 21 |
| t_{CAH} | Column Address Hold Time | 10 | - | 15 | - | 15 | - | ns | 21 |
| t_{RCD} | \overline{RAS} to \overline{CAS} Delay Time | 20 | 45 | 20 | 52 | 20 | 60 | ns | 3 |
| t_{RAD} | \overline{RAS} to Column Address Delay Time | 15 | 30 | 15 | 35 | 15 | 40 | ns | 4 |
| t_{RSH} | \overline{RAS} Hold Time | 15 | - | 18 | - | 20 | - | ns | |
| t_{CSH} | \overline{CAS} Hold Time | 60 | - | 70 | - | 80 | - | ns | |
| t_{CRP} | \overline{CAS} to \overline{RAS} Precharge Time | 5 | - | 5 | - | 5 | - | ns | |
| t_{ODD} | \overline{OE} to D_{IN} Delay Time | 15 | - | 18 | - | 20 | - | ns | 5 |
| t_{DZO} | \overline{OE} Delay Time from D_{IN} | 0 | - | 0 | - | 0 | - | ns | 6 |
| t_{DZC} | \overline{CAS} Delay Time from D_{IN} | 0 | - | 0 | - | 0 | - | ns | 6 |
| t_T | Transition Time (Rise and Fall) | 3 | 50 | 3 | 50 | 3 | 50 | ns | 7 |
| t_{REF} | Refresh Period(1024 cycles) | - | 16 | - | 16 | - | 16 | ms | |
| | Refresh Period (1024 cycles, L-Series) | - | 128 | - | 128 | - | 128 | ms | |

Read Cycle

| Symbol | Parameter | GM71V(S)18160 A/AL-6 | | GM71V(S)18160 A/AL-7 | | GM71V(S)18160 A/AL-8 | | Unit | Note |
|------------------|--|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|-----------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{RAC} | Access Time from \overline{RAS} | - | 60 | - | 70 | - | 80 | ns | 8, 9 |
| t _{CAC} | Access Time from \overline{CAS} | - | 15 | - | 18 | - | 20 | ns | 9, 10, 17 |
| t _{AA} | Access Time from Address | - | 30 | - | 35 | - | 40 | ns | 9, 11, 17 |
| t _{OAC} | Access Time from \overline{OE} | - | 15 | - | 18 | - | 20 | ns | 9,25 |
| t _{RCS} | Read Command Setup Time | 0 | - | 0 | - | 0 | - | ns | 21 |
| t _{RCH} | Read Command Hold Time to \overline{CAS} | 0 | - | 0 | - | 0 | - | ns | 12,22 |
| t _{RRH} | Read Command Hold Time to \overline{RAS} | 0 | - | 0 | - | 0 | - | ns | 12 |
| t _{RAL} | Column Address to \overline{RAS} Lead Time | 30 | - | 35 | - | 40 | - | ns | |
| t _{CAL} | Column Address to \overline{CAS} Lead Time | 30 | - | 35 | - | 40 | - | ns | |
| t _{CLZ} | \overline{CAS} to Output in Low-Z | 0 | - | 0 | - | 0 | - | ns | |
| t _{OH} | Output Data Hold Time | 3 | - | 3 | - | 3 | - | ns | |
| t _{OHO} | Output Data Hold Time from \overline{OE} | 3 | - | 3 | - | 3 | - | ns | |
| t _{OFF} | Output Buffer Turn-off time | - | 15 | - | 15 | - | 15 | ns | 13 |
| t _{OEZ} | Output Buffer Turn-off Time to \overline{OE} | - | 15 | - | 15 | - | 15 | ns | 13 |
| t _{CDD} | \overline{CAS} to D _{IN} Delay Time | 15 | - | 18 | - | 20 | - | ns | 5 |

Write Cycle

| Symbol | Parameter | GM71V(S)18160 A/AL-6 | | GM71V(S)18160 A/AL-7 | | GM71V(S)18160 A/AL-8 | | Unit | Note |
|------------------|---|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{WCS} | Write Command Setup Time | 0 | - | 0 | - | 0 | - | ns | 14,21 |
| t _{WCH} | Write Command Hold Time | 10 | - | 15 | - | 15 | - | ns | 21 |
| t _{WP} | Write Command Pulse Width | 10 | - | 10 | - | 10 | - | ns | |
| t _{RWL} | Write Command to \overline{RAS} Lead Time | 15 | - | 18 | - | 20 | - | ns | |
| t _{CWL} | Write Command to \overline{CAS} Lead Time | 15 | - | 18 | - | 20 | - | ns | 23 |
| t _{DS} | Data-in Setup Time | 0 | - | 0 | - | 0 | - | ns | 15,23 |
| t _{DH} | Data-in Hold Time | 10 | - | 15 | - | 15 | - | ns | 15,23 |

Read-Modify-Write Cycle

| Symbol | Parameter | GM71V(S)18160 A/AL-6 | | GM71V(S)18160 A/AL-7 | | GM71V(S)18160 A/AL-8 | | Unit | Note |
|------------------|--|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{RWC} | Read-Modify-Write Cycle Time | 155 | - | 181 | - | 205 | - | ns | |
| t _{RWD} | $\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time | 85 | - | 98 | - | 110 | - | ns | 14 |
| t _{CWD} | $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay Time | 40 | - | 46 | - | 50 | - | ns | 14 |
| t _{AWD} | Column Address to $\overline{\text{WE}}$ Delay Time | 55 | - | 63 | - | 70 | - | ns | 14 |
| t _{OEH} | $\overline{\text{OE}}$ Hold Time from $\overline{\text{WE}}$ | 15 | - | 18 | - | 20 | - | ns | |

Refresh Cycle

| Symbol | Parameter | GM71V(S)18160 A/AL-6 | | GM71V(S)18160 A/AL-7 | | GM71V(S)18160 A/AL-8 | | Unit | Note |
|------------------|---|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{CSR} | $\overline{\text{CAS}}$ Setup Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle) | 5 | - | 5 | - | 5 | - | ns | 21 |
| t _{CHR} | $\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle) | 10 | - | 10 | - | 10 | - | ns | 22 |
| t _{RPC} | $\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time | 0 | - | 0 | - | 0 | - | ns | 21 |

Fast Page Mode Cycle

| Symbol | Parameter | GM71V(S)18160 A/AL-6 | | GM71V(S)18160 A/AL-7 | | GM71V(S)18160 A/AL-8 | | Unit | Note |
|-------------------|--|-------------------------|---------|-------------------------|---------|-------------------------|---------|------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PC} | Fast Page Mode Cycle Time | 40 | - | 45 | - | 50 | - | ns | |
| t _{RASC} | Fast Page Mode $\overline{\text{RAS}}$ Pulse Width | - | 100,000 | - | 100,000 | - | 100,000 | ns | 16 |
| t _{ACP} | Access Time from $\overline{\text{CAS}}$ Precharge | - | 35 | - | 40 | - | 45 | ns | 9, 17 |
| t _{RHCP} | $\overline{\text{RAS}}$ Hold Time from $\overline{\text{CAS}}$ Precharge | 35 | - | 40 | - | 45 | | ns | |

Fast Page Mode Read-Modify-Write Cycle

| Symbol | Parameter | GM71V(S)18160 A/AL-6 | | GM71V(S)18160 A/AL-7 | | GM71V(S)18160 A/AL-8 | | Unit | Note |
|-------------------|--|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|-------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{PRWC} | Fast Page Mode Read-Modify-Write Cycle Time | 85 | - | 96 | - | 105 | - | ns | |
| t _{CPW} | $\overline{\text{WE}}$ Delay Time from $\overline{\text{CAS}}$ Precharge | 60 | - | 68 | - | 75 | - | ns | 14,22 |

Self Refresh Mode

| Symbol | Parameter | GM71VS18160 AL-6 | | GM71VS18160 AL-7 | | GM71VS18160 AL-8 | | Unit | Note |
|-------------------|---|---------------------|-----|---------------------|-----|---------------------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| t _{RASS} | $\overline{\text{RAS}}$ Pulse Width (Self-Refresh) | 100 | - | 100 | - | 100 | - | us | 26 |
| t _{RPS} | $\overline{\text{RAS}}$ Precharge Time (Self-Refresh) | 110 | - | 130 | - | 150 | - | ns | |
| t _{CHS} | $\overline{\text{CAS}}$ Hold Time (Self-Refresh) | -50 | - | -50 | - | -50 | - | ns | 23 |

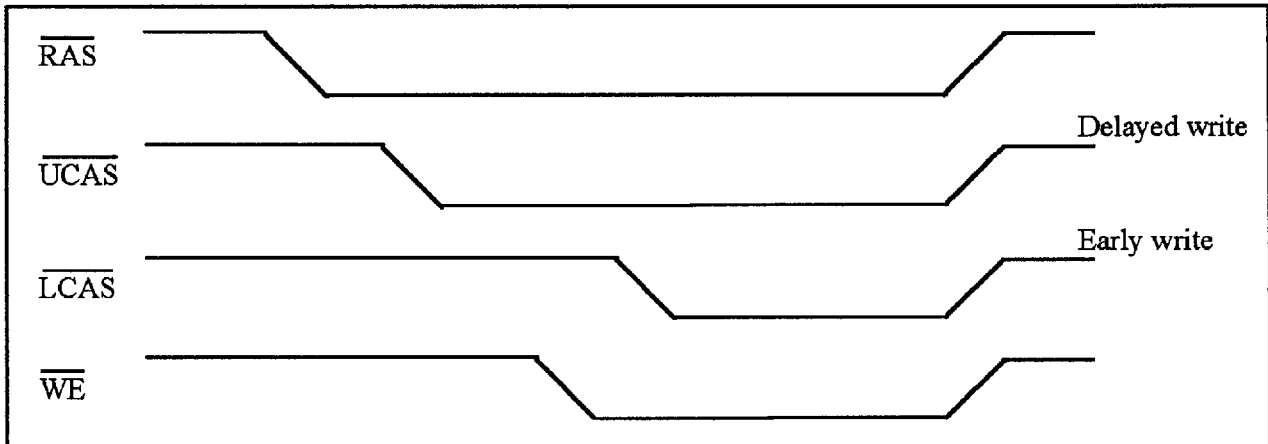
- Notes :**
- AC measurements assume $t_r = 5$ ns.
 - An initial pause of 200us is required after power followed by a minimum of eight initialization cycles (any combination of cycles containing RAS-only refresh or CAS-before-RAS refresh).
 - Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 - Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 - Either t_{ODD} or t_{CDD} must be satisfied.
 - Either t_{DZO} or t_{DZC} must be satisfied.
 - $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 2TTL loads and 100pF. ($V_{OH}=2.4V$, $V_{OL}=0.4V$)
 - Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 - Either t_{RCH} or t_{RRH} must be satisfied for a read cycles.
 - $t_{OFF}(\text{max})$ and $t_{OEZ}(\text{max})$ define the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.
 - t_{WCS} , t_{RWd} , t_{CWD} , t_{AWd} and t_{CPW} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit(high impedance) throughout the entire cycle; if $t_{RWd} \geq t_{RWd}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$, and $t_{AWd} \geq t_{AWd}(\text{min})$, or $t_{CWD} \geq t_{CWD}(\text{min})$, $t_{AWd} \geq t_{AWd}(\text{min})$ and $t_{CPW} \geq t_{CPW}(\text{min})$, the cycle is a read-modify-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 - These parameters are referred to $\overline{\text{UCAS}}$ and $\overline{\text{LCAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 - t_{RASC} defines $\overline{\text{RAS}}$ pulse width in fast page mode cycles.
 - Access time is determined by the longer of t_{AA} or t_{CAC} or t_{ACP} .
 - In delayed write or read-modify-write cycles, $\overline{\text{OE}}$ must disable output buffer prior to applying data to the device. After $\overline{\text{RAS}}$ is reset, if $t_{OEh} \geq t_{CWL}$, the I/O pin will remain open circuit (high impedance); if $t_{OEh} \leq t_{CWL}$, invalid data will be out at each I/O.
 - When both $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ go low at the same time, all 16-bits data are written into the device. $\overline{\text{LCAS}}$ and $\overline{\text{UCAS}}$ cannot be staggered within the same write/read cycles.
 - All the Vcc and Vss pins shall be supplied with the same voltages.

21. t_{ASC} , t_{CAH} , t_{RCS} , t_{WCS} , t_{WCH} , t_{CSR} and t_{RPC} are determined by the earlier falling edge of \overline{UCAS} or \overline{LCAS} .
22. t_{CRP} , t_{CHR} , t_{RCH} , t_{ACP} and t_{CPW} are determined by the later rising edge of \overline{UCAS} or \overline{LCAS} .
23. t_{CWL} , t_{DH} , t_{DS} and t_{CHS} should be satisfied by both \overline{UCAS} and \overline{LCAS} .
24. t_{CP} is determined by the time that both \overline{UCAS} and \overline{LCAS} are high.
25. When output buffers are enabled once, sustain the low impedance state until valid data is obtained. When output buffer is turned on and off within a very short time, generally it causes large V_{CC}/V_{SS} line noise, which causes to degrade $V_{IH\ min}/V_{IL\ max}$ level.
26. Please do not use t_{RASS} timing, $10\ \mu s \leq t_{RASS} \leq 100\ \mu s$. During this period, the device is in transition state from normal operation mode to self refresh mode. If $t_{RASS} \geq 100\ \mu s$, then \overline{RAS} precharge time should use t_{RPS} instead of t_{RP} .
27. If you use distributed CBR refresh mode with $15.6\ \mu s$ interval in normal read/write cycle, CBR refresh should be executed within $15.6\ \mu s$ immediately after exiting from and before entering into self refresh mode.
28. If you use \overline{RAS} only refresh or CBR burst refresh mode in normal read / write cycle, 1024 cycles of dustributed CBR refresh with $15.6\ \mu s$ interval should be executed within 16ms immediately after exiting from and before entering into the self refresh mode.
29. Repetitive self refresh mode without refreshing all memory is not allowed. Once you exit from self refresh mode, all memory cells need to be refreshed before re-entering the self refresh mode again.

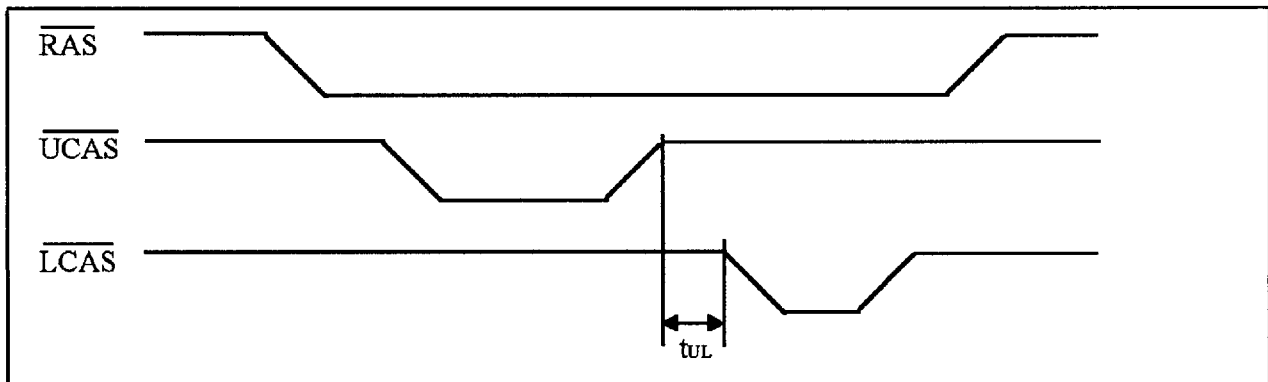
Notes concerning $2C_{AS}$ control

Please do not separate the $\overline{UCAS}/\overline{LCAS}$ operation timing intentionally. However skew between $\overline{UCAS}/\overline{LCAS}$ are allowed under the following conditions.

- (1) Each of the $\overline{UCAS}/\overline{LCAS}$ should satisfy the timing specifications individually.
- (2) Different operation mode for upper / lower byte is not allowed; such as following.



- (3) Closely separated upper / lower control is not allowed. However when the condition ($t_{CP} \leq t_{UL}$) is satisfied, fast page mode can be performed.



Timing Waveforms

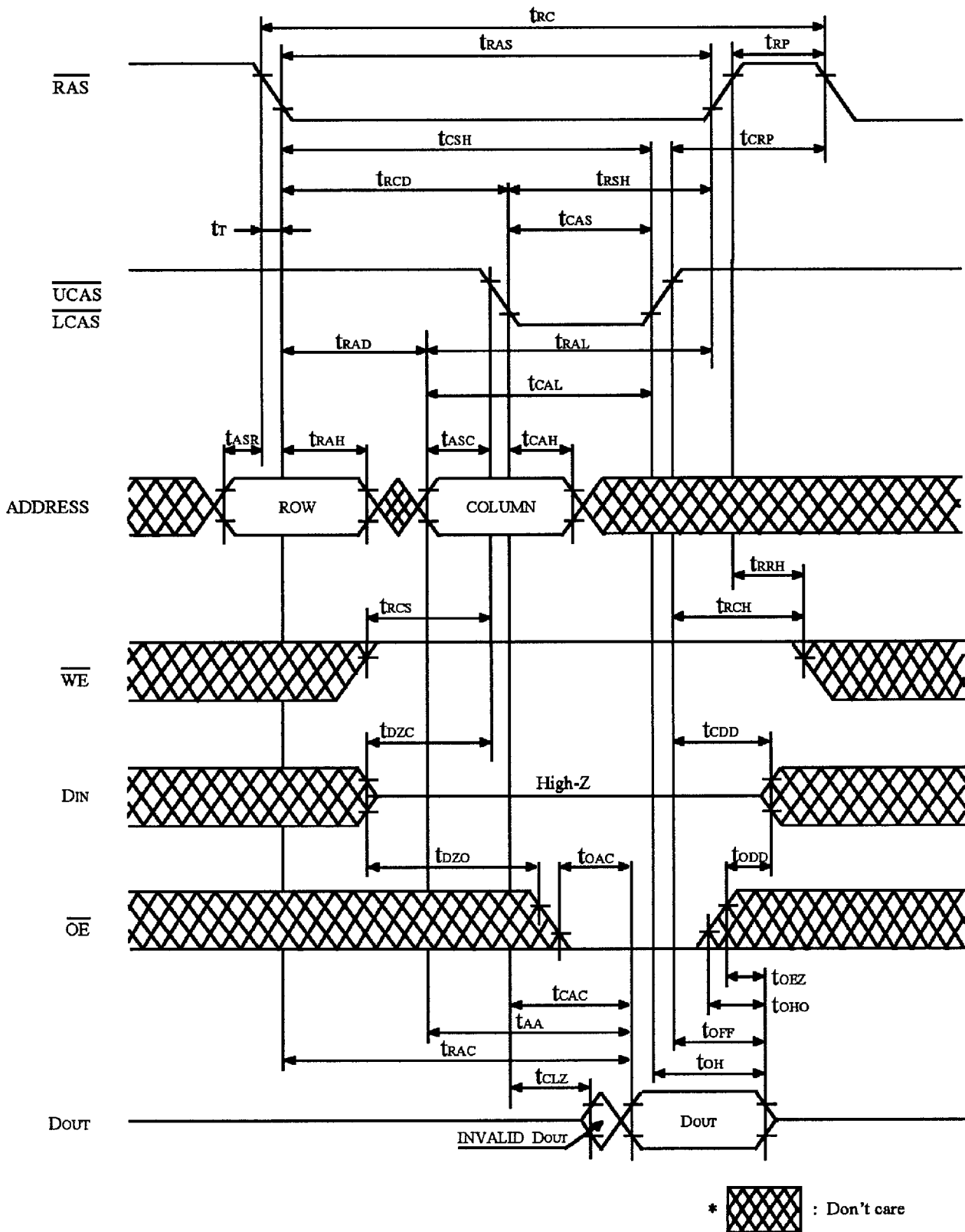
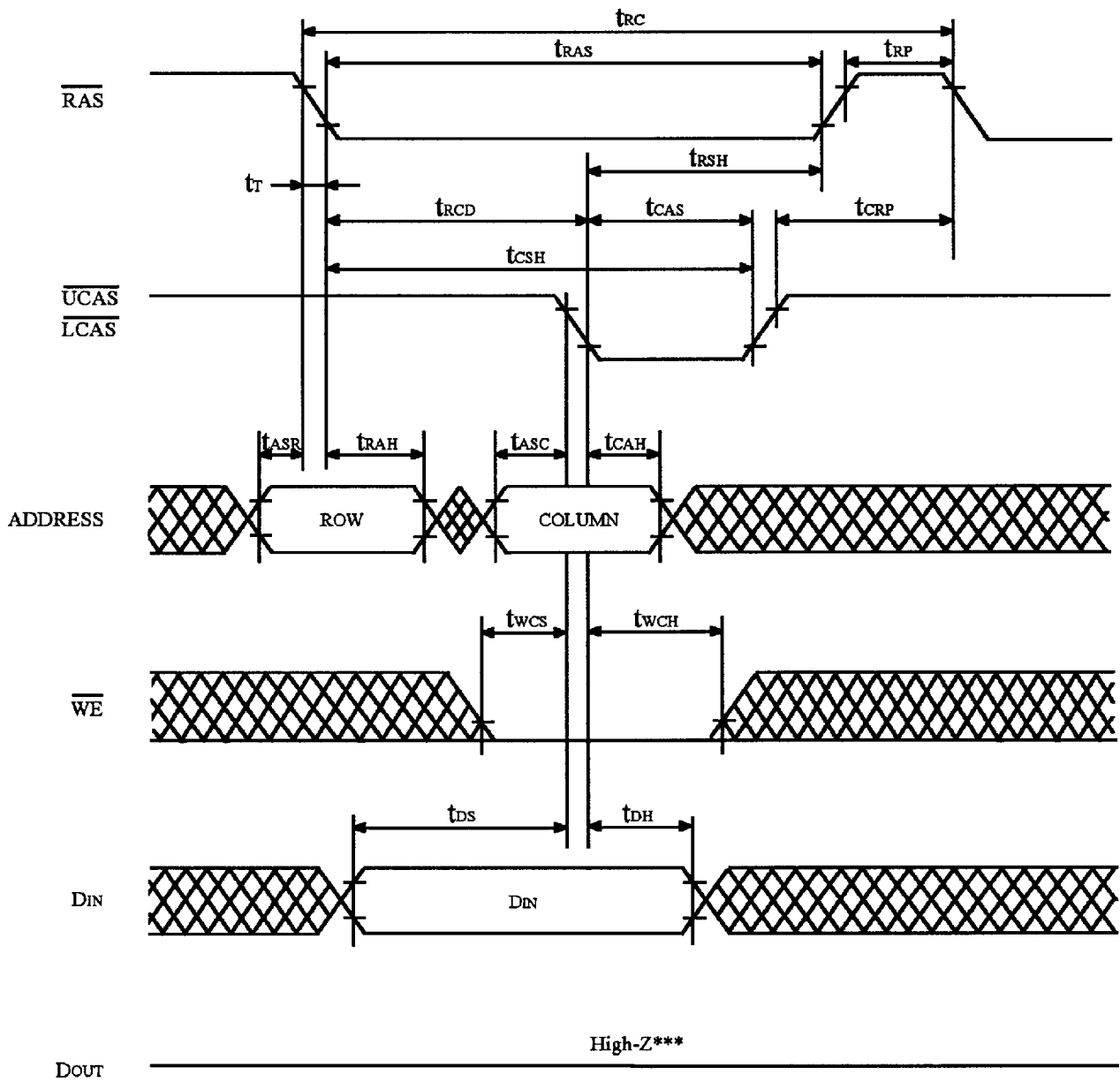


FIGURE 1. READ CYCLE




- *  : Don't care
- ** \overline{OE} : Don't care
- *** $t_{wcs} \geq t_{wcs}(\text{min})$

FIGURE 2. EARLY WRITE CYCLE

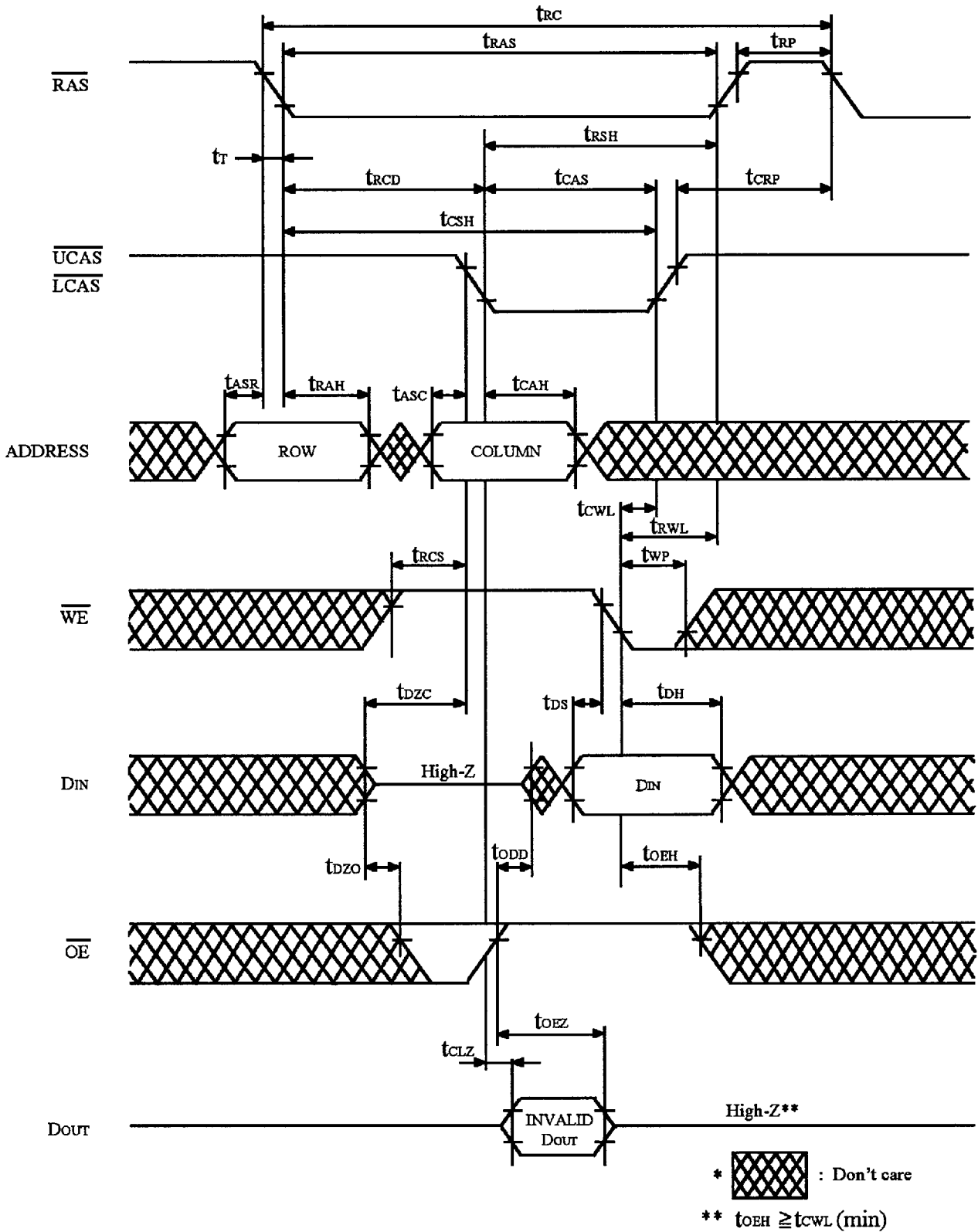


FIGURE 3. DELAYED WRITE CYCLE *19

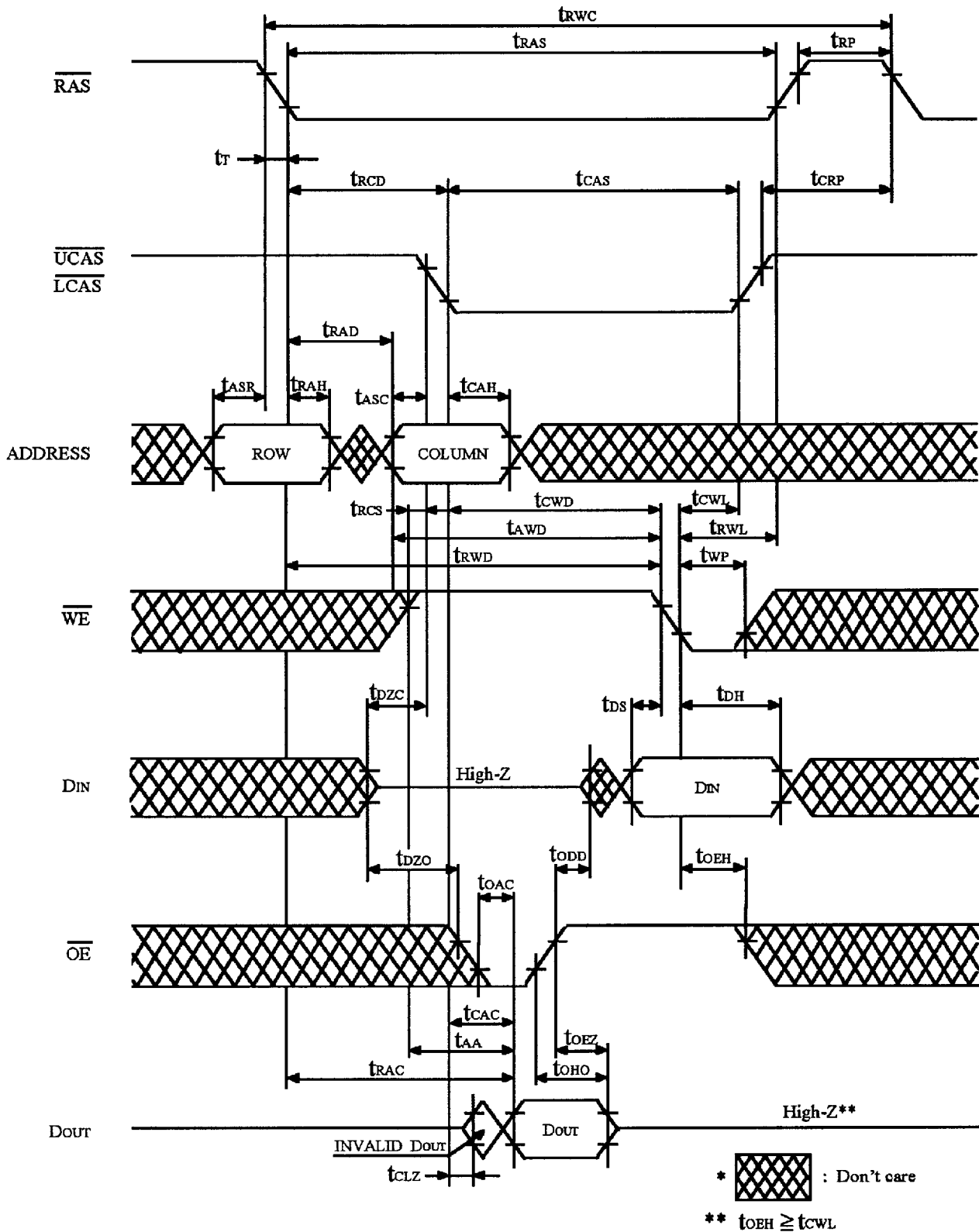


FIGURE 4. READ MODIFY WRITE CYCLE *19

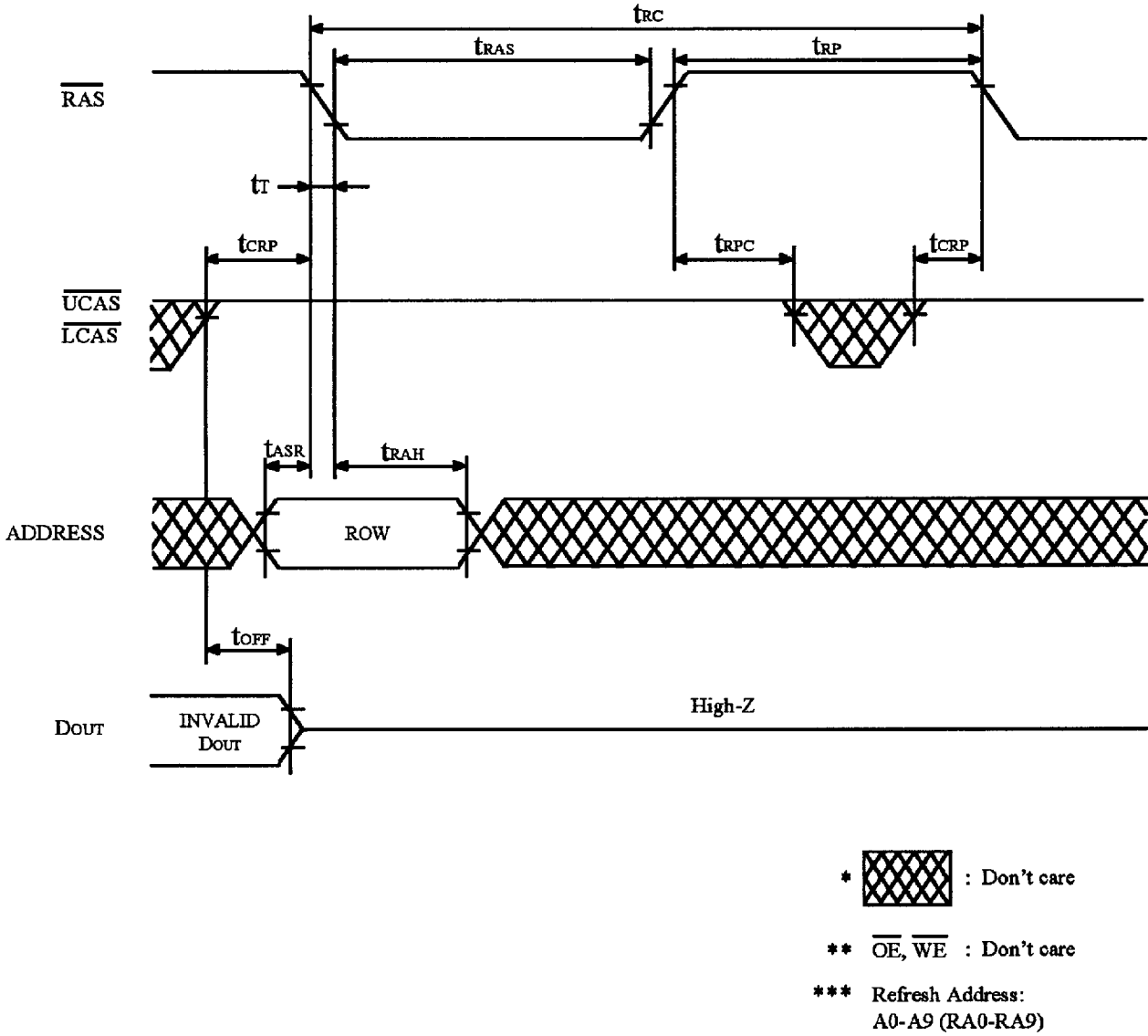


FIGURE 5. $\overline{\text{RAS}}$ ONLY REFRESH CYCLE

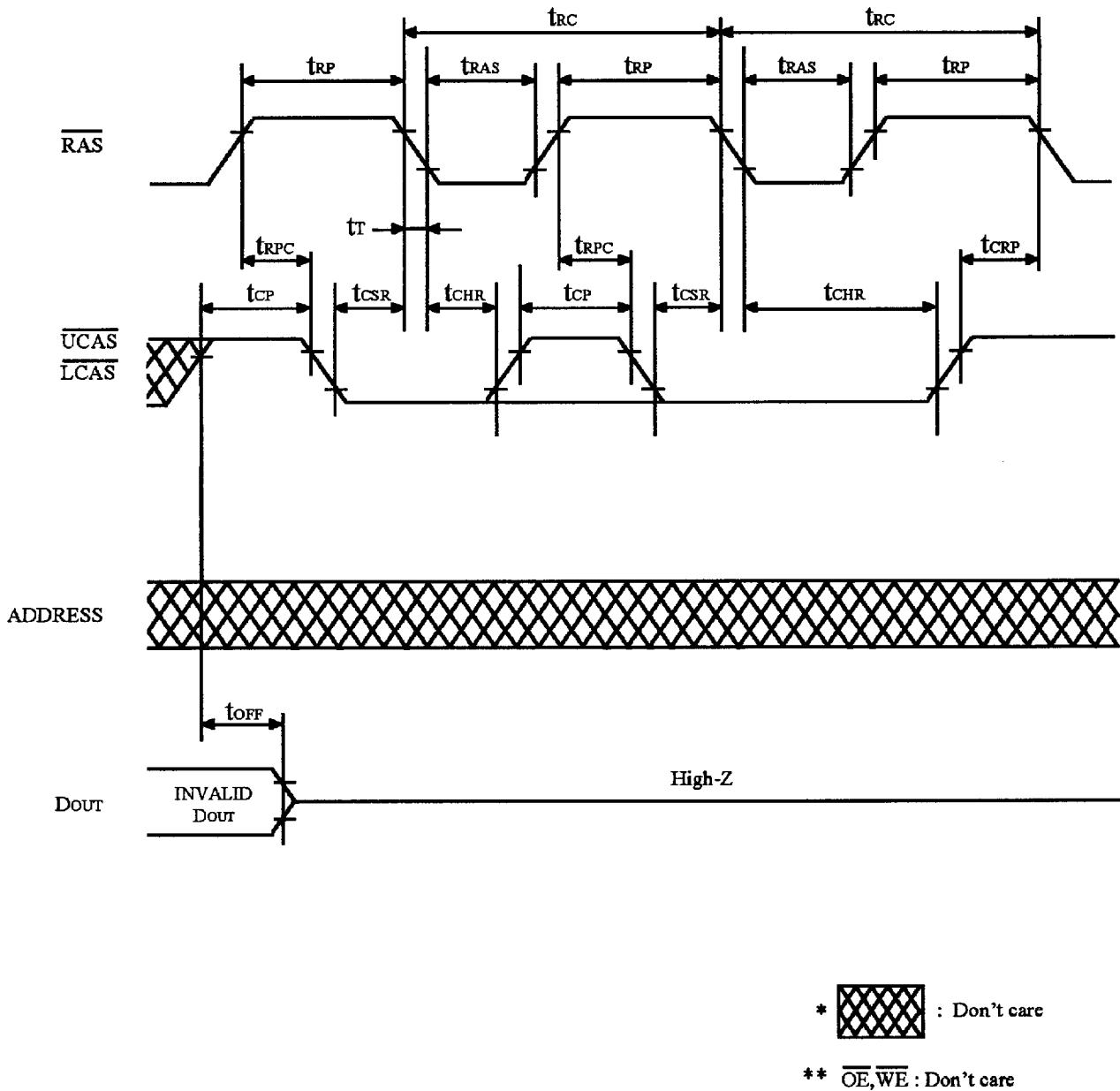


FIGURE 6. \overline{CAS} BEFORE \overline{RAS} REFRESH CYCLE

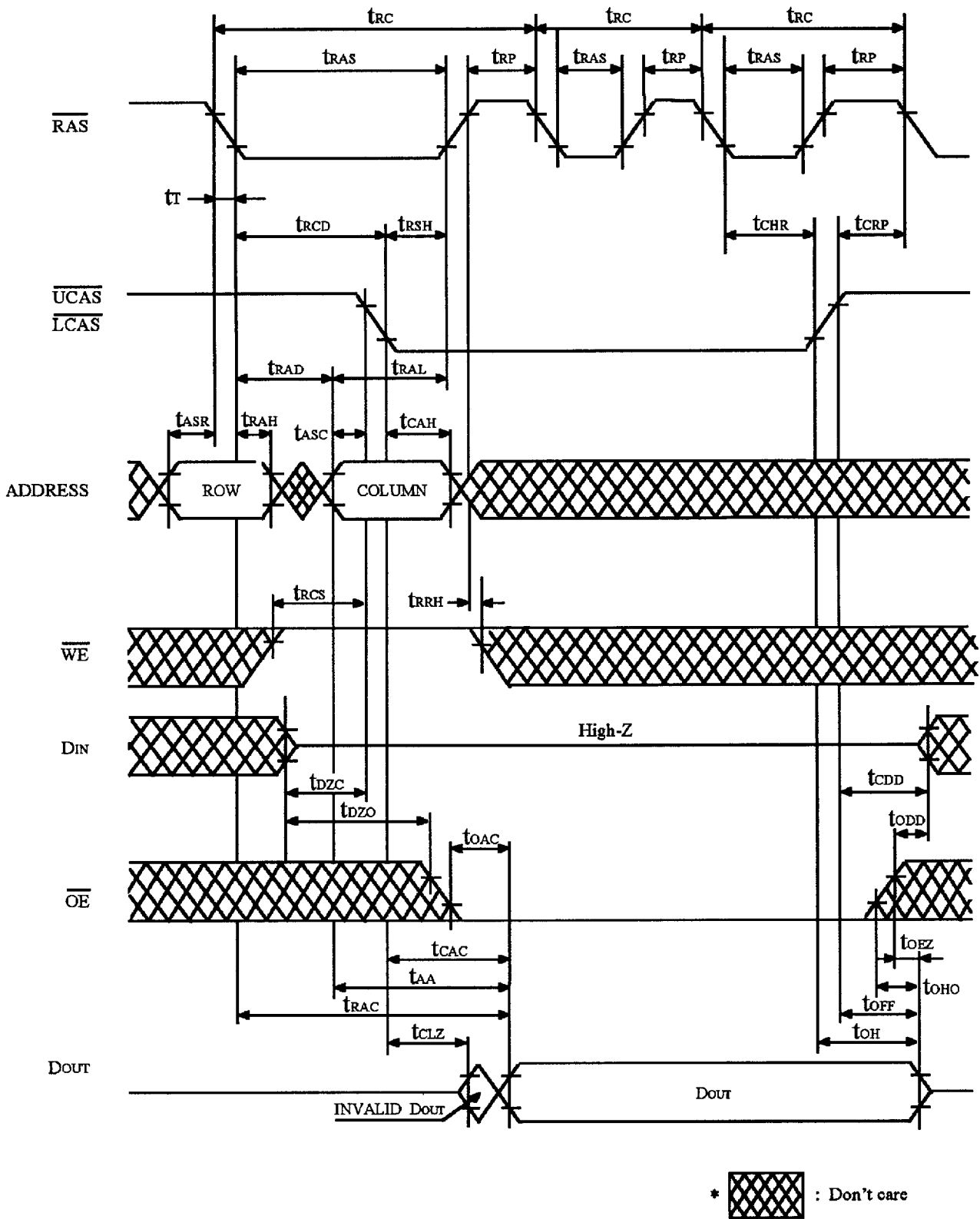


FIGURE 7. HIDDEN REFRESH CYCLE

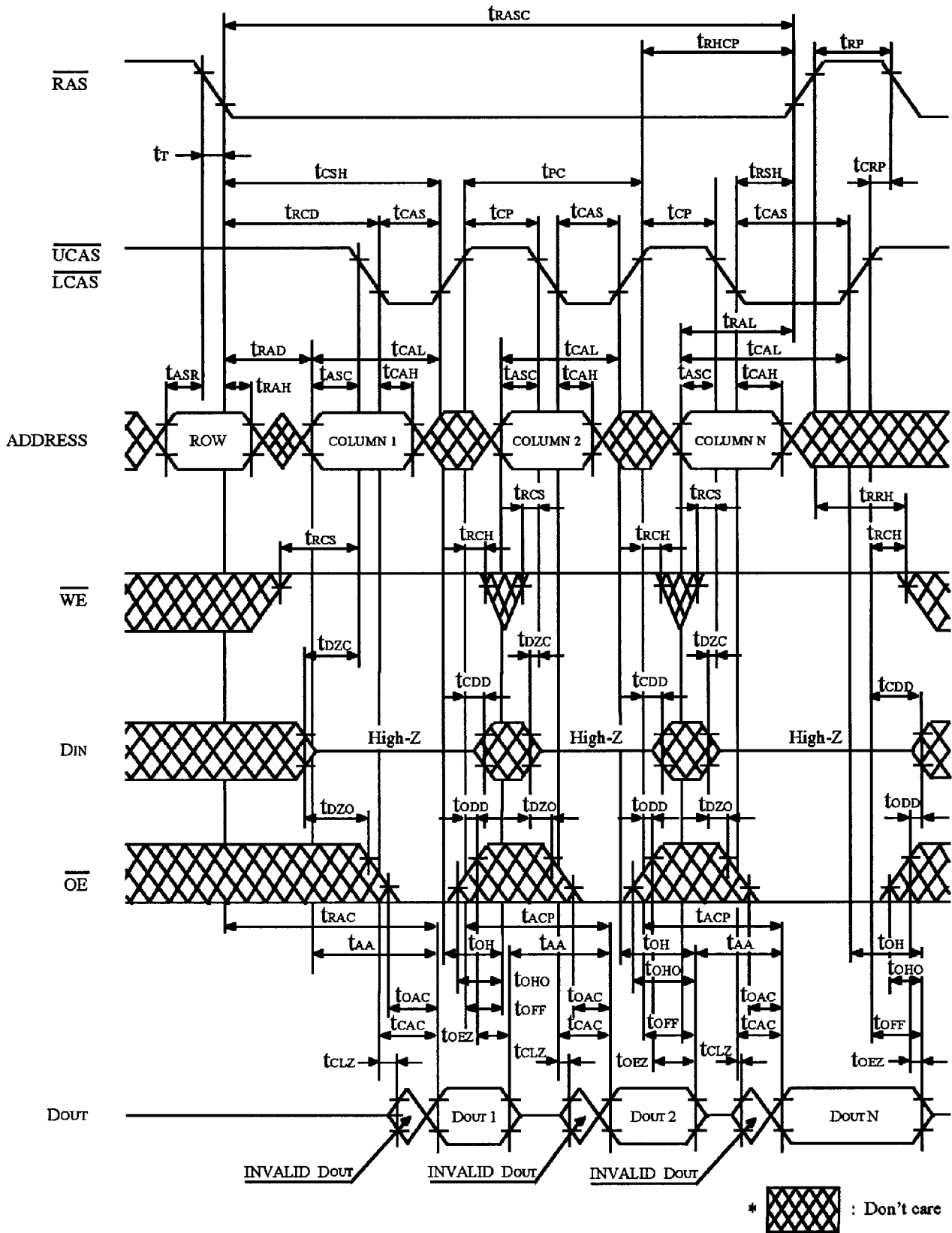


FIGURE 8. FAST PAGE MODE READ CYCLE

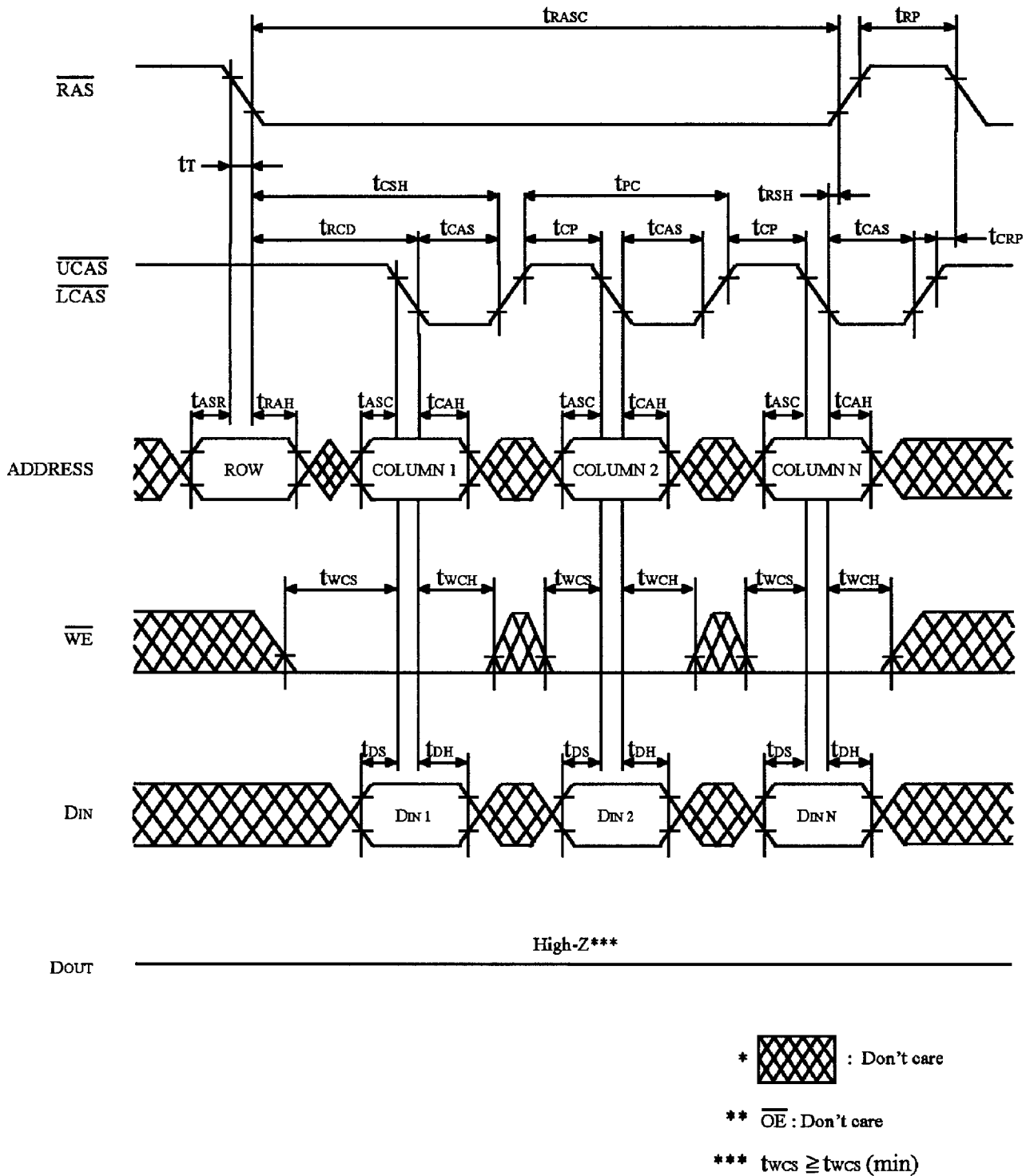


FIGURE 9. FAST PAGE MODE EARLY WRITE CYCLE

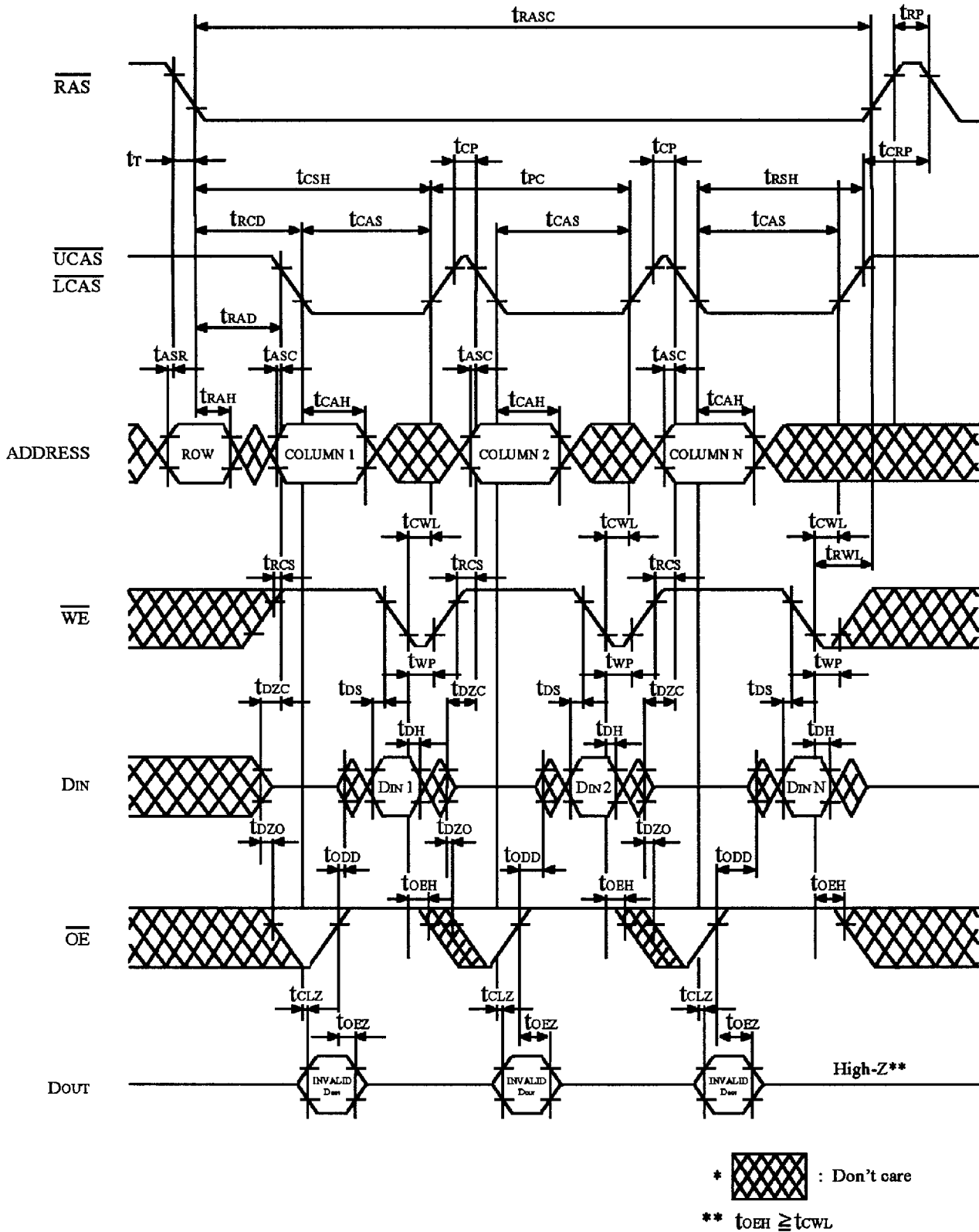


FIGURE 10. FAST PAGE MODE DELAYED WRITE CYCLE *19

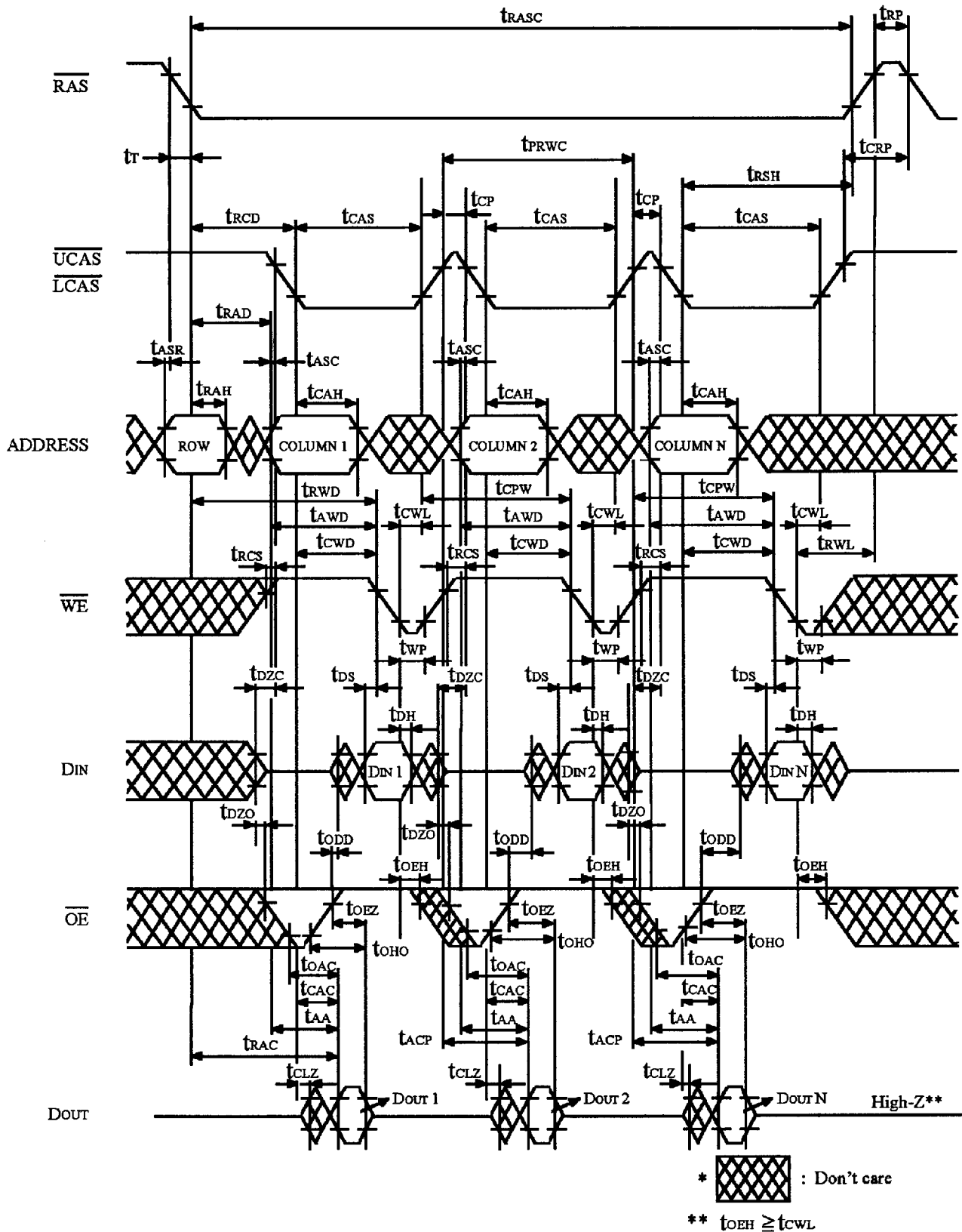


FIGURE 11. FAST PAGE MODE READ MODIFY WRITE CYCLE *19

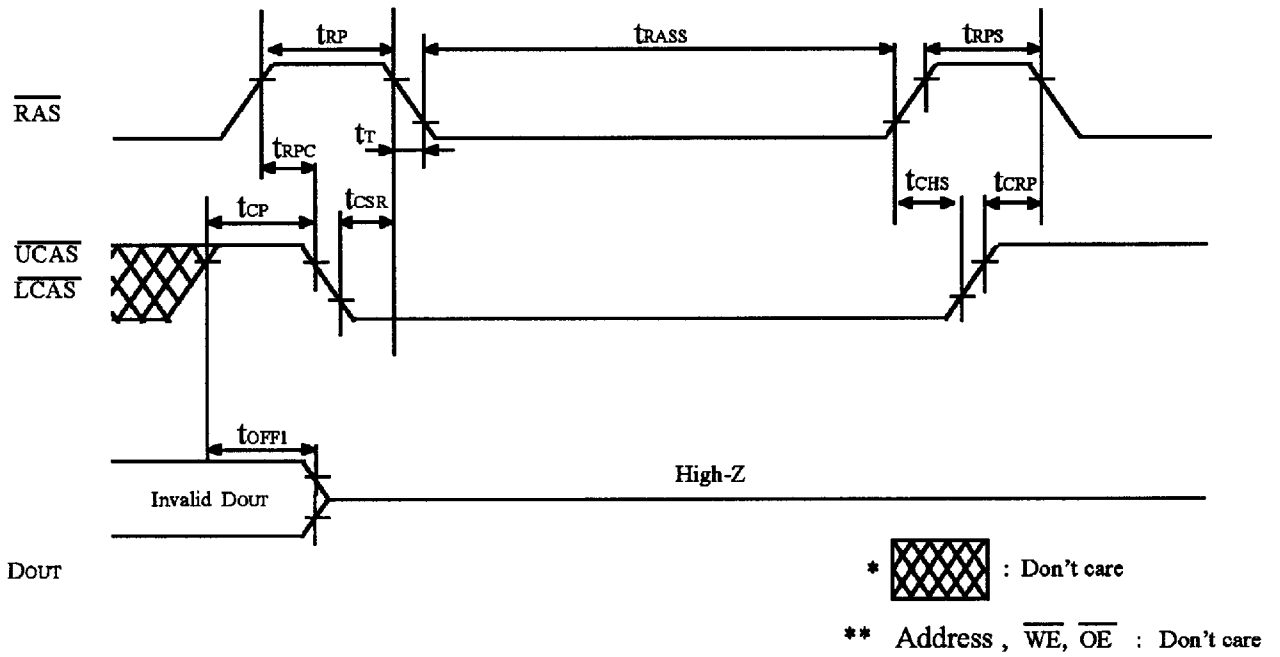
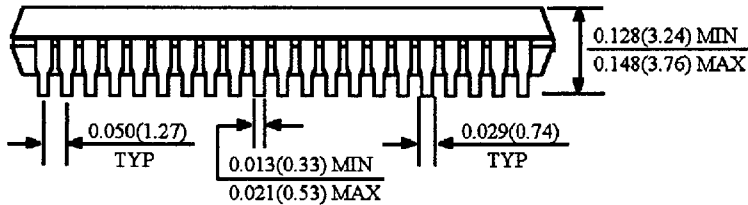
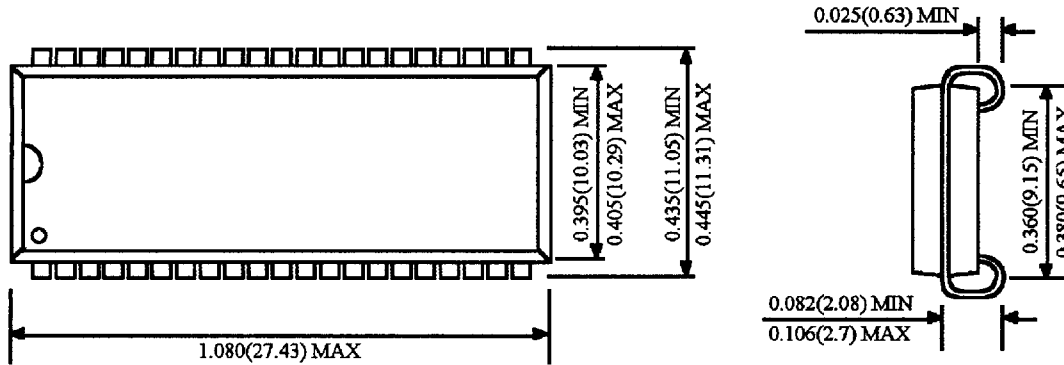


FIGURE 12. SELF-REFRESH CYCLE *26,27,28,29

Package Dimensions

Unit: Inches (mm)

42 SOJ



44(50) TSOP II

