PIN DESCRIPTION

Pin No.	Name	I/O	Description
1	$\overline{OE}_R$	I	RECEIVE enable input.
2–9	R_i	I/O	8-bit RECEIVE data output.
10	$\overline{ERR}$	O	Output from fault registers. Registers detection of odd parity fault on using clock edge (CLK). A registered $\overline{ERR}$ output remains low until cleared. Open drain output, requires pull up resistor.
11	$\overline{CLR}$	O	Clears the fault register output.
16–23	T_i	I/O	8-bit TRANSMIT data output.
15	PARITY	I/O	1-bit PARITY output.
14	$\overline{OE}_T$	I	TRANSMIT enable input.
13	$\overline{EN}$	I	Latch enable for the Error Flag Latch.

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FUNCTION TABLE — 'FCT853 (NONINVERTING)

Inputs						Outputs				Function
$\overline{OE}_T$	$\overline{OE}_R$	$\overline{CLR}$	CLK	R_i (Σ of H'S)	T_i Incl PARITY (Σ of H'S)	R_i	T_i	PARITY	$\overline{ERR}$[1]	
L	H	–	–	H (Odd)	NA	NA	H	L	NA	Transmit data from R Port
L	H	–	–	H (Even)	NA	NA	H	H	NA	to T Port with parity;
L	H	–	–	L (Odd)	NA	NA	L	L	NA	receiving path is disabled.
L	H	–	–	L (Even)	NA	NA	L	H	NA	
H	L	L	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port
H	L	L	L	NA	H (Even)	H	NA	NA	L	to R Port with parity test
H	L	L	L	NA	L (Odd)	L	NA	NA	H	resulting in flag; transmitting
H	L	L	L	NA	L (Even)	L	NA	NA	L	path is disabled.
H	L	H	L	NA	H (Odd)	H	NA	NA	H	Receive data from T Port
H	L	H	L	NA	H (Even)	H	NA	NA	L	to R Port, pass the error test
H	L	H	L	NA	L (Odd)	L	NA	NA	H	resulting to error flag;
H	L	H	L	NA	H (Even)	L	NA	NA	L	transmitting path is disabled.
H	L	H	H	NA	–	–	NA	NA	$\overline{ERR}_{n-1}$	Store the state of error flag register.
–	–	L	H	–	–	–	NA	NA	H	Clear the state of error flag register.
H	H	H	H	–	–	Z	Z	Z	NC	Both transmitting and
H	H	L	H	–	–	Z	Z	Z	H	receiving paths are disabled.
H	H	–	L	L (Odd)	–	Z	Z	Z	H	Parity logic defaults to
H	H	–	L	H (Even)	–	Z	Z	Z	L	transmit mode.
L	L	–	–	H (Odd)	NA	NA	H	H	NA	Forced-error checking.
L	L	–	–	H (Even)	NA	NA	H	L	NA	
L	L	–	–	L (Odd)	NA	NA	L	H	NA	
L	L	–	–	L (Even)	NA	NA	L	L	NA	

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H = High
L = Low
NC = No Change

Z = High Impedance
NA = Not Applicable
$\overline{ERR}_{n-1}$ = Pre-state of $\overline{ERR}$
– = Don't care or irrelevant

Odd = Odd number of logic one's
Even = Even number of logic one's
i = 0, 1, 2, 3, 4, 5, 6, 7
⌐ = Low to High transition of clock

Note:
1. Output state assumes HIGH output pre-state.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
I_{CC}	Quiescent Power Supply Current (CMOS inputs)	0.003	0.5	mA	V_{CC} = MAX, f_1 = 0, Outputs Open, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 3.4V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = GND, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$,
I_C	Total Power Supply Current[5]	1.4	3.4	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}$ -0.2V
		1.9	5.4	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, One Bit Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, V_{IN} = 3.4V or V_{IN} = GND
		4.0	7.8[4]	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		6.2	16.8[4]	mA	V_{CC} = MAX 50% Duty Cycle, Outputs Open, Eight Bits Toggling, f_0 = 10MHz, $\overline{OE}_T$ = GND, $\overline{OE}_R$ = V_{CC}, f_1 = 2.5MHz, V_{IN} = 3.4V or V_{IN} GND

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Notes:

1. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
2. Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
   D_H = Duty Cycle for TTL inputs High
   N_T = Number of TTL inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

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ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	–65 to +150	°C
T_A	Ambient Temperature Under Bias	–65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	–0.5 to +7.0	V
I_{IN}	Input Current	–30 to +5.0	mA

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Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	–0.5 to V_{CC} + 0.5	V
V_{OUT}	Voltage Applied to Output	–0.5 to V_{CC} + 0.5	V

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Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	–55°C	+125°C
Commercial	0°C	+70°C

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Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1823 Tbl 04

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage		–0.5		0.8	V		
V_H	Hysteresis			0.35		V		All inputs
V_{CD}	Input Clamp Diode Voltage			–0.7	–1.2	V	MIN	I_{IN} = –18mA
V_{OH}	Output High Voltage (Except ERR)	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V	V_{CC} – 0.2	V_{CC}		V		I_{OH} = –32µA
		Military/Commercial (CMOS)	V_{CC} – 0.2	V_{CC}		V	MIN	I_{OH} = –300µA
		Military (TTL)	2.4	4.3		V	MIN	I_{OH} = –15mA
		Commercial (TTL)	2.4	4.3		V	MIN	I_{OH} = –24mA
V_{OL}	Output Low Voltage	V_{CC} = 3V, V_{IN} = 0.2V, or V_{CC} – 0.2V		GND	0.2	V		I_{OL} = 300µA
		Military/Commercial (CMOS) All Other		GND	0.2	V	MIN	I_{OL} = 300µA
		Military (TTL) Outputs		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial (TTL)		0.3	0.5	V	MIN	I_{OL} = 48mA
		Military/Commercial (TTL) $\overline{ERR}$		0.3	0.5	V	MIN	I_{OL} = 48mA
I_{IH}	Input HIGH Current (Except I/O Pins)				5	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (Except I/O Pins)				–5	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3] (Except I/O Pins)				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3] (Except I/O Pins)				–5	µA	MAX	V_{IN} = 0.5V
I_{IH}	Input HIGH Current (I/O Pins only)				15	µA	MAX	V_{IN} = V_{CC}
I_{IL}	Input LOW Current (I/O Pins only)				–15	µA	MAX	V_{IN} = GND
I_{IH}	Input HIGH Current[3] (I/O Pins only)				15	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current[3] (I/O Pins only)				–15	µA	MAX	V_{IN} = 0.5V
I_{OS}	Output Short Circuit Current[2]		–60	–120		mA	MAX	V_{OUT} = 0.0V
C_{IN}	Input Capacitance[3]			5	10	pF		All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF		All outputs

1823 Tbl 05

Notes:

1. Typical limits are at V_{CC} = 5.0V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{os} tests should be performed last.
3. This parameter is guaranteed but not tested.

P54/74FCT853A/B (P54/74PCT853A/B)
FAST CMOS PARITY BUS TRANSCEIVER

FEATURES

- Function, Pinout, and Drive Compatible with the FCT and F Logic
- FCT-B speed at 7.0ns max. (Com'l)
  FCT-A speed at 10.0ns max. (Com'l)
- CMOS V_{OH} Levels for Low Power Consumption — Typically 1/3 of FAST Bipolar Logic
- Edge-rate Control Circuitry for Significantly Improved Noise Characteristics
- ESD protection exceeds 2000V
- Inputs and Outputs Interface Directly with TTL, NMOS, and CMOS Devices
- Outputs Meet Levels Required for CMOS Static RAM Low Power Standby Mode
- 48 mA Sink Current (Com'l), 32 mA (Mil)
  24 mA Source Current (Com'l), 15 mA (Mil)
- Buffered Direction Tri-State Output
- High Speed Bidirectional Bus Transceiver for Processor Organized Devices
- Error Flag with Open-Drain Output
- Manufactured in 0.8 micron PACE Technology™

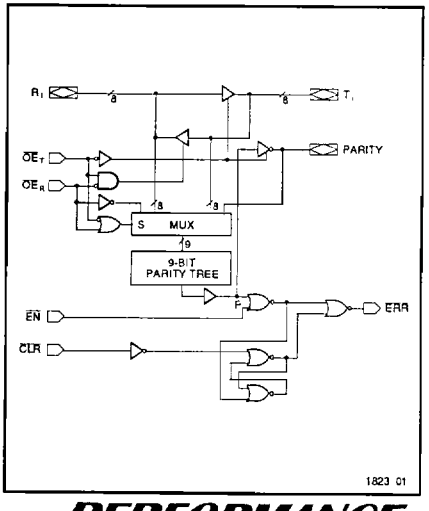
DESCRIPTION

The 'FCT853 is a high-performance bus transceivers designed for two-way communications. It contains an 8-bit data path from the R (port) to the T (port), an 8-bit data path from the T (port) to the R (port), and a 9-bit parity checker/generator. The latch configuration allows an error to be either passed, stored, sampled, or cleared at the error flag output by using the $\overline{EN}$ and $\overline{CLR}$ controls. The clear ($\overline{CLR}$) input is used to clear the error flag register. The output enable $\overline{OE}_T$ and $\overline{OE}_R$ are used to force the port outputs to the high impedance state so that the device can drive bus lines directly. In addition, $\overline{OE}_T$ and $\overline{OE}_R$ can be used to force a parity error by enabling both lines simultaneously. This transmission of inverting parity gives the designer more system diagnostic capability. The data presented at the output is non-inverted.

The 'FCT853 is manufacturered using PACE Technology which is Performance Advanced CMOS Engineered to use 0.8 micron effective channel lengths resulting in 500 picoseconds loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection and single event upset protection, and is supported by a Class 1 environment volume production facility.

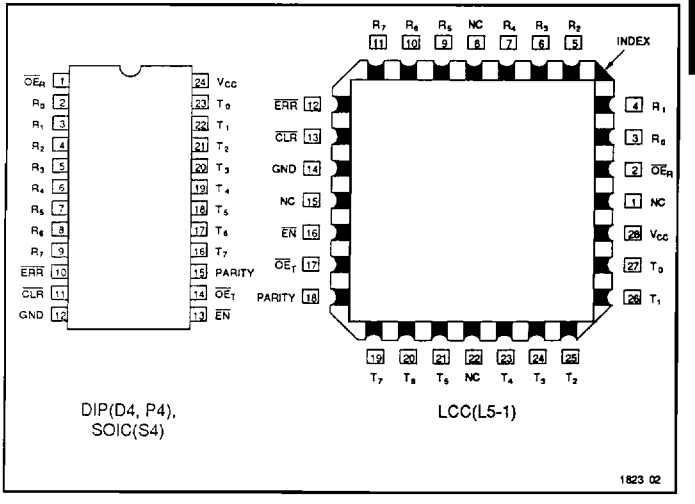
* For a fan-in/fan-out of 4 at 85°C junction temperature and 5.0 V supply. For a fan-in/fan-out of 1, the internal gate delay is 200 picoseconds at room temperature.

FUNCTIONAL BLOCK DIAGRAM



1823 01

PIN CONFIGURATIONS



DIP(D4, P4),
SOIC(S4)

LCC(L5-1)

1823 02

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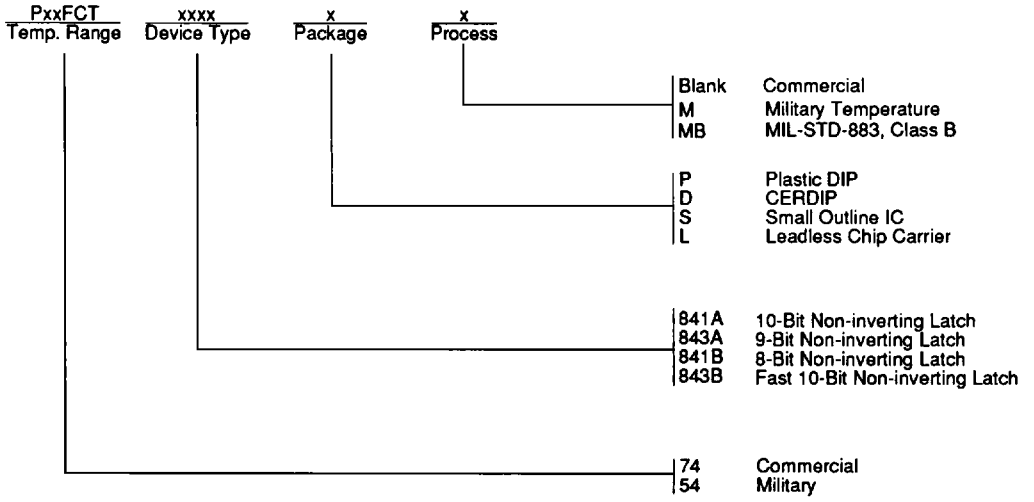
ORDERING INFORMATION



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4/22/92 - 4