HARRIS

HM-65642

8K x 8 Asynchronous CMOS Static RAM

Features

- Full CMOS Design
- Six Transistor Memory Cell
- Low Standby Supply Current 100μA
- Low Operating Supply Current 20mA
- Fast Address Access Time 150ns
- Low Data Retention Supply Voltage 2.0V
- CMOS/TTL Compatible Inputs/Outputs
- JEDEC Approved Pinout
- Equal Cycle and Access Times
- No Clocks or Strobes Required
- Gated Inputs — No Pull-Up or Pull-Down Resistors Required
- Wide Temperature Range ..... -55°C to +125°C
- Easy Microprocessor Interfacing
- Dual Chip Enable Control

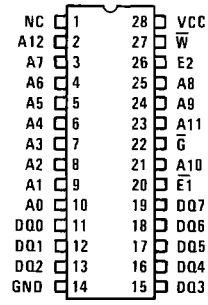
Description

The HM-65642 is a CMOS 8192 x 8 bit Static Random Access Memory. The pinout is the JEDEC 28 pin, 8 bit wide standard, which allows easy memory board layouts which accomodate a variety of industry standard ROM, PROM, EPROM, EEPROM and RAMs. The HM-65642 is ideally suited for use in microprocessor based systems. In particular, interfacing with the Harris 80C86 and 80C88 microprocessors is simplified by the convenient output enable ($\overline{G}$) input.

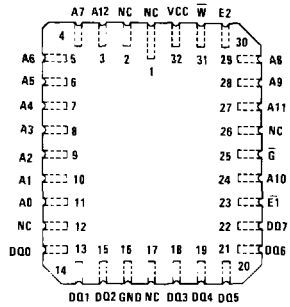
The HM-65642 is a full CMOS RAM which utilizes an array of six transistor (6T) memory cells for the most stable and lowest possible standby supply current over the full military temperature range. In addition to this, the high stability of the 6T RAM cell provides excellent protection against soft errors due to noise and alpha particles. This stability also improves the radiation tolerance of the RAM over that of four transistor or MIX-MOS (4T) devices.

Pinouts

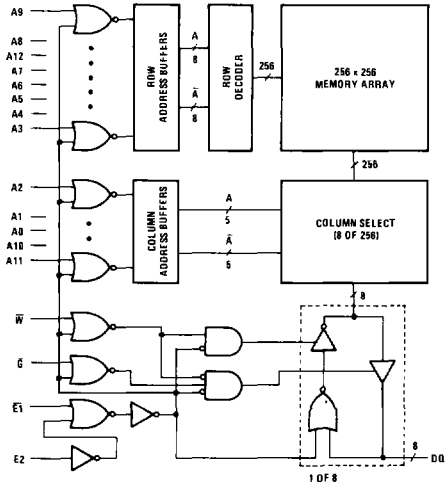
TOP VIEW



LCC
TOP VIEW



Functional Diagram



TRUTH TABLE

MODE	$\overline{E1}$	E2	$\overline{W}$	$\overline{G}$
Standby (CMOS)	X	GND	X	X
Standby (TTL)	VIH	X	X	X
	X	VIL	X	X
Enable (High Z)	VIL	VIH	VIH	VIH
Write	VIL	VIH	VIL	X
Read	VIL	VIH	VIH	VIL

PIN DESCRIPTION

PIN	DESCRIPTION
A	Address Input
DQ	Data Input/Output
$\overline{E1}$	Chip Enable
E2	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable

CAUTION These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

Absolute Maximum Ratings*

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3 to VCC +0.3V
Storage Temperature ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 8°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 45°C/W (CERDIP Package), TBD (LCC Package)
Gate Count 101000
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Input Voltage High (VIH) ..... 2.2 to VCC +0.3V
Input Voltage Low (VIL) ..... -0.3V to +0.8V
Operating Temperature Range
HM-65642B-8 ..... -55°C to +125°C
HM-65642B-9 ..... -40°C to +85°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65642B-8 -55°C to +125°C
HM-65642B-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	100	μA	E2 = GND, VCC = 5.5V
ICCSB2	Standby Supply Current (TTL)	—	5	mA	E2 = 0.8V or $\overline{E1}$ = 2.2V, VCC = 5.5V
ICCDR	Data Retention Supply Current	—	75	μA	E2 = GND, VCC = 2.0V
ICCEN	Enabled Supply Current	—	5	mA	E2 = 2.2V, $\overline{E1}$ = 0.8V, VCC = 5.5V, IIO = 0
ICCOP	Operating Supply Current (Note 3)	—	20	mA	f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V, VCC = 5.5V, IIO = 0
II	Input Leakage Current	-1.0	+1.0	μA	VIN = VCC or GND, VCC = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	μA	E2 = GND, VIO = VCC or GND, VCC = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOH1	Output High Voltage	2.4	—	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output Voltage High (Note 2)	VCC-0.4	—	V	IOH = -100μA, VCC = 4.5V
VOL	Output Low Voltage	—	0.4	V	IOL = 4.0mA, VCC = 4.5V

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	10	pF	f = 1MHz, VIN = VCC or GND
CIO	Input/Output Capacitance (Note 2)	12	pF	f = 1MHz, VIN = VCC or GND

NOTES:
1. Input pulse levels 0 to 3.0V. Input rise and fall times: 5ns (max); Input and output timing reference level 1.5V, Output load 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF
2. Tested at initial design and after major design changes
3. Typical derating 5mA/MHz increase in ICCOP
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications

V_{CC} = 5V ± 10%; T_A = HM-65642B-8 -55°C to +125°C
HM-65642B-9 -40°C to +85°C

PARAMETER		DESCRIPTION			MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1) TAVAX	tRC	Read Cycle Time			150		ns	(Note 1, 4)
(2) TAVQV	tAA	Address Access Time				150	ns	(Note 1, 4)
(3) TE1LQV	tCE1	Chip Enable Access Time		$\overline{E1}$		150	ns	(Note 1, 4)
(4) TE2HQV	tCE2	Chip Enable Access Time		E2		150	ns	(Note 1, 4)
(5) TGLQV	tOE	Output Enable Access Time				70	ns	(Note 1, 4)
(6) TE1LQX	tLZ1	Chip Enable Valid to Output On		$\overline{E1}$	10		ns	(Note 2, 4)
(7) TE2HQX	tLZ2	Chip Enable Valid to Output On		E2	10		ns	(Note 2, 4)
(8) TGLQX	tOLZ	Output Enable Valid to Output On			5		ns	(Note 2, 4)
(9) TE1HQZ	tHZ1	Chip Enable Not Valid to Output Off		$\overline{E1}$		50	ns	(Note 2, 4)
(10) TE2LQZ	tHZ2	Chip Enable Not Valid to Output Off		E2		60	ns	(Note 2, 4)
(11) TGHQZ	tOHZ	Output Enable Not Valid to Output Off				50	ns	(Note 2, 4)
(12) TAXQX	tOH	Output Hold From Address Change			10		ns	(Note 2, 4)
WRITE CYCLE								
(13) TAVAX	tWC	Write Cycle Time			150		ns	(Note 1, 4)
(14) TWLWH	tWP	Write Pulse Width			90		ns	(Note 1, 4)
(15) TE1LE1H	tCW	Chip Enable to End of Write		$\overline{E1}$	90		ns	(Note 1, 4)
(16) TE2HE2L	tCW	Chip Enable to End of Write		E2	90		ns	(Note 1, 4)
(17) TAVWL	tAS	Address Setup Time	Late Write		0		ns	(Note 1, 4)
(18) TAVE1L	tAS	Address Setup Time	Early Write,	$\overline{E1}$	0		ns	(Note 1, 4)
(19) TAVE2H	tAS	Address Setup Time	Early Write,	E2	0		ns	(Note 1, 4)
(20) TWHAX	tWR	Write Recovery Time	Late Write		10		ns	(Note 1, 4)
(21) TE1HAX	tWR	Write Recovery Time	Early Write,	$\overline{E1}$	10		ns	(Note 1, 4)
(22) TE2LAX	tWR	Write Recovery Time	Early Write,	E2	10		ns	(Note 1, 4)
(23) TDVWH	tDW	Data Setup Time	Late Write		60		ns	(Note 1, 4)
(24) TDVE1H	tDW	Data Setup Time	Early Write,	$\overline{E1}$	60		ns	(Note 1, 4)
(25) TDVE2L	tDW	Data Setup Time	Early Write,	E2	60		ns	(Note 1, 4)
(26) TWHDX	tDH	Data Hold Time	Late Write		5		ns	(Note 1, 4)
(27) TE1HDX	tDH	Data Hold Time	Early Write	$\overline{E1}$	10		ns	(Note 1, 4)
(28) TE2LDX	tDH	Data Hold Time	Early Write	E2	10		ns	(Note 1, 4)
(29) TWLQZ	tWHZ	Write Enable Low to Output Off				50	ns	(Note 2, 4)
(30) TWHQX	tOW	Write Enable High to Output On			5		ns	(Note 2, 4)

NOTES:

1. Input pulse levels 0 to 3.0V, Input rise and fall times: 5ns max. Input and output timing reference level 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3 to VCC +0.3V
Storage Temperature ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 8°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 45°C/W (CERDIP Package), TBD (LCC Package)
Gate Count 101000
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Input Voltage High (VIH) ..... 2.2 to VCC +0.3V
Input Voltage Low (VIL) ..... -0.3V to +0.8V
Operating Temperature Range
HM-65642-8 ..... -55°C to +125°C
HM-65642-9 ..... -40°C to +85°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65642-8 -55°C to +125°C
HM-65642-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	250	µA	E2 = GND, VCC = 5.5V
ICCSB2	Standby Supply Current (TTL)	—	5	mA	E2 = 0.8V or $\overline{E1}$ = 2.2V, VCC = 5.5V
ICCDR	Data Retention Supply Current	—	150	µA	E2 = GND, VCC = 2.0V
ICCEN	Enabled Supply Current	—	5	mA	E2 = 2.2V, $\overline{E1}$ = 0.8V, VCC = 5.5V, IIO = 0
ICCOP	Operating Supply Current (Note 3)	—	20	mA	f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V, VCC = 5.5V, IIO = 0
II	Input Leakage Current	-1.0	+1.0	µA	VIN = VCC or GND, VCC = 5.5V
IIOZ	Input/Output Leakage Current	-1.0	+1.0	µA	E2 = GND, VIO = VCC or GND, VCC = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOH1	Output High Voltage	2.4	—	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output Voltage High (Note 2)	VCC-0.4	—	V	IOH = -100µA, VCC = 4.5V
VOL	Output Low Voltage	—	0.4	V	IOL = 4.0mA, VCC = 4.5V

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	10	pF	f = 1MHz, VIN = VCC or GND
CIO	Input/Output Capacitance (Note 2)	12	pF	f = 1MHz, VIN = VCC or GND

NOTES:

1. Input pulse levels: 0 to 3.0V, Input rise and fall times: 5ns (max), Input and output timing reference level: 1.5V, Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

A.C. Electrical Specifications

V_{CC} = 5V ± 10%; T_A = HM-65642-8 -55°C to +125°C
HM-65642-9 -40°C to +85°C

PARAMETER		DESCRIPTION			MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1) TAVAX	tRC	Read Cycle Time			150		ns	(Note 1, 4)
(2) TAVQV	tAA	Address Access Time				150	ns	(Note 1, 4)
(3) TE1LQV	tCE1	Chip Enable Access Time		$\overline{E1}$		150	ns	(Note 1, 4)
(4) TE2HQV	tCE2	Chip Enable Access Time		E2		150	ns	(Note 1, 4)
(5) TGLQV	tOE	Output Enable Access Time				70	ns	(Note 1, 4)
(6) TE1LQX	tLZ1	Chip Enable Valid to Output On		$\overline{E1}$	10		ns	(Note 2, 4)
(7) TE2HQX	tLZ2	Chip Enable Valid to Output On		E2	10		ns	(Note 2, 4)
(8) TGLQX	tOLZ	Output Enable Valid to Output On			5		ns	(Note 2, 4)
(9) TE1HQZ	tHZ1	Chip Enable Not Valid to Output Off		$\overline{E1}$		50	ns	(Note 2, 4)
(10) TE2LQZ	tHZ2	Chip Enable Not Valid to Output Off		E2		60	ns	(Note 2, 4)
(11) TGHQZ	tOHZ	Output Enable Not Valid to Output Off				50	ns	(Note 2, 4)
(12) TAXQX	tOH	Output Hold From Address Change			10		ns	(Note 2, 4)
WRITE CYCLE								
(13) TAVAX	tWC	Write Cycle Time			150		ns	(Note 1, 4)
(14) TWLWH	tWP	Write Pulse Width			90		ns	(Note 1, 4)
(15) TE1LE1H	tCW	Chip Enable to End of Write		$\overline{E1}$	90		ns	(Note 1, 4)
(16) TE2HE2L	tCW	Chip Enable to End of Write		E2	90		ns	(Note 1, 4)
(17) TAVWL	tAS	Address Setup Time	Late Write		0		ns	(Note 1, 4)
(18) TAVE1L	tAS	Address Setup Time	Early Write,	$\overline{E1}$	0		ns	(Note 1, 4)
(19) TAVE2H	tAS	Address Setup Time	Early Write,	E2	0		ns	(Note 1, 4)
(20) TWHAX	tWR	Write Recovery Time	Late Write		10		ns	(Note 1, 4)
(21) TE1HAX	tWR	Write Recovery Time	Early Write,	$\overline{E1}$	10		ns	(Note 1, 4)
(22) TE2LAX	tWR	Write Recovery Time	Early Write,	E2	10		ns	(Note 1, 4)
(23) TDVWH	tDW	Data Setup Time	Late Write		60		ns	(Note 1, 4)
(24) TDVE1H	tDW	Data Setup Time	Early Write,	$\overline{E1}$	60		ns	(Note 1, 4)
(25) TDVE2L	tDW	Data Setup Time	Early Write,	E2	60		ns	(Note 1, 4)
(26) TWHDX	tDH	Data Hold Time	Late Write		5		ns	(Note 1, 4)
(27) TE1HDX	tDH	Data Hold Time	Early Write,	$\overline{E1}$	10		ns	(Note 1, 4)
(28) TE2LDX	tDH	Data Hold Time	Early Write,	E2	10		ns	(Note 1, 4)
(29) TWLQZ	tWHZ	Write Enable Low to Output Off				50	ns	(Note 2, 4)
(30) TWHQX	tOW	Write Enable High to Output On			5		ns	(Note 2, 4)

NOTES

1. Input pulse levels: 0 to 3.0V; Input rise and fall times: 5ns max; Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in I_{CCOP}.
4. V_{CC} = 4.5V and 5.5V.

Absolute Maximum Ratings*

Supply Voltage ..... +7.0V
Input, Output or I/O Voltage Applied ..... GND -0.3 to VCC +0.3V
Storage Temperature ..... -65°C to +150°C
Maximum Package Power Dissipation ..... 1 Watt
θ_{jc} ..... 8°C/W (CERDIP Package), TBD (LCC Package)
θ_{ja} ..... 45°C/W (CERDIP Package), TBD (LCC Package)
Gate Count 101000
Junction Temperature ..... +150°C
Lead Temperature (Soldering, Ten Seconds) ..... +275°C

CAUTION. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range ..... +4.5V to +5.5V
Input Voltage High (VIH) ..... 2.2 to VCC +0.3V
Input Voltage Low (VIL) ..... -0.3V to +0.8V
Operating Temperature Range
HM-65642C-8 ..... -55°C to +125°C
HM-65642C-9 ..... -40°C to +85°C

D.C. Electrical Specifications

VCC = 5V ± 10%; T_A = HM-65642C-8 -55°C to +125°C
HM-65642C-9 -40°C to +85°C

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
ICCSB1	Standby Supply Current (CMOS)	—	400	µA	E2 = GND, VCC = 5.5V
ICCSB2	Standby Supply Current (TTL)	—	5	mA	E2 = 0.8V or $\overline{E1}$ = 2.2V, VCC = 5.5V
ICCDR	Data Retention Supply Current	—	250	µA	E2 = GND, VCC = 2.0V
ICCEN	Enabled Supply Current	—	5	mA	E2 = 2.2V, $\overline{E1}$ = 0.8V, VCC = 5.5V, IIO = 0
ICCOP	Operating Supply Current (Note 3)	—	20	mA	f = 1MHz, $\overline{E1}$ = 0.8V, E2 = 2.2V, VCC = 5.5V, IIO = 0
II	Input Leakage Current	-2.0	+2.0	µA	VIN = VCC or GND, VCC = 5.5V
IIOZ	Input/Output Leakage Current	-2.0	+2.0	µA	E2 = GND, VIO = VCC or GND, VCC = 5.5V
VCCDR	Data Retention Supply Voltage	2.0	—	V	
VOH1	Output High Voltage	2.4	—	V	IOH = -1.0mA, VCC = 4.5V
VOH2	Output Voltage High (Note 2)	VCC-0.4	—	V	IOH = -100µA, VCC = 4.5V
VOL	Output Low Voltage	—	0.4	V	IOL = 4.0mA, VCC = 4.5V

Capacitance

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
CI	Input Capacitance (Note 2)	10	pF	f = 1MHz, VIN = VCC or GND
CIO	Input/Output Capacitance (Note 2)	12	pF	f = 1MHz, VIN = VCC or GND

NOTES:

1. Input pulse levels: 0 to 3.0V; Input rise and fall times, 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. *Tested at initial design and after major design changes.*
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V

A.C. Electrical Specifications

V_{CC} = 5V ± 10%; T_A = HM-65642C-8 -55°C to +125°C
HM-65642C-9 -40°C to +85°C

PARAMETER		DESCRIPTION			MIN	MAX	UNITS	TEST CONDITIONS
READ CYCLE								
(1) TAVAX	tRC	Read Cycle Time			200		ns	(Note 1, 4)
(2) TAVQV	tAA	Address Access Time				200	ns	(Note 1, 4)
(3) TE1LQV	tCE1	Chip Enable Access Time		$\overline{E1}$		200	ns	(Note 1, 4)
(4) TE2HQV	tCE2	Chip Enable Access Time		E2		200	ns	(Note 1, 4)
(5) TGLQV	tOE	Output Enable Access Time				70	ns	(Note 1, 4)
(6) TE1LQX	tLZ1	Chip Enable Valid to Output On		$\overline{E1}$	10		ns	(Note 2, 4)
(7) TE2HQX	tLZ2	Chip Enable Valid to Output On		E2	10		ns	(Note 2, 4)
(8) TGLQX	tOLZ	Output Enable Valid to Output On			5		ns	(Note 2, 4)
(9) TE1HQZ	tHZ1	Chip Enable Not Valid to Output Off		$\overline{E1}$		70	ns	(Note 2, 4)
(10) TE2LQZ	tHZ2	Chip Enable Not Valid to Output Off		E2		70	ns	(Note 2, 4)
(11) TGHQZ	tOHZ	Output Enable Not Valid to Output Off				60	ns	(Note 2, 4)
(12) TAXQX	tOH	Output Hold From Address Change			10		ns	(Note 2, 4)
WRITE CYCLE								
(13) TAVAX	tWC	Write Cycle Time			200		ns	(Note 1, 4)
(14) TWLWH	tWP	Write Pulse Width			120		ns	(Note 1, 4)
(15) TE1LE1H	tCW	Chip Enable to End of Write		$\overline{E1}$	120		ns	(Note 1, 4)
(16) TE2HE2L	tCW	Chip Enable to End of Write		E2	120		ns	(Note 1, 4)
(17) TAVWL	tAS	Address Setup Time	Late Write		0		ns	(Note 1, 4)
(18) TAVE1L	tAS	Address Setup Time	Early Write,	$\overline{E1}$	0		ns	(Note 1, 4)
(19) TAVE2H	tAS	Address Setup Time	Early Write,	E2	0		ns	(Note 1, 4)
(20) TWHAX	tWR	Write Recovery Time	Late Write		10		ns	(Note 1, 4)
(21) TE1HAX	tWR	Write Recovery Time	Early Write,	$\overline{E1}$	10		ns	(Note 1, 4)
(22) TE2LAX	tWR	Write Recovery Time	Early Write,	E2	10		ns	(Note 1, 4)
(23) TDVWH	tDW	Data Setup Time	Late Write		80		ns	(Note 1, 4)
(24) TDVE1H	tDW	Data Setup Time	Early Write,	$\overline{E1}$	80		ns	(Note 1, 4)
(25) TDVE2L	tDW	Data Setup Time	Early Write,	E2	80		ns	(Note 1, 4)
(26) TWHDX	tDH	Data Hold Time	Late Write		5		ns	(Note 1, 4)
(27) TE1HDX	tDH	Data Hold Time	Early Write,	$\overline{E1}$	10		ns	(Note 1, 4)
(28) TE2LDX	tDH	Data Hold Time	Early Write,	E2	10		ns	(Note 1, 4)
(29) TWLQZ	tWHZ	Write Enable Low to Output Off				70	ns	(Note 2, 4)
(30) TWHQX	tOW	Write Enable High to Output On			5		ns	(Note 2, 4)

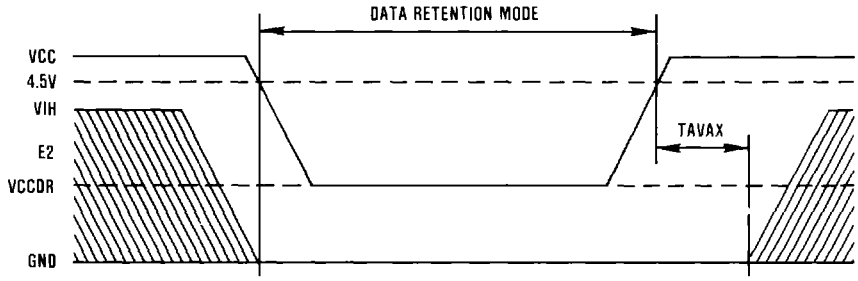
NOTES:

1. Input pulse levels 0 to 3.0V; Input rise and fall times: 5ns max; Input and output timing reference level: 1.5V, Output load: 1 TTL gate equivalent and CL = 50pF (min) — for CL greater than 50pF, access time is derated by 0.15ns per pF.
2. Tested at initial design and after major design changes.
3. Typical derating: 5mA/MHz increase in ICCOP.
4. VCC = 4.5V and 5.5V.

Low Voltage Data Retention

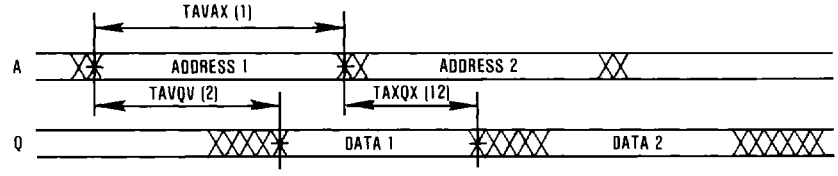
Harris CMOS RAMs are designed with battery backup in mind. Data retention voltage and supply current are guaranteed over the operating temperature range. The following rules ensure data retention:

1. The RAM must be kept disabled during data retention. This is accomplished by holding the E2 pin between -0.3V and GND.
2. During power-up and power-down transitions, E2 must be held between -0.3V and 10% of VCC.
3. The RAM can begin operating one TAVAX after VCC reaches the minimum operating voltage of 4.5V

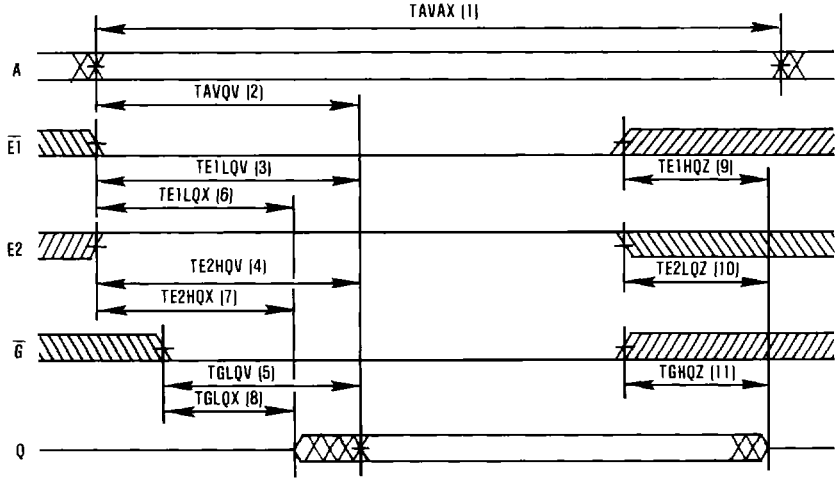


Read Cycles

READ CYCLE I: $\overline{W}$, E2 HIGH; $\overline{G}$, $\overline{E1}$ LOW

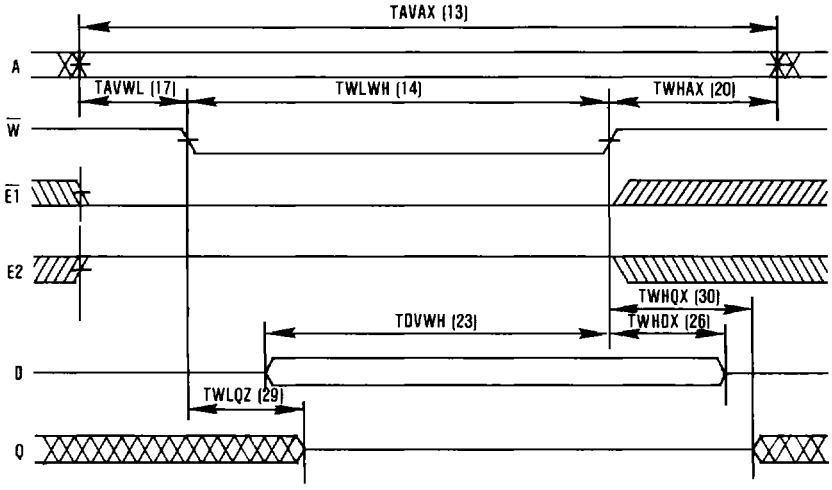


READ CYCLE II: $\overline{W}$ HIGH

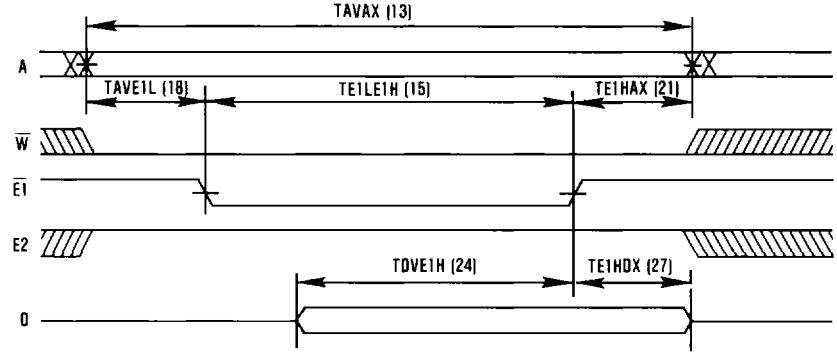


Write Cycles

WRITE CYCLE I: LATE WRITE



WRITE CYCLE II: EARLY WRITE – CONTROLLED BY $\overline{E1}$



WRITE CYCLE III: EARLY WRITE – CONTROLLED BY E2