National Semiconductor

SCAN182245A
Serially Controlled Access Network Non-Inverting Transceiver with 25Ω Series Resistor Outputs

General Description

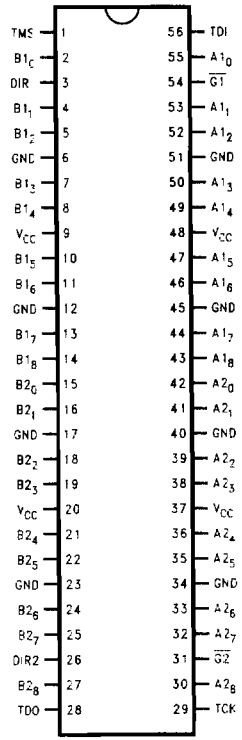
The SCAN182245A is a high performance BiCMOS bidirectional line driver featuring separate data inputs organized into dual 9-bit bytes with byte-oriented output enable and direction control signals. This device is compliant with IEEE 1149.1 Standard Test Access Port and Boundary Scan Architecture with the incorporation of the defined boundary-scan test logic and test access port consisting of Test Data Input (TDI), Test Data Out (TDO), Test Mode Select (TMS), and Test Clock (TCK).

Features

- High performance BiCMOS technology
- 25Ω series resistors in outputs eliminate the need for external terminating resistors
- Dual output enable control signals
- TRI-STATE® outputs for bus-oriented applications
- 25 mil pitch SSOP (Shrink Small Outline Package)
- IEEE 1149.1 (JTAG) Compliant
- Includes CLAMP, IDCODE and HIGHZ instructions
- Additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT
- Power Up TRI-STATE for hot insert
- Member of National's SCAN Products

Ordering Code: See Section 10

Connection Diagram



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Pin Names	Description
$A1_{(0-8)}$	Side A1 Inputs or TRI-STATE Outputs
$B1_{(0-8)}$	Side B1 Inputs or TRI-STATE Outputs
$A2_{(0-8)}$	Side A2 Inputs or TRI-STATE Outputs
$B2_{(0-8)}$	Side B2 Inputs or TRI-STATE Outputs
$\overline{G1}$, $\overline{G2}$	Output Enable Pins (Active Low)
DIR1, DIR2	Direction of Data Flow Pins

Order Number	Description
SCAN182245ASSC	SSOP in Tubes
SCAN182245ASSCX	SSOP Tape and Reel
SCAN182245AFMQB	Flatpak Military

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Truth Tables

Inputs		$A1_{(0-8)}$		$B1_{(0-8)}$
†$\overline{G1}$	DIR1			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

Inputs		$A2_{(0-8)}$		$B2_{(0-8)}$
†$\overline{G2}$	DIR2			
L	L	H	←	H
L	L	L	←	L
L	H	H	→	H
L	H	L	→	L
H	X	Z		Z

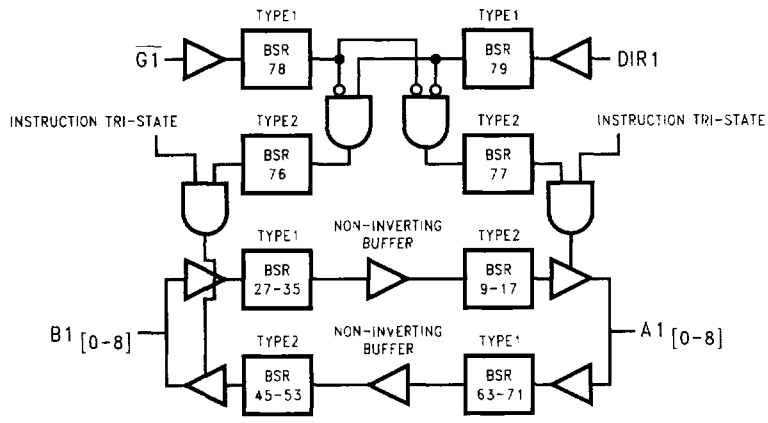
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
↑ = Inactive-to-Active transition must occur to enable outputs upon power-up.

Functional Description

The SCAN182245A consists of two sets of nine non-inverting bidirectional buffers with TRI-STATE outputs and is intended for bus-oriented applications. Direction pins (DIR1 and DIR2) LOW enables data from B ports to A ports, when HIGH enables data from A ports to B ports. The Output Enable pins ($\overline{G1}$ and $\overline{G2}$) when HIGH disables both A and B ports by placing them in a high impedance condition.

Block Diagrams

A1, B1, $\overline{G1}$ and DIR1



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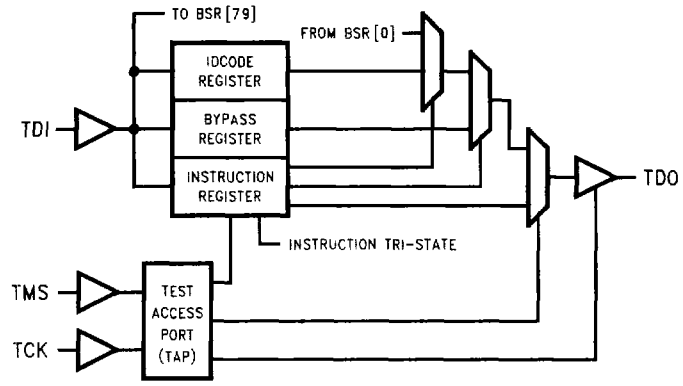
Note: BSR stands for Boundary Scan Register

Block Diagrams (Continued)

Tap Controller



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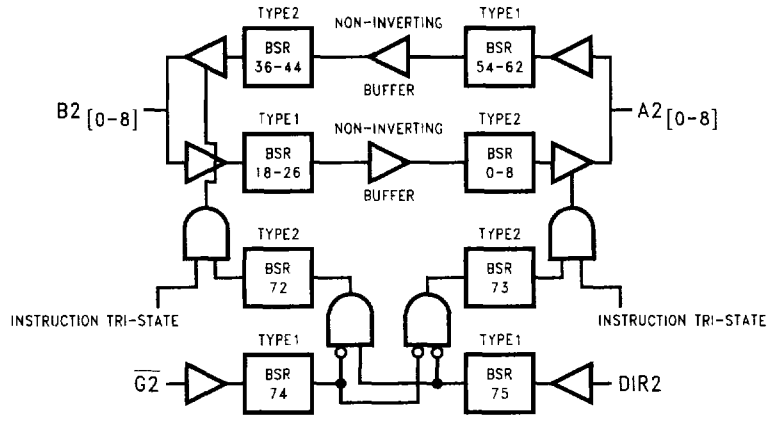
A2, B2, $\overline{G2}$ and DIR2



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Note: BSR stands for Boundary Scan Register.

SCAN-ABT Live Insertion and Power Cycling Characteristics

SCAN-ABT is intended to serve in Live Insertion backplane applications. It provides 2nd Level Isolation[1] which indicates that while external circuitry to control the output enable pin is unnecessary, there may be a need to implement differential length backplane connector pins for V_{CC} and GND. As well, pre-bias circuitry for backplane pins may be necessary to avoid capacitive loading effects during live insertion.

SCAN-ABT provides control of output enable pins during power cycling via the circuit in *Figure A*. It essentially controls the $\overline{G_n}$ pin until V_{CC} reaches a known level.

During *power-up*, when V_{CC} ramps through the 0.0V to 0.7V range, all internal device circuitry is inactive, leaving output and I/O pins of the device in high impedance. From approximately 0.8V to 1.8V V_{CC}, the Power-On-Reset circuitry, (POR), in *Figure A* becomes active and maintains device high impedance mode. The POR does this by providing a low from its output that resets the flip-flop The output, $\overline{Q}$, of the flip-flop then goes high and disables the NOR gate from an incidental low input on the $\overline{G_n}$ pin. After 1.8V V_{CC}, the POR circuitry becomes inactive and ceases to control the flip-flop. To bring the device out of high impedance, the $\overline{G_n}$ input must receive an inactive-to-active transition, a high-to-low transition on $\overline{G_n}$ in this case to change the state of the flip-flop. With a low on the $\overline{Q}$ output of the flip-flop, the NOR gate is free to allow propagation of a $\overline{G_n}$ signal.

During *power-down*, the Power-On-Reset circuitry will become active and reset the flip-flop at approximately 1.8V V_{CC}. Again, the $\overline{Q}$ output of the flip-flop returns to a high and disables the NOR gate from inputs from the $\overline{G_n}$ pin. The device will then remain in high impedance for the remaining ramp down from 1.8V to 0.0V V_{CC}.

Some suggestions to help the designer with live insertion issues:

- The $\overline{G_n}$ pin can float during power-up until the Power-On-Reset circuitry becomes inactive.
- The $\overline{G_n}$ pin can float on power-down only after the Power-On-Reset has become active.

The description of the functionality of the Power-On-Reset circuitry can best be described in the diagram of *Figure B*.

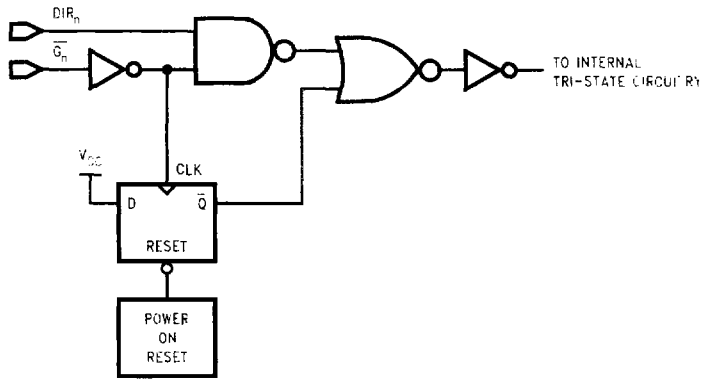

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FIGURE A

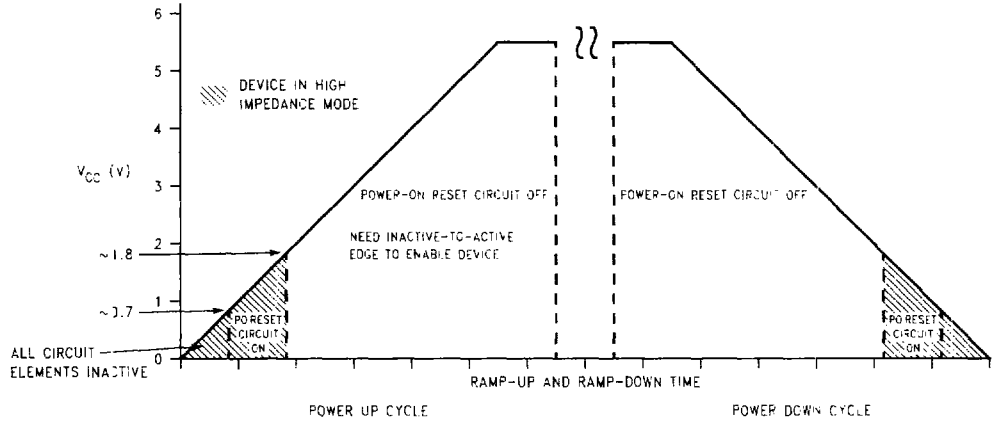

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FIGURE B

[1] *Advanced BiCMOS Logic Databook*, National Semiconductor, 1994 Edition, p. 4-3.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Storage Temperature	−65°C to +150°C
Ambient Temperature under Bias	−55°C to +125°C
Junction Temperature under Bias	
Ceramic	−55°C to +175°C
Plastic	−55°C to +150°C
V_{CC} Pin Potential to Ground Pin	−0.5V to +7.0V
Input Voltage (Note 2)	−0.5V to +7.0V
Input Current (Note 2)	−30 mA to +5.0 mA
Voltage Applied to Any Output in the Disabled or Power-Off State	−0.5V to +5.5V
in the HIGH State	−0.5V to V_{CC}
Current Applied to Output in LOW State (Max)	Twice the Rated I_{OL} (mA)
DC Latchup Source Current	
Commercial	−500 mA
Military	−300 mA
Over Voltage Latchup (I/O)	10V
ESD (HBM) Min.	2000V

Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Note 2: Either voltage limit or current limit is sufficient to protect inputs.

Recommended Operating Conditions

Free Air Ambient Temperature	
Military	−55°C to +125°C
Commercial	−40°C to +85°C
Supply Voltage	
Military	+4.5V to +5.5V
Commercial	+4.5V to +5.5V
Minimum Input Edge Rate	($\Delta V/\Delta t$)
Data Input	50 mV/ns
Enable Input	20 mV/ns

DC Electrical Characteristics

Symbol	Parameter		V_{CC}	Min	Typ	Max	Units	Conditions
V_{IH}	Input HIGH Voltage			2.0			V	Recognized HIGH Signal
V_{IL}	Input LOW Voltage					0.8	V	Recognized LOW Signal
V_{CD}	Input Clamp Diode Voltage		Min			−1.2	V	I_{IN} = −18 mA
V_{OH}	Output HIGH Voltage		Min	2.5			V	I_{OH} = −3 mA
		Mil	Min	2.0			V	I_{OH} = −24 mA
		Comm	Min	2.0			V	I_{OH} = −32 mA
V_{OL}	Output LOW Voltage							
		Mil	Min			0.8	V	I_{OL} = 12 mA
		Comm	Min			0.8	V	I_{OL} = 15 mA
I_{IH}	Input HIGH Current	All Others	Max			5	μA	V_{IN} = 2.7V (Note 1)
			Max			5	μA	V_{IN} = V_{CC}
		TMS, TDI	Max			5	μA	V_{IN} = V_{CC}
I_{BVI}	Input HIGH Current Breakdown Test		Max			7	μA	V_{IN} = 7.0V
I_{BVIT}	Input HIGH Current Breakdown Test (I/O)		Max			100	μA	V_{IN} = 5.5V
I_{IL}	Input LOW Current	All Others	Max			−5	μA	V_{IN} = 0.5V (Note 1)
			Max			−5	μA	V_{IN} = 0.0V
		TMS, TDI	Max			−385	μA	V_{IN} = 0.0V
V_{ID}	Input Leakage Test		0.0	4.75			V	I_{ID} = 1.9 μA All Other Pins Grounded
$I_{IH} + I_{OZH}$	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
$I_{IL} + I_{OZL}$	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V
I_{OZH}	Output Leakage Current		Max			50	μA	V_{OUT} = 2.7V
I_{OZL}	Output Leakage Current		Max			−50	μA	V_{OUT} = 0.5V

Note 1: Guaranteed not tested.

DC Electrical Characteristics (Continued)

Symbol	Parameter	V_{CC}	Min	Typ	Max	Units	Conditions
I_{OS}	Output Short-Circuit Current	Max	−100		−275	mA	V_{OUT} = 0.0V
I_{CEX}	Output HIGH Leakage Current	Max			50	μA	V_{OUT} = V_{CC}
I_{ZZ}	Bus Drainage Test	0.0			100	μA	V_{OUT} = 5.5V All Others GND
I_{CCH}	Power Supply Current	Max			250	μA	V_{OUT} = V_{CC}; TDI, TMS = V_{CC}
		Max			1.0	mA	V_{OUT} = V_{CC}; TDI, TMS = GND
I_{CCL}	Power Supply Current	Max			60	mA	V_{OUT} = LOW; TDI, TMS = V_{CC}
		Max			60.8	mA	V_{OUT} = LOW; TDI, TMS = GND
I_{CCZ}	Power Supply Current	Max			250	μA	TDI, TMS = V_{CC}
		Max			1.0	mA	TDI, TMS = GND
I_{CCT}	Additional I_{CC}/Input All Other Inputs	Max			2.9	mA	V_{IN} = V_{CC} − 2.1V
	TDI, TMS inputs	Max			3	mA	V_{IN} = V_{CC} − 2.1V
I_{CCD}	Dynamic I_{CC} No Load	Max			0.2	mA/ MHz	Outputs Open One Bit Toggling, 50% Duty Cycle

AC Electrical Characteristics Normal Operation

Symbol	Parameter	V_{CC}* (V)	Military T_A = −55°C to +125°C C_L = 50 pF			Commercial T_A = −40°C to +85°C C_L = 50 pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay A to B, B to A	5.0				1.0 1.5	3.1 4.4	5.2 6.5	ns	1, 2
t_{PLZ} t_{PHZ}	Disable Time	5.0				1.5 1.5	4.8 5.2	8.6 8.9	ns	3, 4
t_{PZL} t_{PZH}	Enable Time	5.0				1.5 1.5	5.5 4.6	9.1 8.2	ns	3, 4

*Voltage Range 5.0V ±0.5V

AC Electrical Characteristics Scan Test Operation

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF			Commercial $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF			Units	Fig. No.
			Min	Typ	Max	Min	Typ	Max		
t_{PLH} t_{PHL}	Propagation Delay TCK to TDO	5.0				2.9 4.2	6.1 7.7	10.2 12.1	ns	5
t_{PLZ} t_{PHZ}	Disable Time TCK to TDO	5.0				2.1 3.3	5.9 7.4	10.7 12.5	ns	6, 7
t_{PZL} t_{PZH}	Enable Time TCK to TDO	5.0				4.6 2.8	8.7 6.8	13.7 11.5	ns	6, 7
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-DR State	5.0				2.8 4.5	6.3 8.2	10.7 13.0	ns	5
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Update-IR State	5.0				3.3 5.0	7.2 9.3	12.2 14.8	ns	5
t_{PLH} t_{PHL}	Propagation Delay TCK to Data Out during Test Logic Reset State	5.0				3.7 5.7	8.4 10.8	14.0 17.2	ns	5
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-DR State	5.0				2.8 3.5	7.6 8.4	13.9 14.5	ns	6, 7
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Update-IR State	5.0				3.6 3.8	8.7 9.2	15.1 15.9	ns	6, 7
t_{PLZ} t_{PHZ}	Disable Time TCK to Data Out during Test Logic Reset State	5.0				4.0 4.2	9.8 9.9	17.1 16.6	ns	6, 7
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-DR State	5.0				4.4 3.0	9.3 7.5	15.5 13.3	ns	6, 7
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Update-IR State	5.0				5.2 3.9	10.7 9.0	17.4 15.4	ns	6, 7
t_{PZL} t_{PZH}	Enable Time TCK to Data Out during Test Logic Reset State	5.0				5.7 3.0	12.0 10.2	19.8 17.6	ns	6, 7

*Voltage Range 5.0V ±0.5V

All Propagation Delays involving TCK are measured from the falling edge of TCK.

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AC Operating Requirements Scan Test Operation

Symbol	Parameter	V_{CC}* (V)	Military $T_A = -55°C$ to $+125°C$ $C_L = 50$ pF	Commercial $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF	Units	Fig. No.
			Guaranteed Minimum			
t_S	Setup Time Data to TCK (Note 1)	5.0		4.8	ns	9
t_H	Hold Time Data to TCK (Note 1)	5.0		2.5	ns	9
t_S	Setup Time, H or L $\overline{G1}$, $\overline{G2}$ to TCK (Note 2)	5.0		4.1	ns	9
t_H	Hold Time, H or L TCK to $\overline{G1}$, $\overline{G2}$ (Note 2)	5.0		1.7	ns	9
t_S	Setup Time, H or L DIR1, DIR2 to TCK (Note 4)	5.0		4.2	ns	9
t_H	Hold Time, H or L TCK to DIR1, DIR2 (Note 4)	5.0		2.3	ns	9
t_S	Setup Time Internal OE to TCK (Note 3)	5.0		3.8	ns	9
t_H	Hold Time, H or L TCK to Internal OE (Note 3)	5.0		2.3	ns	9
t_S	Setup Time, H or L TMS to TCK	5.0		8.7	ns	9
t_H	Hold Time, H or L TCK to TMS	5.0		1.5	ns	9
t_S	Setup Time, H or L TDI to TCK	5.0		6.7	ns	9
t_H	Hold Time, H or L TCK to TDI	5.0		5.0	ns	9
t_W	Pulse Width TCK H L	5.0		10.2 8.5	ns	10
f_{max}	Maximum TCK Clock Frequency	5.0		50	MHz	
t_{PU}	Wait Time, Power Up to TCK	5.0		100	ns	
t_{DN}	Power Down Delay	0.0		100	ms	

*Voltage Range 5.0V ±0.5V

All Input Timing Delays involving TCK are measured from the rising edge of TCK.

Note 1: Timing pertains to the TYPE1 BSR and TYPE2 BSR after the buffer (BSR 0–8, 9–17, 18–26, 27–35, 36–44, 45–53, 54–62, 63–71).

Note 2: Timing pertains to BSR 74 and 78 only.

Note 3: Timing pertains to BSR 72, 73, 76 and 77 only.

Note 4: Timing pertains to BSR 75 and 79 only.

Capacitance

Symbol	Parameter	Typ	Units	Conditions, $T_A = 25°C$
C_{IN}	Input Capacitance	5.9	pF	$V_{CC} = 0.0V$ ($\overline{G}_n$, DIR_n)
$C_{I/O}$ (Note 1)	Output Capacitance	13.7	pF	$V_{CC} = 5.0V$ (A_n, B_n)

Note 1: $C_{I/O}$ is measured at frequency f = 1 MHz, per MIL-STD-883B, Method 3012.

Waveforms

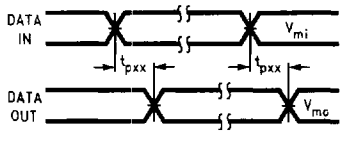

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FIGURE 1. Waveform for Inverting and Non-Inverting Functions

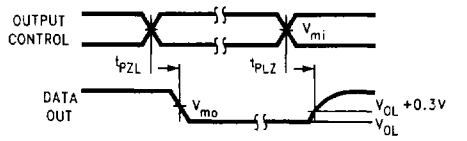

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FIGURE 4. TRI-STATE Output Low Enable and Disable Times

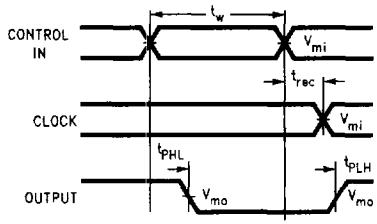

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FIGURE 2. Propagation Delay, Pulse Width and t_{rec} Waveforms

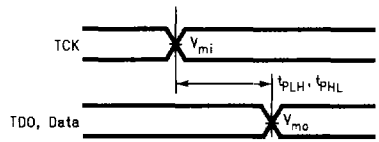

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FIGURE 5. Propagation Delay

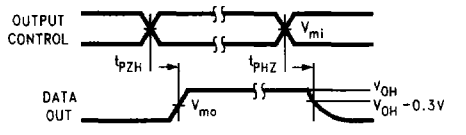

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FIGURE 3. TRI-STATE Output High Enable and Disable Times

V_{mi} = 1.5V

V_{mo} = 1.5V

Note: Input pulses have the following characteristics: f = 1 MHz, t_r = 2.5 ns, t_f = 2.5 ns, amplitude = 3.0V.

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Waveforms (Continued)

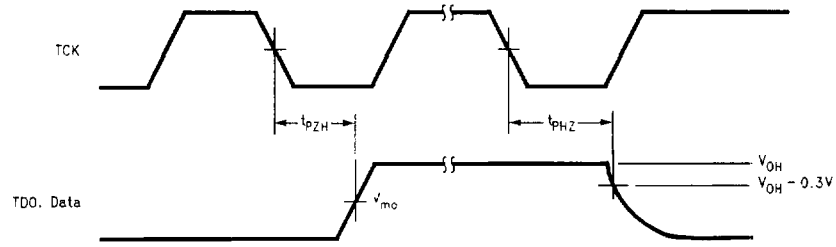

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FIGURE 6. TRI-STATE Output High Enable and Disable Times

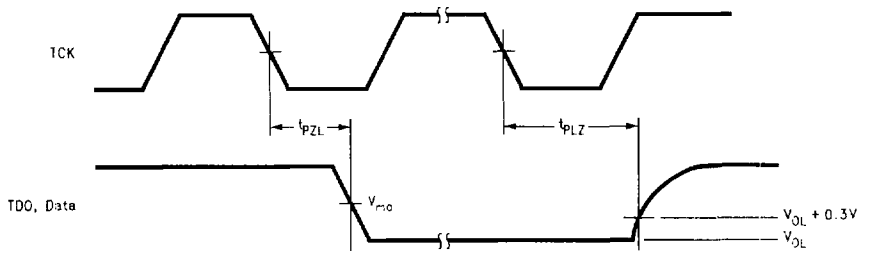

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FIGURE 7. TRI-STATE Output Low Enable and Disable Times

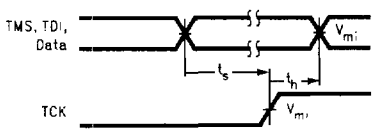

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FIGURE 8. Setup Time, Hold Time and Recovery Time

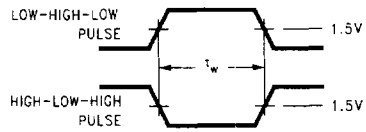

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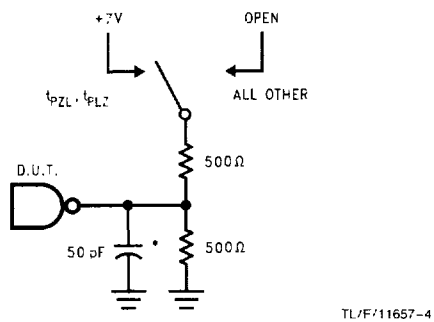
FIGURE 9. Pulse Width

V_{mi} = 1.5V
V_{mo} = 1.5V



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*Includes jig and probe capacitance

FIGURE 10. Standard AC Test Load

Note: Input pulses have the following characteristics: f = 1 MHz, t_r = 2.5 ns, t_f = 2.5 ns, amplitude = 3.0V.

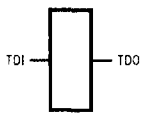
Description of BOUNDARY-SCAN Circuitry

The scan cells used in the BOUNDARY-SCAN register are one of the following two types depending upon their location. Scan cell TYPE1 is intended to solely observe system data, while TYPE2 has the additional ability to control system data. (See IEEE Standard 1149.1 *Figure 10–11* for a further description of scan cell TYPE1 and *Figure 10–12* for a further description of scan cell TYPE2.)

Scan cell TYPE1 is located on each system input pin while scan cell TYPE2 is located at each system output pin as well as at each of the two internal active-high output enable signals. AOE controls the activity of the A-outputs while BOE controls the activity of the B-outputs. Each will activate their respective outputs by loading a logic high.

The BYPASS register is a single bit shift register stage identical to scan cell TYPE1. It captures a fixed logic low.

Bypass Register Scan Chain Definition
Logic 0



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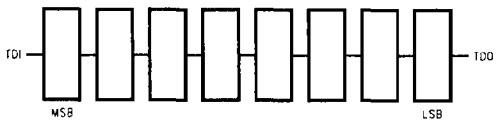
SCAN182245A Product IDCODE
(32-Bit Code per IEEE 1149.1)

Version	Entity	Part Number	Manufacturer ID	Required by 1149.1
0000	111111	0000000000	00000001111	1

MSB **LSB**

The INSTRUCTION register is an 8-bit register which captures the default value of 10000001 (SAMPLE/PRELOAD) during the CAPTURE-IR instruction command. The benefit of capturing SAMPLE/PRELOAD as the default instruction during CAPTURE-IR is that the user is no longer required to shift in the 8-bit instruction for SAMPLE/PRELOAD. The sequence of: CAPTURE-IR → EXIT1-IR → UPDATE-IR will update the SAMPLE/PRELOAD instruction. For more information refer to the section on instruction definitions.

Instruction Register Scan Chain Definition



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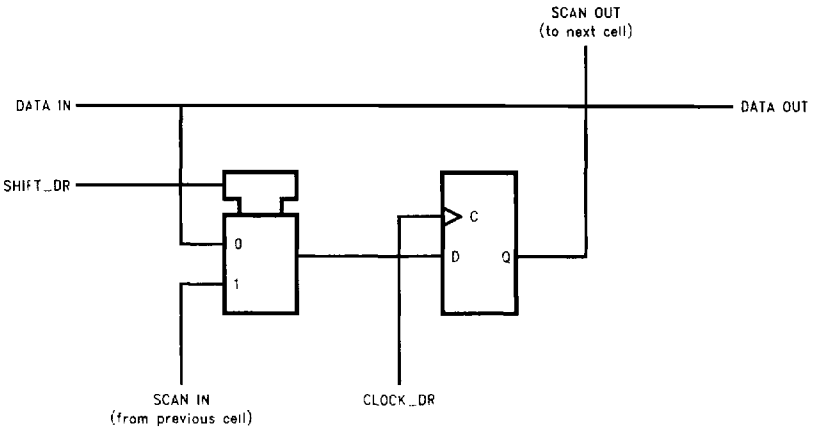
MSB → LSB

Instruction Code	Instruction
00000000	EXTEST
10000001	SAMPLE/PRELOAD
10000010	CLAMP
00000011	HIGHZ
01000001	SAMPLE-IN
01000010	SAMPLE-OUT
00100010	EXTEST-OUT
10101010	IDCODE
11111111	BYPASS
All Others	BYPASS

Description of BOUNDARY-SCAN Circuitry (Continued)

Scan Cell TYPE1



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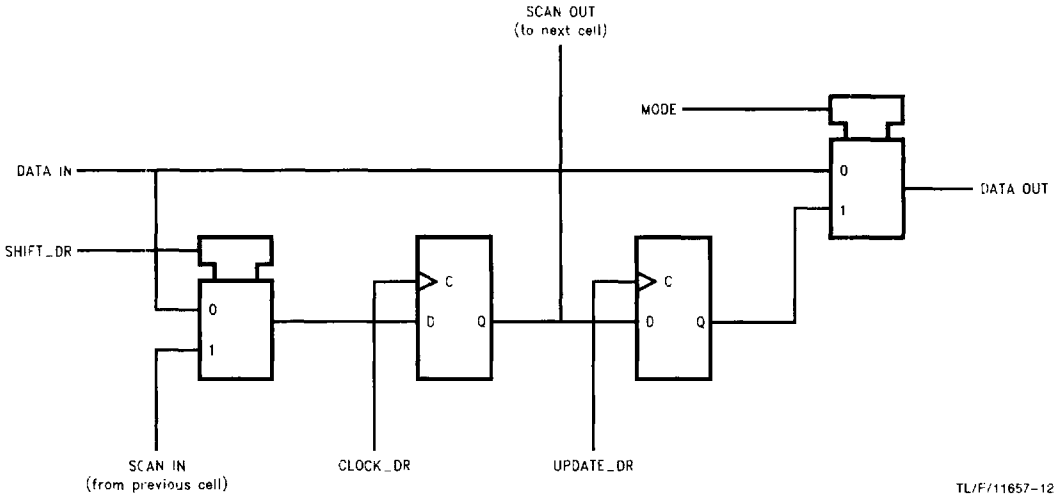
Scan Cell TYPE2



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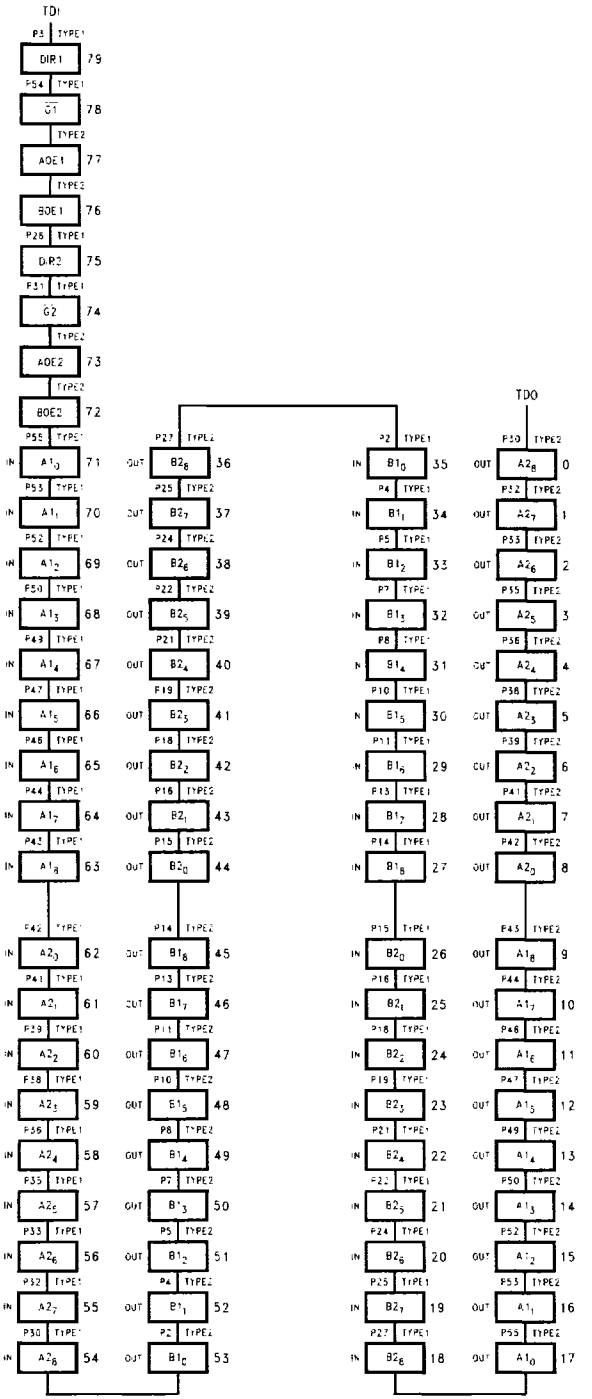
Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register
SCAN182245 Scan Chain Definition (80 Bits in Length)



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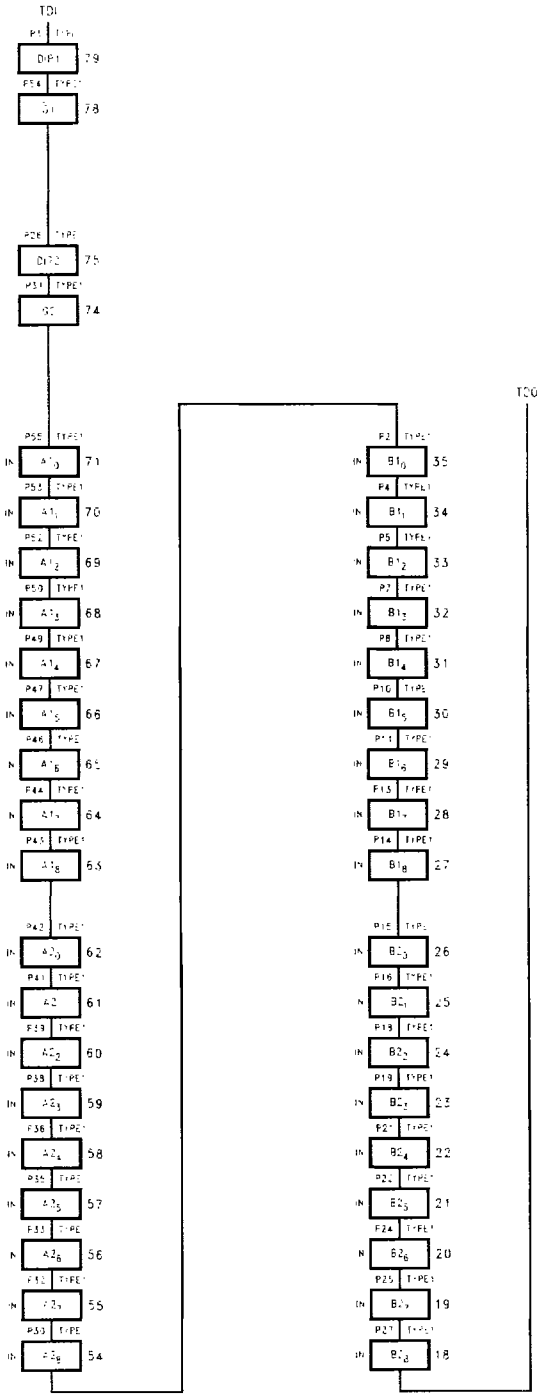
Description of BOUNDARY-SCAN Circuitry (Continued)

Input BOUNDARY-SCAN Register
SCAN182245 Scan Chain Definition (40 Bits in Length)



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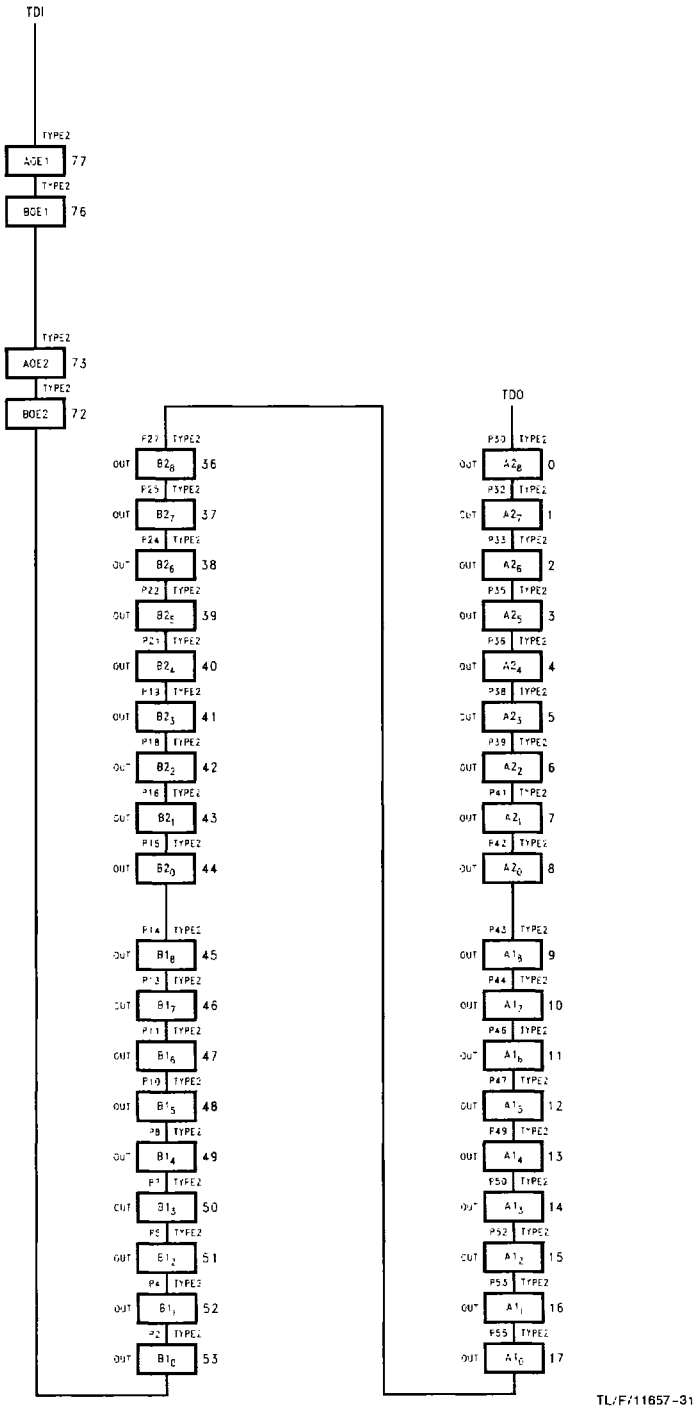
Description of BOUNDARY-SCAN Circuitry (Continued)

Output BOUNDARY-SCAN Register
SCAN182245 Scan Chain Definition (40 Bits in Length)



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Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
79	DIR1	3	Input	TYPE1	
78	$\overline{G1}$	54	Input	TYPE1	
77	AOE_1		Internal	TYPE2	
76	BOE_1		Internal	TYPE2	Control
75	DIR2	26	Input	TYPE1	Signals
74	$\overline{G2}$	31	Input	TYPE1	
73	AOE_2		Internal	TYPE2	
72	BOE_2		Internal	TYPE2	
71	$A1_0$	55	Input	TYPE1	
70	$A1_1$	53	Input	TYPE1	
69	$A1_2$	52	Input	TYPE1	
68	$A1_3$	50	Input	TYPE1	
67	$A1_4$	49	Input	TYPE1	A1–in
66	$A1_5$	47	Input	TYPE1	
65	$A1_6$	46	Input	TYPE1	
64	$A1_7$	44	Input	TYPE1	
63	$A1_8$	43	Input	TYPE1	
62	$A2_0$	42	Input	TYPE1	
61	$A2_1$	41	Input	TYPE1	
60	$A2_2$	39	Input	TYPE1	
59	$A2_3$	38	Input	TYPE1	
58	$A2_4$	36	Input	TYPE1	A2–in
57	$A2_5$	35	Input	TYPE1	
56	$A2_6$	33	Input	TYPE1	
55	$A2_7$	32	Input	TYPE1	
54	$A2_8$	30	Input	TYPE1	
53	$B1_0$	2	Output	TYPE2	
52	$B1_1$	4	Output	TYPE2	
51	$B1_2$	5	Output	TYPE2	
50	$B1_3$	7	Output	TYPE2	
49	$B1_4$	8	Output	TYPE2	B1–out
48	$B1_5$	10	Output	TYPE2	
47	$B1_6$	11	Output	TYPE2	
46	$B1_7$	13	Output	TYPE2	
45	$B1_8$	14	Output	TYPE2	
44	$B2_0$	15	Output	TYPE2	
43	$B2_1$	16	Output	TYPE2	
42	$B2_2$	18	Output	TYPE2	
41	$B2_3$	19	Output	TYPE2	
40	$B2_4$	21	Output	TYPE2	B2–out
39	$B2_5$	22	Output	TYPE2	
38	$B2_6$	24	Output	TYPE2	
37	$B2_7$	25	Output	TYPE2	
36	$B2_8$	27	Output	TYPE2	
35	$B1_0$	2	Input	TYPE1	
34	$B1_1$	4	Input	TYPE1	
33	$B1_2$	5	Input	TYPE1	
32	$B1_3$	7	Input	TYPE1	
31	$B1_4$	8	Input	TYPE1	B1–in
30	$B1_5$	10	Input	TYPE1	
29	$B1_6$	11	Input	TYPE1	
28	$B1_7$	13	Input	TYPE1	
27	$B1_8$	14	Input	TYPE1	

Description of BOUNDARY-SCAN Circuitry (Continued)

BOUNDARY-SCAN Register Definition Index (Continued)

Bit No.	Pin Name	Pin No.	Pin Type	Scan Cell Type	
26	$B2_0$	15	Input	TYPE1	
25	$B2_1$	16	Input	TYPE1	
24	$B2_2$	18	Input	TYPE1	
23	$B2_3$	19	Input	TYPE1	
22	$B2_4$	21	Input	TYPE1	B2-in
21	$B2_5$	22	Input	TYPE1	
20	$B2_6$	24	Input	TYPE1	
19	$B2_7$	25	Input	TYPE1	
18	$B2_8$	27	Input	TYPE1	
17	$A1_0$	55	Output	TYPE2	
16	$A1_1$	53	Output	TYPE2	
15	$A1_2$	52	Output	TYPE2	
14	$A1_3$	50	Output	TYPE2	
13	$A1_4$	49	Output	TYPE2	A1-out
12	$A1_5$	47	Output	TYPE2	
11	$A1_6$	46	Output	TYPE2	
10	$A1_7$	44	Output	TYPE2	
9	$A1_8$	43	Output	TYPE2	
8	$A2_0$	42	Output	TYPE2	
7	$A2_1$	41	Output	TYPE2	
6	$A2_2$	39	Output	TYPE2	
5	$A2_3$	38	Output	TYPE2	
4	$A2_4$	36	Output	TYPE2	A2-out
3	$A2_5$	35	Output	TYPE2	
2	$A2_6$	33	Output	TYPE2	
1	$A2_7$	32	Output	TYPE2	
0	$A2_8$	30	Output	TYPE2	

Description of BOUNDARY-SCAN Circuitry (Continued)

TEST ACCESS PORT (TAP)

The Test Access Port (TAP) consists of four pins dedicated solely to the operation of the test logic. The four pins include TMS (Test Mode Select), TDI (Test Data In), TDO (Test Data Out), and TCK (Test Clock). These products contain a power-up reset function in lieu of adding the $\overline{TRST}$ pin. The motivation of this option is to save package size and hence customer board space, thus making the decision to implement 1149.1 less costly to the system designer.

TCK: This input provides the test clock for the test logic defined by the IEEE 1149.1 Standard. In accordance with the standard requirements, all test logic will retain its state indefinitely upon stopping TCK at a logic low, or 0. Additionally, the same retention may occur upon stopping TCK at a logic high, or 1, which is a permission granted by the standard. The motivation for TCK to be a dedicated test input is 1) to insure that it can be used independently of system clocks running at different frequencies, 2) that it permits shifting of test data without altering any system logic state when undertaking on-line system monitoring tasks, and 3) that it can be used to test all board interconnect even when that interconnect transfers clock signals from one device to another.

TMS: This input is the command signal to control system operation modes. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. The requirement that an unforced TMS input produce a logic high is to ensure that the normal operation of the design can continue without interference from the test logic by guaranteeing that an undriven TMS input can put the TAP Controller into the Test Logic Reset state.

TDI: This signal provides the serial data input of test instructions and data to the test logic. Its value is accepted into the test logic upon the rising edge of TCK. This input has a pull-up resistor to implement a logic high for an undriven input. Test data will arrive at TDO without inversion after the appropriate number of clock cycles as determined by the length of the register currently connected between TDI and TDO. The requirement that an unforced TDI input produce a logic high is to assist in the determination of manufacturing defects in the test scan chain interconnect. A consistent field of 1's in shifting out the data registers can indicate where a break in the scan chain interconnect occurred.

TDO: This signal provides the serial data output of test instructions and data from the test logic. Changes in the logic state and drive activity for this output occur upon the falling edge of TCK. This is to avoid a race condition when TDO is connected to TDI of the next chip in the scan chain which is sampled on the rising edge. This output shall remain inactive except when the scanning of data is in progress. This is to permit the ability to multiplex scan chains on the board without causing signal contention between multiple TDO outputs connected together to form parallel scan chains.

TAP STATE DESCRIPTIONS

Changes in the state of the TAP Controller are solely a response to the value of TMS upon the rising edge of TCK, or upon power-up (or the application of a logic low to the optional $\overline{TRST}$ input which is not included in the products referring to this document). In any given state actions of the test logic taken in that state occur on the falling or rising edge of TCK following the rising edge of TCK which caused the TAP Controller to enter the state initially.

Note: It may happen that actions to occur in one state happen on the same rising edge of TCK that cause the TAP Controller to enter the next state.

Test Logic Reset: The test logic is disabled during this state such that normal operation of the system logic may proceed uninhibited.

Two features of the state diagram are realized in this state. First it can be noted that independent of what state the TAP Controller is currently in, it will enter the Test Logic Reset state after, at most, five clock cycles of TCK with the TMS input high. Secondly, if a temporary glitch should occur on the TMS input during a rising edge of TCK, the TAP Controller will enter the Run-Test/Idle state then return to the Test Logic Reset state via the Select-DR state and Select-IR state provided that TMS returns to its logic high value for rising edge clocks following the glitch. The TAP Controller will also be forced into the Test Logic Reset state upon a low assertion of the $\overline{TRST}$ pin or, in the case of the products referencing this article, upon power-up.

Run-Test/Idle: In this state activity in the test logic occurs according to the instruction present. None of the mandatory instructions undertake any test logic activity during this state. During the description above regarding recovery from a glitch on the TMS input the current instruction is the BYPASS instruction and as a result no activity occurs in this state with that instruction present. This state is designed to provide the capability of performing built-in test functions during optional instructions. For instructions that do not activate test logic during this state, all test data registers retain their current state, i.e., remain idle.

SELECT-DR Scan: This is a temporary state in which all test data registers retain their previous values.

Capture-DR: In this controller state data may be parallel loaded into the data register selected by the current instruction; otherwise, it retains its previous values.

SHIFT-DR: In this state the test data register selected between TDI and TDO by the current instruction will shift one stage at each rising edge of TCK. TDO is active during this state. Test data registers not selected by the current instruction maintain their previous values.

Exit1-DR: This is a temporary state in which all test data registers retain their previous values.

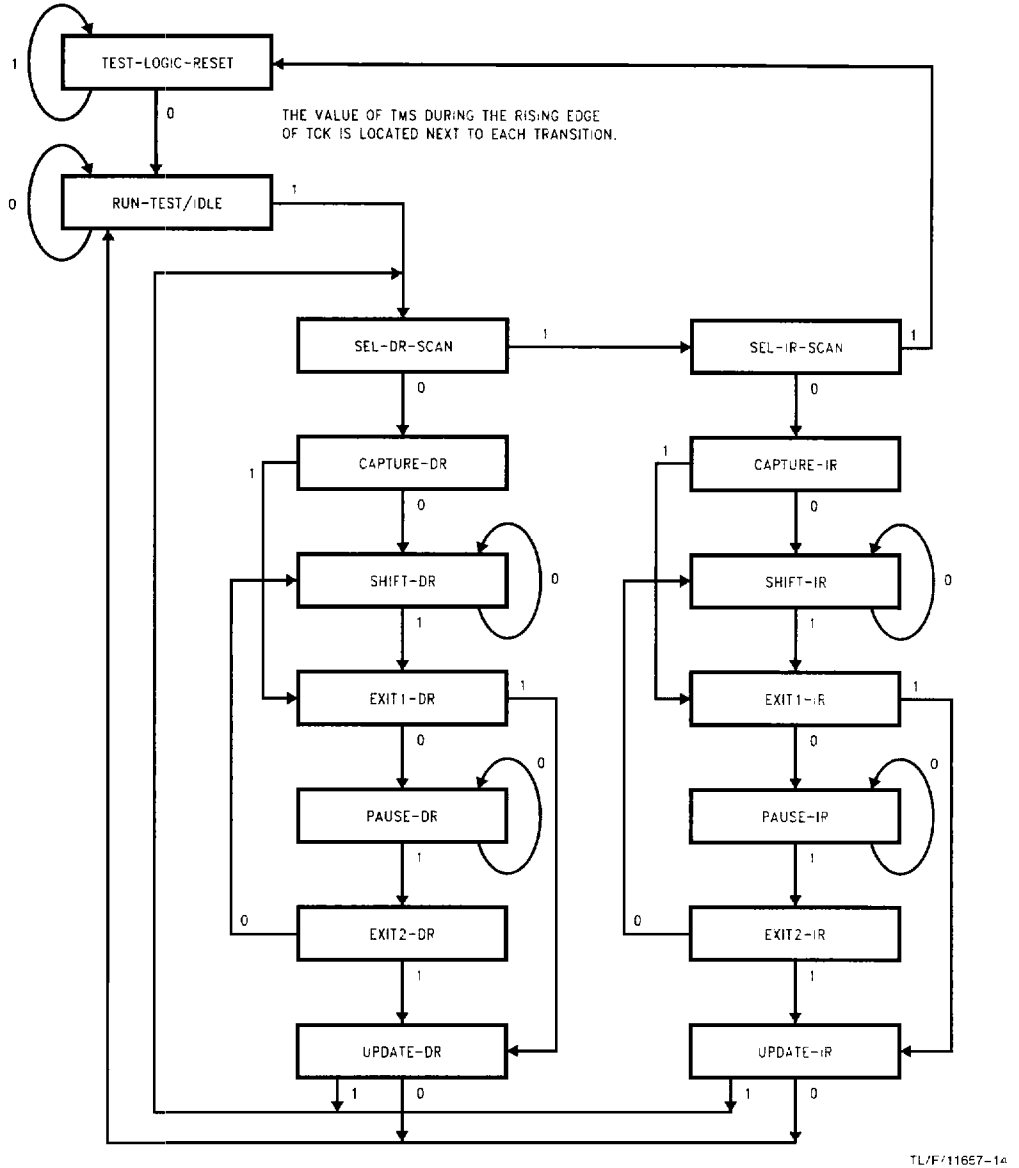
PAUSE-DR: This is a temporary state in which all data registers retain their previous values. This state is intended to temporarily halt the shifting of test data into the data register selected while retaining the ability to keep TCK running; TCK may be a free-running clock.

Exit2-DR: This is a temporary state in which all test data registers retain their previous values.

UPDATE-DR: The parallel output register of the selected test data register may be updated on the falling edge of TCK in this state, provided the test data register has such a parallel output register. The intent of the parallel output register is to provide the ability to apply the contents of the test data registers to the test logic simultaneously rather than applying it as it is being shifted in. All test data registers not selected by the current instruction retain their previous values.

Description of BOUNDARY-SCAN Circuitry (Continued)

TAP Controller State Diagram



Description of BOUNDARY-SCAN Circuitry (Continued)

SELECT-IR Scan: This is a temporary state in which the INSTRUCTION register retains its previous value.

Capture-IR: In this controller state data must be parallel loaded into the INSTRUCTION register. The only restriction on what that data may be is that its least significant bit must be a logic high, or 1, and its second least significant bit must be a logic low, or 0. These opposite state bits can be used to check the correct operation of the scan chain on the board by forcing a bit toggle when the instructions are shifted.

SHIFT-IR: In this state the INSTRUCTION register selected between TDI and TDO will shift one stage at each rising edge of TCK. TDO is active during this state.

Exit1-IR: This is a temporary state in which the INSTRUCTION register retains its previous value.

PAUSE-IR: This is a temporary state in which the INSTRUCTION register retains its previous value. This state is intended to temporarily halt the shifting of test data into the INSTRUCTION register while retaining the ability to keep TCK running.

Exit2-IR: This is a temporary state in which the INSTRUCTION register retains its previous value.

UPDATE-IR: The parallel output register of the INSTRUCTION register will be updated on the falling edge of TCK in this state. The intent of the parallel output register is to provide the ability to apply the contents of the INSTRUCTION register to the test logic simultaneously rather than applying it as it is being shifted in.

TDO OUTPUT ACTIVITY

Control of the TDO output buffer follows the table outlined below:

Controller State	Register Selected between TDI and TDO	TDO Driver
Test Logic Reset	BYPASS	Inactive
Run Test/Idle	BYPASS	Inactive
SELECT-DR Scan	**	Inactive
SELECT-IR Scan	INSTRUCTION	Inactive
Capture-IR	INSTRUCTION	Inactive
SHIFT-IR	INSTRUCTION	ACTIVE
Exit1-IR	INSTRUCTION	Inactive
PAUSE-IR	INSTRUCTION	Inactive
Exit2-IR	INSTRUCTION	Inactive
UPDATE-IR	INSTRUCTION	Inactive
Capture-DR	**	Inactive
SHIFT-DR	TEST DATA	ACTIVE
Exit1-DR	**	Inactive
PAUSE-DR	**	Inactive
Exit2-DR	**	Inactive
UPDATE-DR	**	Inactive

Note: ** = Data register selected depends on currently active instruction.

FEATURES OF THE TAP CONTROLLER

The TAP Controller will not be initialized by the operation of any system pin such as a system reset. The TAP Controller will be initialized into the Test Logic Reset state upon power-up. This requirement is intended to avoid bus signal contention upon system power-up by disabling the test logic which allows the system logic to operate normally and hence be controlled to avoid any contention. (The TAP Controller will return to the Test Logic Reset state after, at most, five clock cycles of TCK with TMS high; but the time required to enact that operation may not be sufficient to avoid contention.)

Note that the TAP Controller has been defined such that six of the sixteen states have the ability to maintain their state provided that TMS remains at the same value it had when entering the state. Those states include Test Logic Reset to hold off the test logic during normal system operation, Run Test/Idle to undertake multi-cycle self tests, SHIFT-DR and SHIFT-IR to maintain the data shifting process for an extended period, and PAUSE-DR and PAUSE-IR to halt the shifting process while some other activity is performed such as retrieving test data from additional memory. This feature is available in any/all states where multiple clock cycles may be required to achieve the desired outcome or where activity is to be halted but still provide the ability to make TCK a free-running clock.

INSTRUCTION REGISTER

The INSTRUCTION register permits specific commands to be shifted into the design to select a particular test data register and/or a specific test function. Additionally, the capture sequence of the INSTRUCTION register permits design specific data to be examined.

The INSTRUCTION register must be at least two bits long, the specific INSTRUCTION register included into the devices which reference this document is eight bits long, and the two least significant bits must capture the value "01". The significance of the two bit minimum length is two fold. First it permits the ability to supply unique codes for at least each of the three mandatory instructions required by the standard. Secondly, the bit value "01" in the least significant locations can be used to check the connectivity of the scan chain by forcing a bit toggle at each instruction during a scan of the INSTRUCTION registers. This technique not only assists in determining the correct connectivity of the scan chain about the board, but also assists in pin-pointing the location of any break in the scan chain.

The six most significant bits will contain device specific codes which can be used to differentiate them from each other when being interrogated through the boundary-scan ring. On these products the DEVICE IDENTIFICATION register was not incorporated in order to minimize any cost and/or performance impact to the customer. As a result of that decision the operation of the test logic may be precisely identical in several of the functions. The different codes captured into the INSTRUCTION register is a means of distinguishing the products in order to supply a method of evaluating the correct board placement of the products when an interrogation is performed through the scan chain only.

The order of scan through the INSTRUCTION register must be least-to-most; that is, the least significant bit is closest to TDO for a loaded instruction. During the SHIFT-IR state the instruction shifts one bit between TDI and TDO upon each rising edge of TCK and appears without inversion at TDO following the appropriate number of TCK cycles depending on the fixed length of the INSTRUCTION register. A latched parallel output register accompanies each bit of the INSTRUCTION register such that the instruction can be updated or applied to the test logic simultaneously, rather than during the shift sequence. This latched parallel output

Description of BOUNDARY-SCAN Circuitry (Continued)

changes upon the falling edge of TCK in the Update-IR state as well as upon the falling edge of TCK during the Test Logic Reset state. (It changes asynchronously upon the low assertion of the $\overline{TRST}$ input or upon power-up.)

Each instruction will identify a particular test data register to be connected between TDI and TDO when in the Shift-DR state along with defining any particular test actions to occur to that test data register and/or any others.

INSTRUCTION DEFINITIONS

The required instructions include the BYPASS, EXTEST, and SAMPLE/PRELOAD instructions. The optional instructions of HIGHZ, CLAMP and IDCODE, as well as the additional instructions SAMPLE-IN, SAMPLE-OUT and EXTEST-OUT have also been incorporated into the specific devices which reference this document. The optional INTEST instruction was not incorporated due to the additional propagation delay penalty to the system logic which would result from gating that logic in order to provide controllability as well as observability. In the following descriptions each instruction will identify the test data register to be connected between TDI and TDO during the SHIFT-DR state, any restrictions on the binary codes used to implement the instruction, and what test data registers are used in undertaking the actions of the instruction.

1. **EXTEST.** This instruction allows circuitry external to the component package, typically the board interconnect, to be tested. BOUNDARY-SCAN register cells at the output pins are used to apply test stimuli, while those at the input pins capture test results. When this instruction is selected, the states of all signals on the system input pins will be loaded into the BOUNDARY-SCAN register upon the rising edge of TCK in the Capture-DR state and the contents of the BOUNDARY-SCAN register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-DR state. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 000. . .0 instruction binary code must invoke the EXTEST instruction. During this instruction the BOUNDARY-SCAN register is connected between TDI and TDO in the SHIFT-DR state. Additional binary codes for this instruction are permitted.
2. **SAMPLE/PRELOAD.** This instruction allows a "snapshot" of the normal operation of the component to be taken and examined. It also allows data values to be loaded onto the latched parallel outputs of the BOUNDARY-SCAN SHIFT register prior to selection of another BOUNDARY-SCAN test instruction. During this instruction the BOUNDARY-SCAN register is connected between TDI and TDO in the SHIFT-DR state. When this instruction is selected, the states of all signals on the system pins will be loaded into the BOUNDARY-SCAN register upon the rising edge of TCK in the CAPTURE-DR state and the contents of the BOUNDARY-SCAN register will be loaded into the parallel output register included with the BOUNDARY-SCAN register bits upon the falling edge of TCK in the UPDATE-DR state.

   Note that by interfacing these two actions through the Exit1-DR state, the current state of the system pins can be captured into the BOUNDARY-SCAN register and stored into its parallel output registers for later application back onto those same pins. When the SAMPLE/PRELOAD instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. This instruction is mandatory under the guidelines of IEEE Standard 1149.1, but the binary code may be device specific.
3. **BYPASS.** This instruction allows rapid movement of test data to and from other components on a board that are required to perform test operations by selecting the BYPASS register, a single-bit shift-register stage, between TDI and TDO in the SHIFT-DR state to provide a minimum-length serial scan path. This instruction is mandatory under the guidelines of IEEE Standard 1149.1. The 111. . .1 instruction binary code must invoke the BYPASS instruction. This specific opcode, along with the requirement that an undriven TDI input produce a logic high value, is intended to load the BYPASS instruction during an instruction-scan cycle if the scan chain is broken. In such a case all instructions following the break in the scan chain will be loaded with the BYPASS instruction and hence have no impact upon the system's normal functional operation. Additional binary codes for this instruction are permitted. When the BYPASS instruction is selected, the test logic shall have no impact upon the system logic in performing its system function. When the optional IDCODE register is not included, this instruction is loaded into the INSTRUCTION register in the Test Logic Reset state.
4. **CLAMP.** This instruction allows fixed guarding values to be placed on signals that control the operation of logic not involved in the test, but does not require that the BOUNDARY-SCAN register be part of the serial scan path as in the EXTEST instruction. The contents of the BOUNDARY-SCAN register will solely define the state of the system outputs upon the falling edge of TCK in the UPDATE-IR state for this instruction. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.
5. **HIGHZ.** This instruction allows all of a components system outputs to be placed in an inactive drive state to permit its outputs to be safely backdriven during testing of other integrated circuits on the printed circuit board. All outputs of the device will become inactive even if during their normal system function they are two-state outputs. The BYPASS register is connected between TDI and TDO in the SHIFT-DR state. This instruction is optional under the guidelines of IEEE Standard 1149.1 and therefore the binary code/s may be device specific.
6. **IDCODE.** This instruction allows a blind interrogation of an identification code that is unique to this device type. During this instruction the IDCODE Register is connected between TDI and TDO in the SHIFT-DR state.
7. **SAMPLE-IN.** This instruction is analogous to SAMPLE/PRELOAD but shortens the SCAN chain to include only the input and control pin cells (see Input BOUNDARY-SCAN register definition diagram). During this instruction only the Input BOUNDARY-SCAN register is connected between TDI and TDO in the SHIFT-DR state.
8. **SAMPLE-OUT.** This instruction is analogous to SAMPLE/PRELOAD but shortens the SCAN chain to include only the output and internal TRI-STATE control cells (see Output BOUNDARY-SCAN register definition diagram). During this instruction only the Output BOUNDARY-SCAN register is connected between TDI and TDO in the SHIFT-DR state.

Description of BOUNDARY-SCAN Circuitry (Continued)

9. **EXTEST-OUT.** This instruction is analogous to EXTEST but shortens the SCAN chain to include only the output and internal TRI-STATE control cells (see Output BOUNDARY-SCAN register definition diagram). During this instruction only the Output BOUNDARY-SCAN register is connected between TDI and TDO in the SHIFT-DR state.

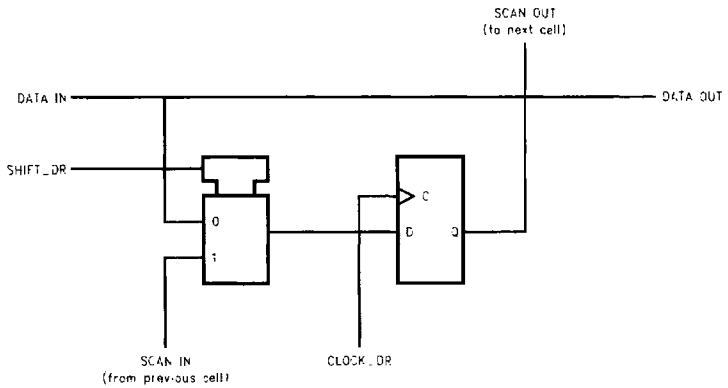
Each of the previously defined instructions fully indicates which data registers may operate or interact with the system logic while the instruction is current. Test data registers that are not selected by the current instruction must be controlled such that they do not interfere with the system logic or the operation of the test data registers currently selected. While a given instruction may lead to operation of more than one test data register, only one test data register may be connected between TDI and TDO during the SHIFT-DR state for the given instruction.

BOUNDARY-SCAN REGISTER

The BOUNDARY-SCAN register permits testing of printed circuit board interconnects such as opens and shorts while also providing access to the components inputs and outputs when testing or monitoring its system logic. This register, as with all test data registers included in a 1149.1-compliant device, must be of fixed length. Data applied at the TDI input must appear without inversion at TDO during the SHIFT-DR state following the appropriate number of TCK cycles determined by the specific fixed length. This test data register will shift one stage toward TDO at each rising edge of TCK in the SHIFT-DR state when selected by the current instruction. Data will be parallel loaded into the BOUNDARY-SCAN register upon a rising edge of TCK in the Capture-DR state and the parallel register stages of the BOUNDARY-SCAN register will be latched upon the falling edge of TCK in the UPDATE-DR state provided that it is selected by the current instruction; otherwise, no change to its contents shall occur.

The shift register stages used in the make-up of the BOUNDARY-SCAN register may or may not be required to incorporate a parallel output register as well as its shift register stage. This requirement depends on the function of the system logic pin with which it is associated as well as the operational requirements of that pin during certain instructions defined for the device. The Input and Output BOUNDARY-SCAN cells demonstrate the parallel register stage, or lack thereof. The first cell can be used on system input pins

Input BOUNDARY-SCAN Cell



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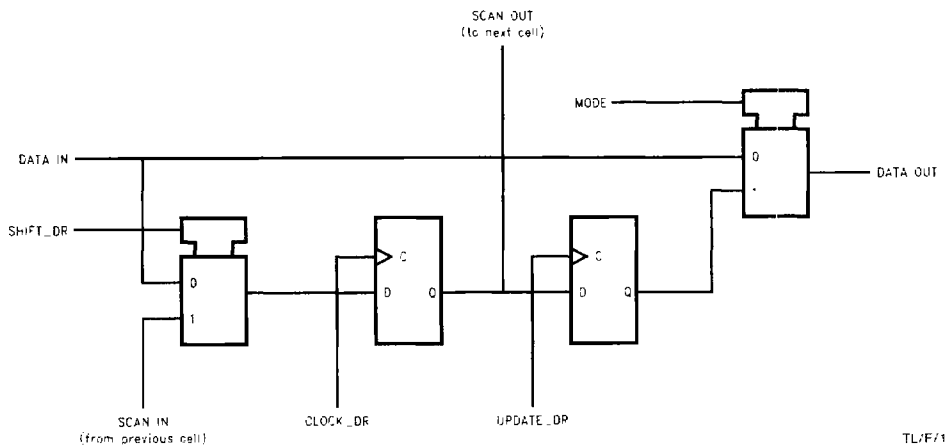
Output BOUNDARY-SCAN Cell



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Description of BOUNDARY-SCAN Circuitry (Continued)

where only observability of its logic state is necessary while the second scan cell can be used at system outputs where observability and controllability are required. Note that in the input scan cell there is no multiplexer directly in the data path while one does exist in the output scan cell. It is the logic gating of the data path that results in the performance penalty of the data path when controlling test logic is added. It is for this reason that the optional INTEST instruction was not included as one of the available features on the products which specifically reference this document. It was deemed unnecessary to pay the performance cost in exchange for the limited functional extension of controlling inputs as well.

If INTEST capability is desired, the system logic of the products referencing this document can be considered an extension of the EXTEST capability. All 1149.1-compliant devices require that the input and output data path scan cells be placed at logically equivalent locations to the system pin. As a result of that action the input/output buffers and voltage level translators are already tested as an extension of interconnect tests. If these interconnect tests are combined with the triggering of a 374 flip-flop clock input, as an example, the internal logic of the device can be evaluated as an extension of the EXTEST capability. Because the National SCAN products currently offered have easily manipulated system logic, the 1149.1 user can logically extend the internal system logic to the EXTEST function. This feature is available during the EXTEST instructions for these products because the state of the outputs is captured along with the state of the inputs during the rising edge of TCK in the CAPTURE-DR state. Note that this is contrary to a recommendation of capturing fixed values on the outputs during EXTEST, but it provides for a feature that would otherwise not exist.

While these cells are sufficient to observe the logic state of the signal in which they are placed, they have a limitation in observing the activity of such a signal as in the specific case of a three-stated output. To determine the activity as well as the logic state of such an output, two such scan cells are required. One in the data signal path and another in the output enable signal path. By observing at both locations the drive activity and/or logic value can be inferred. In the case of a single output enable signal controlling more than one output data path, the output enable signal may be observable and controllable at a single location rather than at each specific output without loss of functional intent provided that the specific location retain control over all the data outputs in unison. This provision is included to reduce the hardware overhead as in the case of a device where such output enable signals are organized byte-wide.

The order of the required scan cells in the BOUNDARY-SCAN register is undefined by the 1149.1 Standard and hence can be device specific even if the system function of that device be identical to another 1149.1-compliant device. In other words, even if two identical system function devices are 1149.1-compliant there is no guarantee that such devices will be identical in the structure of the BOUNDARY-SCAN register.

BYPASS REGISTER

The BYPASS register is also a test data register and therefore must comply with the definitions surrounding test data register operation; but its advantage is in its size, not necessarily in its function. The BYPASS register consists of a single shift register stage in order to shorten the board-level serial scan chain by bypassing some devices while accessing others. This feature is intended to reduce the software overhead in applying and retrieving serial test data by permitting a shortcut between TDI and TDO of any given integrated circuit in order to expedite access to others.

The BYPASS register must capture a logic low value upon the rising edge of TCK in the SHIFT-DR state provided that it is selected by the current instruction. This feature is designed to accompany those devices which incorporate the 32-bit device identification register. (The BYPASS register is a test data register whose least significant bit is a fixed logic high.) Upon an initial scan of the data registers connected across the board, all devices will either connect the BYPASS register or the optional device IDENTIFICATION register in its test data register scan path between TDI and TDO while in the SHIFT-DR state. (This condition is a result of power-up or a logic low assertion to $\overline{\text{TRST}}$ to initialize each 1149.1 device on board.) By shifting the data registers the retrieval of each logic zero indicates a BYPASS register connection until the first logic high is read. The logic high will be the framing bit of a device IDENTIFICATION register which would then indicate that the following thirty-one bits are identifiers to the specific device at that location of the scan chain. The requirement that the BYPASS register capture a logic low value is intended to form the background for the device IDENTIFICATION register framing bit. Additionally, the logic low value is opposite the value to be produced in the case of an undriven TDI input pin.

Input BOUNDARY-SCAN Register

The Input BOUNDARY-SCAN register operates in a manner analogous to the full length BOUNDARY-SCAN register.

Output BOUNDARY-SCAN register

The Output BOUNDARY-SCAN register operates in a manner analogous to the full length BOUNDARY-SCAN register.