54AC/74AC352 • 54ACT/74ACT352

Dual 4-Input Multiplexer

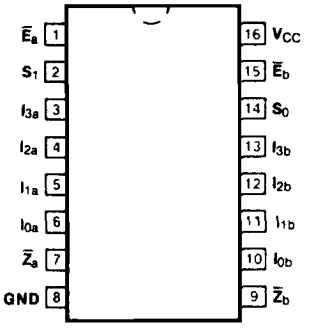
Description

The 'AC/'ACT352 is a very high-speed dual 4-input multiplexer with common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The 'AC/'ACT352 is the functional equivalent of the 'AC/'ACT153 except with inverted outputs.

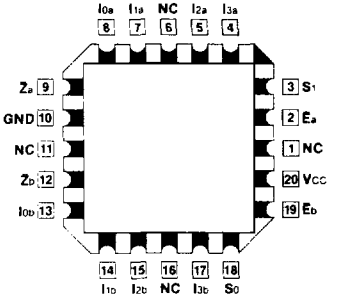
- **Inverted Version of the 'AC/'ACT153**
- **Separate Enables for Each Multiplexer**
- **Outputs Source/Sink 24 mA**
- **'ACT352 has TTL-Compatible Inputs**

Ordering Code: See Section 6

Connection Diagrams

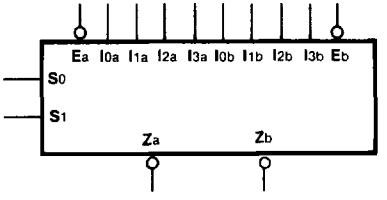


Pin Assignment for DIP, Flatpak and SOIC



Pin Assignment for LCC

Logic Symbol



Pin Names

I_{0a} - I_{3a}	Side A Data Inputs
I_{0b} - I_{3b}	Side B Data Inputs
S_0, S_1	Common Select Inputs
$\overline{E}_a$	Side A Enable Input
$\overline{E}_b$	Side B Enable Input
$\overline{Z}_a$, $\overline{Z}_b$	Multiplexer Outputs

Functional Description

The 'AC/'ACT352 is a dual 4-input multiplexer. It selects two bits of data from up to four sources under the control of the common Select inputs (S_0, S_1). The two 4-input multiplexer circuits have individual active LOW Enables ($\overline{E}_a$, $\overline{E}_b$) which can be used to strobe the outputs independently. When the Enables ($\overline{E}_a$, $\overline{E}_b$) are HIGH, the corresponding outputs ($\overline{Z}_a$, $\overline{Z}_b$) are forced HIGH.

The logic equations for the outputs are shown below:

$$\overline{Z}_a = \overline{E}_a \bullet (I_{0a} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1a} \bullet \overline{S}_1 \bullet S_0 + I_{2a} \bullet S_1 \bullet \overline{S}_0 + I_{3a} \bullet S_1 \bullet S_0)$$

$$\overline{Z}_b = \overline{E}_b \bullet (I_{0b} \bullet \overline{S}_1 \bullet \overline{S}_0 + I_{1b} \bullet \overline{S}_1 \bullet S_0 + I_{2b} \bullet S_1 \bullet \overline{S}_0 + I_{3b} \bullet S_1 \bullet S_0)$$

The 'AC/'ACT352 can be used to move data from a group of registers to a common output bus. The particular register from which the data came would be determined by the state of the Select inputs. A less obvious application is as a function generator. The 'AC/ACT352 can generate two functions of three variables. This is useful for implementing highly irregular random logic.

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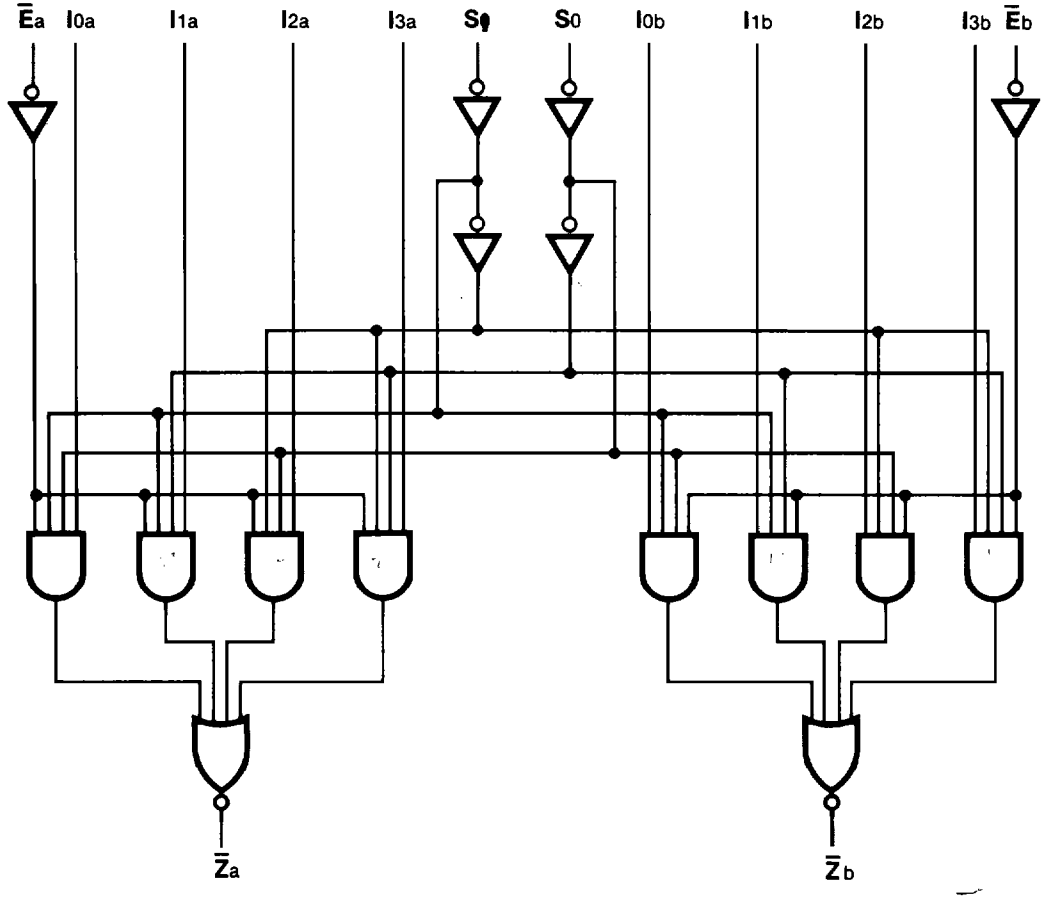
Truth Table

Select Inputs		Inputs (a or b)					Outputs
S_0	S_1	$\overline{E}$	I_0	I_1	I_2	I_3	$\overline{Z}$
X	X	H	X	X	X	X	H
L	L	L	L	X	X	X	H
L	L	L	H	X	X	X	L
H	L	L	X	L	X	X	H
H	L	L	X	H	X	X	L
L	H	L	X	X	L	X	H
L	H	L	X	X	H	X	L
H	H	L	X	X	X	L	H
H	H	L	X	X	X	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

DC Characteristics (unless otherwise specified)

Symbol	Parameter	54AC/ACT	74AC/ACT	Units	Conditions
I_{CC}	Maximum Quiescent Supply Current	160	80	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, T_A = Worst Case
I_{CC}	Maximum Quiescent Supply Current	8.0	8.0	μA	$V_{IN} = V_{CC}$ or Ground, $V_{CC} = 5.5$ V, $T_A = 25°C$
I_{CCT}	Maximum Additional Icc/Input ('ACT352)	1.6	1.5	mA	$V_{IN} = V_{CC} - 2.1$ V $V_{CC} = 5.5$ V T_A = Worst Case

AC Characteristics

Symbol	Parameter	Vcc* (V)	74AC $T_A = +25°C$, $C_L = 50$ pF			54AC $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74AC $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5						ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	3.3 5.0		9.0 6.5						ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	3.3 5.0		6.5 5.0						ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	3.3 5.0		6.5 5.0						ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		8.5 6.0						ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	3.3 5.0		8.5 6.0						ns	3-5

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	74ACT $T_A = +25°C$, $C_L = 50$ pF			54ACT $T_A = -55°C$ to $+125°C$, $C_L = 50$ pF		74ACT $T_A = -40°C$ to $+85°C$, $C_L = 50$ pF		Units	Fig. No.
			Min	Typ	Max	Min	Max	Min	Max		
t_{PLH}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0						ns	3-6
t_{PHL}	Propagation Delay S_n to $\overline{Z}_n$	5.0		7.0						ns	3-6
t_{PLH}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0		5.5						ns	3-6
t_{PHL}	Propagation Delay $\overline{E}_n$ to $\overline{Z}_n$	5.0		5.5						ns	3-6
t_{PLH}	Propagation Delay I_n to $\overline{Z}_n$	5.0		6.5						ns	3-5
t_{PHL}	Propagation Delay I_n to $\overline{Z}_n$	5.0		6.5						ns	3-5

*Voltage Range 5.0 is 5.0 V ± 0.5 V

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Capacitance

Symbol	Parameter	54/74AC/ACT Typ	Units	Conditions
C_{IN}	Input Capacitance	4.5	pF	$V_{CC} = 5.5$ V
C_{PD}	Power Dissipation Capacitance		pF	$V_{CC} = 5.5$ V