P54/74FCT841AT/BT/CT–P54/74FCT843AT/BT/CT–P54/74FCT845AT/BT/CT BUS INTERFACE LATCHES

FEATURES

- **Function, Pinout and Drive Compatible with the FCT, F and AM29841/843/845 Logic**
- **FCT-C speed at 5.5ns max. (Com'l) FCT-B speed at 6.5ns max. (Com'l)**
- **Reduced V_{OH} (typically = 3.3V) versions of Equivalent FCT functions**
- **Edge-rate Control Circuitry for Significantly Improved Noise Characteristics**
- **ESD protection exceeds 2000V**
- **Power-off disable feature**
- **Matched Rise and Fall times**
- **Fully Compatible with TTL Input and Output Logic Levels**
- **64 mA Sink Current (Com'l), 32 mA (Mil) 15 mA Source Current (Com'l), 12 mA (Mil)**
- **Buffered Common Clear and Preset Input**
- **High Speed Parallel Latches**
- **Buffered Common Latch Enable Input**
- **Manufactured in 0.7 micron PACE Technology™**

DESCRIPTION

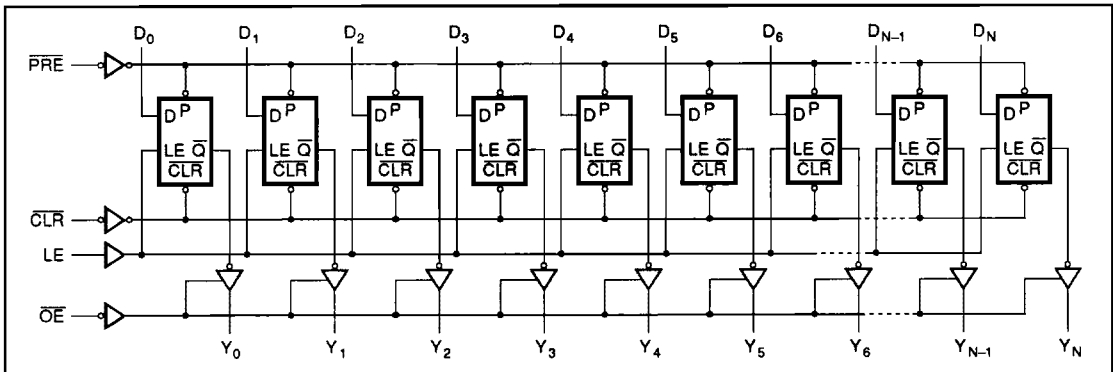
The 'FCT840T series bus interface latches are designed to eliminate the extra packages required to buffer existing latches and provide extra data width for wider address/data paths or buses carrying parity. The 'FCT841T is a buffered 10-bit wide version of the 'FCT373 function. The 'FCT843T is a 9-bit wide buffered latch with Preset ($\overline{PRE}$) and Clear ($\overline{CLR}$) controls making it ideal for parity bus interfacing in high-performance systems. The 'FCT845T is an inverting 8-bit buffered latch with all the 'FCT843T controls plus multiple enables ($\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$) to allow multiusers control of the interface, e.g., $\overline{CS}$, DMA, and RD/$\overline{WR}$. They are ideal for use as an output port requiring high I_{OL}/I_{OH}.

The 'FCT800T high performance interface family is designed for high-capacitance load drive capability while providing low-capacitance bus loading at both inputs and outputs. All inputs have clamp diodes and all outputs are designed for low-capacitance bus loading in the high impedance state.

The 'FCT840T interface family are manufactured using PACE Technology which is Performance Advanced CMOS Engineered to use 0.7 micron effective channel lengths giving 400 picosecond loaded* internal gate delays. PACE Technology includes two-level metal and epitaxial substrates. In addition to very high performance and very high density, the technology features latch-up protection, single event upset protection, and is supported by a Class 1 environment volume production facility.

* For a fan-in/fan-out of 4, at 85°C junction temperature and 5.0V.

FUNCTIONAL BLOCK DIAGRAM

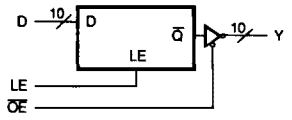


'FCT843T

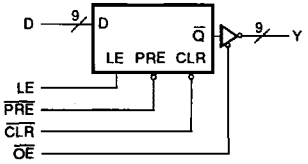
1719 01

LOGIC SYMBOLS

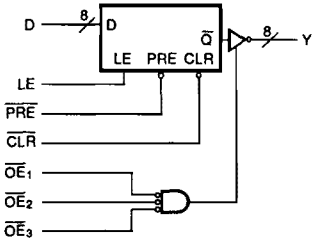
'FCT841T (10-Bit Latch)



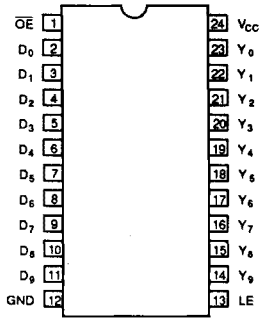
'FCT843T (9-Bit Latch)



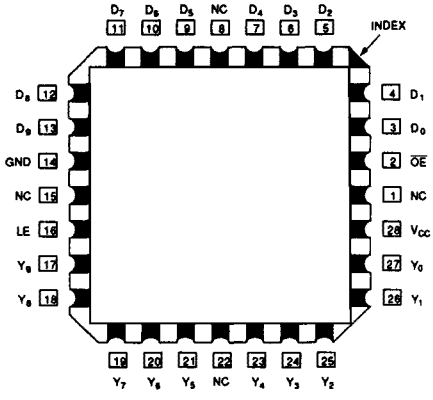
'FCT845T (8-Bit Latch)



PIN CONFIGURATONS

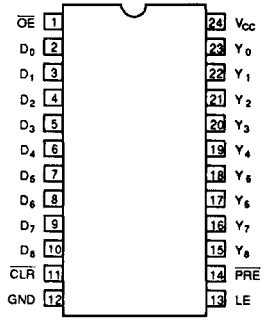


DIP (D4,P4)
SOIC (S4)



LCC (L5-1)

1719 02



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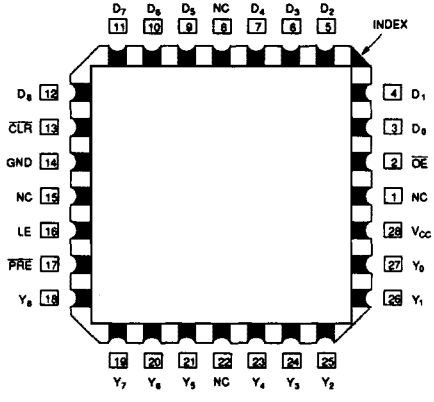
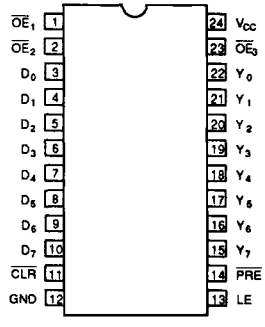
SOIC (S4)

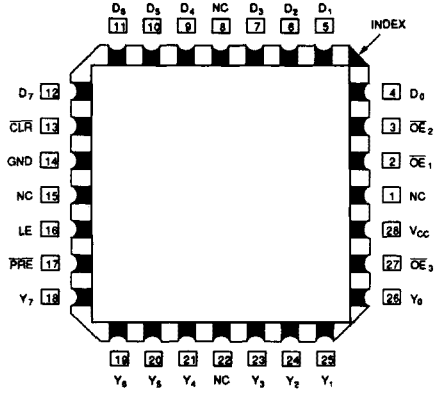


LCC (L5-1)

1719 03



DIP (D4,P4)
SOIC (S4)



LCC (L5-1)

1719 04

PIN DESCRIPTION

Name	I/O	Description
$\overline{CLR}$	I	When $\overline{CLR}$ is low, the outputs are LOW if $\overline{OE}$ is LOW. When $\overline{CLR}$ is HIGH, data can be entered into the latch.
D_1	I	The latch data inputs.
LE	I	The latch enable input. The latches are transparent when LE is HIGH. Input data is latched on the HIGH-to-LOW transition.
Y_1	O	The three-state latch outputs.
$\overline{OE}$	I	The output enable control. When $\overline{OE}$ is LOW, the outputs are enabled. When $\overline{OE}$ is HIGH, the outputs Y_1 are in the high-impedance (off) state.
$\overline{PRE}$	I	Preset line. When $\overline{PRE}$ is LOW, the outputs are HIGH if $\overline{OE}$ is LOW. Preset overrides $\overline{CLR}$.

1719 Tbl 01

FUNCTION TABLES§
'FCT841T/843T/845T

Inputs					Internal	Outputs	Function
$\overline{CLR}$	$\overline{PRE}$	$\overline{OE}$	LE	D_1	O_1	Y_1	
H	H	H	X	X	X	Z	High Z
H	H	H	H	L	L	Z	High Z
H	H	H	H	H	H	Z	HighZ
H	H	H	L	X	NC	Z	Latched (High Z)
H	H	L	H	L	L	L	Transparent
H	H	L	H	H	H	H	Transparent
H	H	L	L	X	NC	NC	Latched
H	L	L	X	X	H	H	Preset
L	H	L	X	X	L	L	Clear
L	L	L	X	X	H	H	Preset
L	H	H	L	X	L	Z	Latched (High Z)
H	L	H	L	X	H	Z	Latched (High Z)

§ H = HIGH, L = LOW, X = Don't care, NC = No Change, Z = High Impedance. 1719 Tbl 02

7

ABSOLUTE MAXIMUM RATINGS[1,2]

Symbol	Parameter	Value	Unit
T_{STG}	Storage Temperature	−65 to +150	°C
T_A	Ambient Temperature Under Bias	−65 to +135	°C
V_{CC}	V_{CC} Potential to Ground	−0.5 to +7.0	V
P_T	Power Dissipation	0.5	W

1719 Tbl 03

Symbol	Parameter	Value	Unit
I_{OUTPUT}	Current Applied to Output	120	mA
V_{IN}	Input Voltage	−0.5 to +7.0	V
V_{OUT}	Voltage Applied to Output	−0.5 to +7.0	V

1719 Tbl 04

Notes:

1. Operation beyond the limits set forth in the above table may impair the useful life of the device. Unless otherwise noted, these limits are over the operating free-air temperature range.
2. Unused inputs must always be connected to an appropriate logic voltage level, preferably either V_{CC} or ground.

RECOMMENDED OPERATING CONDITIONS

Free Air Ambient Temperature	Min	Max
Military	−55°C	+125°C
Commercial	0°C	+70°C

1719 Tbl 05

Supply Voltage (V_{CC})	Min	Max
Military	+4.5V	+5.5V
Commercial	+4.75V	+5.25V

1719 Tbl 06

DC ELECTRICAL CHARACTERISTICS (Over recommended operating conditions)

Symbol	Parameter		Min	Typ[1]	Max	Units	V_{CC}	Conditions
V_{IH}	Input HIGH Voltage		2.0			V		
V_{IL}	Input LOW Voltage				0.8	V		
V_H	Hysteresis			0.2		V		All inputs
V_{IK}	Input Clamp Diode Voltage			−0.7	−1.2	V	MIN	I_{IN} = −18mA
V_{OH}	Output HIGH Voltage	Military	2.4	3.3		V	MIN	I_{OH} = −12mA
		Commercial	2.4	3.3		V	MIN	I_{OH} = −15mA
V_{OL}	Output LOW Voltage	Military		0.3	0.5	V	MIN	I_{OL} = 32mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 48mA
		Commercial		0.3	0.5	V	MIN	I_{OL} = 64mA
I_I	Input HIGH Current				20	µA	MAX	V_{IN} = V_{CC}
I_{IH}	Input HIGH Current				5	µA	MAX	V_{IN} = 2.7V
I_{IL}	Input LOW Current				−5	µA	MAX	V_{IN} = 0.5V
I_{OZH}	Off State I_{OUT} HIGH-Level Output Current				10	µA	MAX	V_{OUT} = 2.7V
I_{OZL}	Off State I_{OUT} LOW-Level Output Current				−10	µA	MAX	V_{OUT} = 0.5V
I_{OS}	Output Short Circuit Current[2]		−60	−120	−225	mA	MAX	V_{OUT} = 0.0V
I_{OFF}	Power-off Disable				100	µA	0V	V_{OUT} = 4.5V
C_{IN}	Input Capacitance[3]			5	10	pF	MAX	All inputs
C_{OUT}	Output Capacitance[3]			9	12	pF	MAX	All outputs
I_{CC}	Quiescent Power Supply Current			0.2	1.5	mA	MAX	$V_{IN} \leq 0.2V$, $V_{IN} \geq V_{CC} - 0.2V$

1719 Tbl 07

Notes:

1. Typical limits are at V_{CC} = 3.3V, T_A = +25°C ambient.
2. Not more than one output should be shorted at a time. Duration of short should not exceed one second. The use of high speed test apparatus and/or sample and hold techniques are preferable in order to minimize internal chip heating and more accurately reflect operational values. Otherwise prolonged shorting of a high output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
3. This parameter is guaranteed but not tested.

DC CHARACTERISTICS (Over recommended operating conditions unless otherwise specified.)

Symbol	Parameter	Typ[1]	Max	Units	Conditions
ΔI_{CC}	Quiescent Power Supply Current (TTL inputs)	0.5	2.0	mA	V_{CC} = MAX, V_{IN} = 2.7V[2], f_1 = 0, Outputs Open
I_{CCD}	Dynamic Power Supply Current[3]	0.15	0.25	mA/ mHz	V_{CC} = MAX, One Input Toggling, 50% Duty Cycle, Outputs Open, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
I_C	Total Power Supply Current[5]	1.7	4.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		2.0	5.0	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, One Bit Toggling at f_1 = 10mHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND
		3.2	6.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$
		5.2	14.5[4]	mA	V_{CC} = MAX, 50% Duty Cycle, Outputs Open, Eight Bits Toggling at f_1 = 2.5MHz, $\overline{OE}$ = GND, LE = V_{CC}, V_{IN} = 3.4V or V_{IN} = GND

1719 Tbl 08

Notes:

1. Typical values are at V_{CC} = 3.3V, +25°C ambient.
2. Per TTL driven input (V_{IN} = 2.7V); all other inputs at V_{CC} or GND.
3. This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
4. Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
5. $I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}$
   $I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD}(f_0/2 + f_1 N_1)$
   I_{CC} = Quiescent Current with CMOS input levels
   ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 2.7V)
   D_H = Duty Cycle for TTL Inputs High
   N_T = Number of TTL Inputs at D_H
   I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
   f_0 = Clock Frequency for Register Devices (Zero for Non-Register Devices)
   f_1 = Input Frequency
   N_1 = Number of Inputs at f_1
   All currents are in milliamps and all frequencies are in megahertz.

7

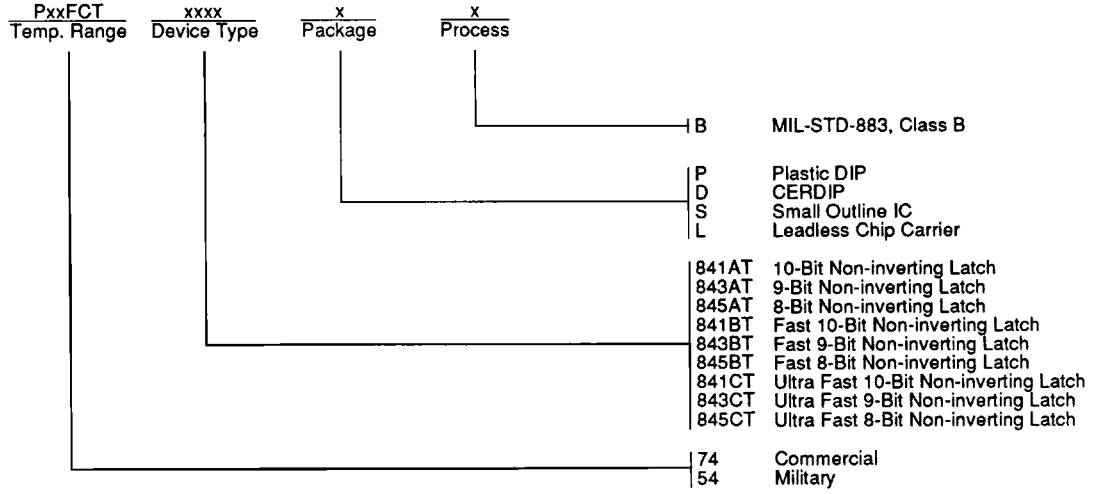
SWITCHING CHARACTERISTICS OVER OPERATING RANGE

Sym.	Parameter		Test Conditions[1]	FCT841AT/843AT/845AT				FCT841BT/843BT/845BT				FCT841CT/843CT/845CT				Units
				MIL		COM'L		MIL		COM'L		MIL		COM'L		
				Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	Min.[2]	Max.	
t_{PLH} t_{PHL}	Propagation Delay D_i to Y_i ($\overline{LE}$ = HIGH)		C_L = 50pF R_L = 500Ω		10.0		9.0		7.5		6.5		6.3		5.5	ns
			C_L = 300pF[3] R_L = 500Ω		15.0		13.0		15.0		13.0		15.0		13.0	ns
t_{SU}	Data to LE Set-up Time		C_L = 50pF	2.5		2.5		2.5		2.5		2.5		2.5		ns
t_H	Data to LE Hold Time		R_L = 500Ω	3.0		2.5		2.5		2.5		2.5		2.5		ns
t_{PLH} t_{PHL}	Propagation Delay LE to Y_i		C_L = 50pF R_L = 500Ω		13.0		12.0		10.5		8.0		6.8		6.4	ns
			C_L = 300pF[3] R_L = 500Ω		20.0		16.0		18.0		15.5		16.0		15.0	ns
t_{PLH}	Propagation Delay $\overline{PRE}$ to Y_i		C_L = 50pF R_L = 500Ω		14.0		12.0		10.0		8.0		9.0		7.0	ns
t_{REM}	Recovery Time $\overline{PRE}$ to Y_i				17.0		14.0		13.0		10.0		12.0		9.0	ns
t_{PHL}	Propagation Delay $\overline{CLR}$ to Y_i				14.0		13.0		11.0		10.0		10.0		9.0	ns
t_{REM}	Recovery Time $\overline{CLR}$ to Y_i				17.0		14.0		10.0		10.0		9.0		9.0	ns
t_W	LE Pulse Width[3]	HIGH		5.0		4.0		4.0		4.0		4.0		4.0		ns
t_W	$\overline{PRE}$ Pulse Width[3]	LOW		7.0		5.0		4.0		4.0		4.0		4.0		ns
t_W	$\overline{CLR}$ Pulse Width[3]	LOW		5.0		4.0		4.0		4.0		4.0		4.0		ns
t_{PZH} t_{PZL}	Output Enable Time $\overline{OE}$ to Y_i		C_L = 50pF R_L = 500Ω		13.0		11.5		8.5		8.0		7.3		6.5	ns
			C_L = 300pF[3] R_L = 500Ω		25.0		23.0		15.0		14.0		13.0		12.0	ns
t_{PHZ} t_{PLZ}	Output Disable Time $\overline{OE}$ to Y_i		C_L = 5pF[3] R_L = 500Ω		9.0		7.0		6.5		6.0		6.0		5.7	ns
			C_L = 50pF R_L = 500Ω		10.0		8.0		7.5		7.0		6.3		6.0	ns

1719 Tbl 09

Notes:
1. See test circuit and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameters are guaranteed but not tested.

ORDERING INFORMATION



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7