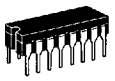
Quint Latch

MC10H175

The MC10H175 is a quint D type latch with common reset and clock lines. This MECL 10KH part is a functional/pinout duplication of the standard MECL 10K family part, with 100% improvement in propagation delay and no increase in power–supply current.

- Propagation Delay, 1.2 ns Typical
- Power Dissipation, 400 mW Typical
- Improved Noise Margin 150 mV (Over Operating Voltage and Temperature Range)
- Voltage Compensated
- MECL 10K–Compatible



L SUFFIX
CERAMIC PACKAGE
CASE 620–10

P SUFFIX
PLASTIC PACKAGE
CASE 648–08

FN SUFFIX
PLCC
CASE 775–02

MAXIMUM RATINGS

Characteristic	Symbol	Rating	Unit
Power Supply (V_{CC} = 0)	V_{EE}	–8.0 to 0	Vdc
Input Voltage (V_{CC} = 0)	V_I	0 to V_{EE}	Vdc
Output Current — Continuous — Surge	I_{out}	50 100	mA
Operating Temperature Range	T_A	0 to +75	°C
Storage Temperature Range — Plastic — Ceramic	T_{stg}	–55 to +150 –55 to +165	°C °C

ELECTRICAL CHARACTERISTICS (V_{EE} = –5.2 V ±5%) (See Note)

		0°		25°		75°		
Characteristic	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Unit**
Power Supply Current	I_E	—	107	—	97	—	107	mA
Input Current High Pins 5,6,7,9,10,12,13 Pin 11	I_{inH}	 — —	 565 1120	 — —	 335 660	 — —	 335 660	µA
Input Current Low	I_{inL}	0.5	—	0.5	—	0.3	—	µA
High Output Voltage	V_{OH}	–1.02	–0.84	–0.98	–0.81	–0.92	–0.735	Vdc
Low Output Voltage	V_{OL}	–1.95	–1.63	–1.95	–1.63	–1.95	–1.60	Vdc
High Input Voltage	V_{IH}	–1.17	–0.84	–1.13	–0.81	–1.07	–0.735	Vdc
Low Input Voltage	V_{IL}	–1.95	–1.48	–1.95	–1.48	–1.95	–1.45	Vdc

AC PARAMETERS

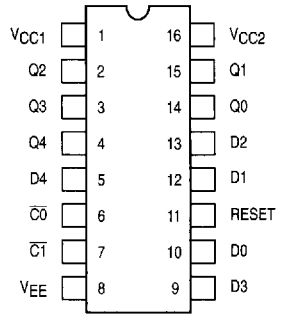
Propagation Delay Data Clock Reset	t_{pd}	 0.6 0.7 1.0	 1.6 1.9 2.2	 0.6 0.7 1.0	 1.6 2.0 2.3	 0.6 0.8 1.0	 1.7 2.1 2.4	ns
Set–up Time	t_{set}	1.5	—	1.5	—	1.5	—	ns
Hold Time	t_{hold}	0.8	—	0.8	—	0.8	—	ns
Rise Time	t_r	0.5	1.8	0.5	1.9	0.5	2.0	ns
Fall Time	t_f	0.5	1.8	0.5	1.9	0.5	2.0	ns

NOTE:
Each MECL 10H series circuit has been designed to meet the dc specifications shown in the test table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 linear fpm is maintained. Outputs are terminated through a 50–ohm resistor to –2.0 volts.

TRUTH TABLE

D	$\overline{C0}$	$\overline{C1}$	Reset	Q_{n+1}
L	L	L	X	L
H	L	L	X	H
X	H	X	L	Qn
X	X	H	L	Qn
X	H	X	H	L
X	X	H	H	L

DIP PIN ASSIGNMENT



Pin assignment is for Dual–in–Line Package.
For PLCC pin assignment, see the Pin Conversion Tables on page 6–11.

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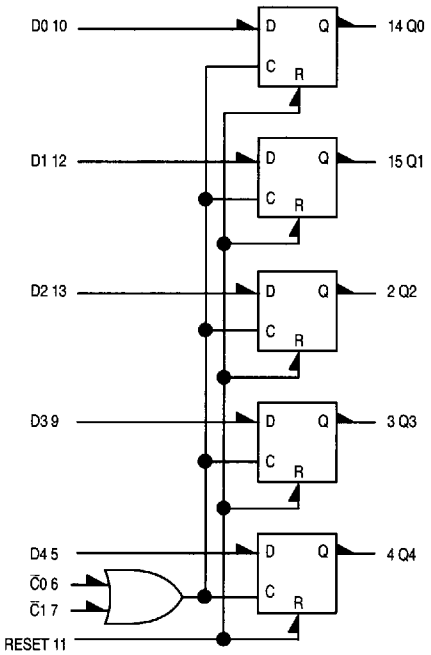
APPLICATION INFORMATION

The MC10H175 is a high speed, low power quint latch. It features five D type latches with common reset and a common two–input clock. Data is transferred on the negative edge of the clock and latched on the positive edge. The two clock inputs are "OR"ed together.

Any change on the data input will be reflected at the outputs while the clock is low. The outputs are latched on the positive transition of the clock. While the clock is in the high state, a change in the information present at the data inputs will not affect the output information. **THE RESET INPUT IS ENABLED ONLY WHEN THE CLOCK IS IN THE HIGH STATE**.

LOGIC DIAGRAM



V_{CC1} = PIN 1
V_{CC2} = PIN 16
V_{EE} = PIN 8