



(Separate preset, common clock and clear)

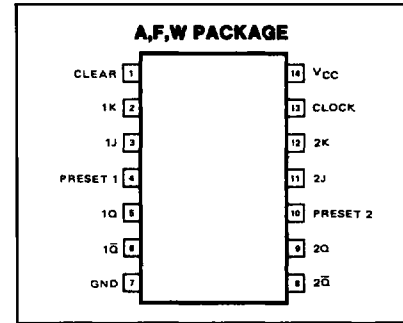
SPEED/PACKAGE AVAILABILITY

54LS F,W 74LS A,F
 54S A,F,W 74S A,F

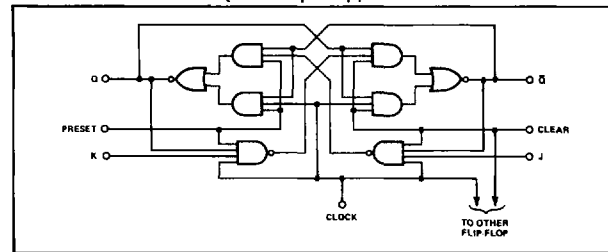
DESCRIPTION

The preset or clear inputs, when low, set or reset the outputs regardless of the levels at the other inputs. When preset and clear inputs are inactive (high), a high level at the clock input enables the J and K inputs and data will be accepted. The logic levels at the J and K inputs may be allowed to change when the clock pulse is high and the bistable will perform according to the function table as long as minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

PIN CONFIGURATION



BLOCK DIAGRAM (Each Flip-Flop)



SWITCHING CHARACTERISTICS $V_{CC} = 5V, T_A = 25^\circ C$

| TEST CONDITIONS | | | 54/74LS | | | 54/74S | | | UNIT |
|--------------------------------------|----------------------------------|------------------|---------|-----|-----|--------|-----|-----|------|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| PARAMETER | FROM INPUT | TO OUTPUT | | | | | | | |
| f_{Clock} Clock frequency | | | 30 | 45 | | 80 | 125 | | MHz |
| t_w (Clock) Width of clock pulse | | | 20 | | | | | | ns |
| | | | | | | 6 | | | |
| | | | | | | 6.5 | | | |
| t_w (Preset) Width of preset pulse | | | 25 | | | 8 | | | ns |
| t_w (Clear) Width of clear pulse | | | 25 | | | 8 | | | ns |
| t_{Setup} Input setup time | | | 20↓ | | | 3↓ | | | ns |
| t_{Hold} Input hold time | | | 0↓ | | | 0↓ | | | ns |
| Propagation delay time | | | | | | | | | |
| t_{PLH} Low-to-high | CLR, PRE or CLK (as appropriate) | | | 11 | 20 | 2 | 4 | 7 | ns |
| t_{PHL} High-to-low | | | | 15 | 30 | 2 | 5 | 7 | |

Load circuit and typical waveforms are shown at the front of section.

TRUTH TABLE (Each Flip-Flop)

| Inputs | | | | | Outputs | |
|--------|-------|-------|---|---|---------|-------------|
| Preset | Clear | Clock | J | K | Q | \bar{Q} |
| L | H | X | X | X | H | L |
| H | L | X | X | X | L | H |
| L | L | X | X | X | H* | H* |
| H | H | ↓ | L | L | Q_0 | \bar{Q}_0 |
| H | H | ↓ | H | L | H | L |
| H | H | ↓ | L | H | L | H |
| H | H | ↓ | H | H | Toggle | Toggle |
| H | H | H | X | X | Q_0 | \bar{Q}_0 |

H = high level (steady state)
 L = low level (steady state)
 X = irrelevant
 ↓ = transition from high to low level
 Q_0 = the level of Q before the indicated steady-state input conditions were established
 TOGGLE: = Each output changes to the complement of its previous level on each clock transition.
 *This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.