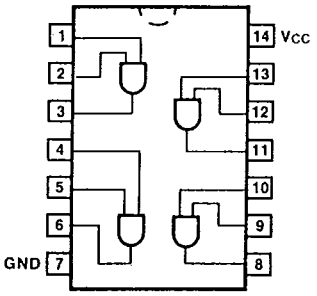
54/7409
54S/74S09
54LS/74LS09

QUAD 2-INPUT AND GATE
(With Open-Collector Output)

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	7409PC, 74S09PC 74LS09PC		9A
Ceramic DIP (D)	A	7409DC, 74S09DC 74LS09DC	5409DM, 54S09DM 54LS09DM	6A
Flatpak (F)	A	7409FC, 74S09FC 74LS09FC	5409FM, 54S09FM 54LS09FM	3I

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PINS	54/74 (U.L.) HIGH/LOW	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
Inputs	1.0/1.0	1.25/1.25	0.5/0.25
Outputs	OC**/10	OC**/12.5	OC**/5.0 (2.5)

DC AND AC CHARACTERISTICS: See Section 3*

SYMBOL	PARAMETER	54/74 Min	54/74 Max	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS	
I_{CCH}	Power Supply Current		21		32		4.8	mA	V_{IN} = Open	V_{CC} = Max
I_{CCL}			33		57		8.8		V_{IN} = Gnd	
t_{PLH}	Propagation Delay		32	2.0	10		20	ns	Fig. 3-2, 3-5	
t_{PHL}			24	2.0	10		15			

*DC limits apply over operating temperature range; AC limits apply at T_A = +25°C and V_{CC} = +5.0 V.
**OC — Open Collector