M5M52B88J-8,-10,-12

262144-BIT (32768-WORD BY 8-BIT) BiCMOS STATIC RAM

DESCRIPTION

The M5M52B88 is a family of 32768-word by 8-bit static RAMs, fabricated with the high-performance BiCMOS process and designed for high-speed application. These devices operate on a single 5V supply, and are directly TTL compatible. They include a power-down feature as well.

FEATURES

- Fast access time M5M52B88J-8 ..... 8ns(max)
  M5M52B88J-10 ..... 10ns(max)
  M5M52B88J-12 ..... 12ns(max)
- Low power dissipation Active ..... 450mW(typ)
  Stand by ..... 50mW(typ)
- Power down by $\overline{S}$
- Center power (Vcc, GND) pin out
- Single 5V power supply
- Fully static operation
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- Easy memory expansion by chip-select ($\overline{S}$) input
- Output enable ($\overline{OE}$) prevents data contention in the I/O bus
- All address inputs are changeable with each other.

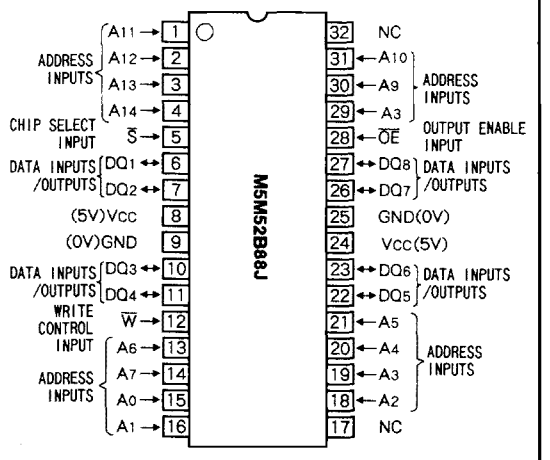
APPLICATION

High-speed memory systems

FUNCTION

A write operation is executed during the $\overline{S}$ low, and $\overline{W}$ low overlap time. In this period, address signals must be stable. When $\overline{W}$ is low, the DQ terminal is maintained in the high impedance state.

PIN CONFIGURATION (TOP VIEW)



Outline 32P0J(SOJ)

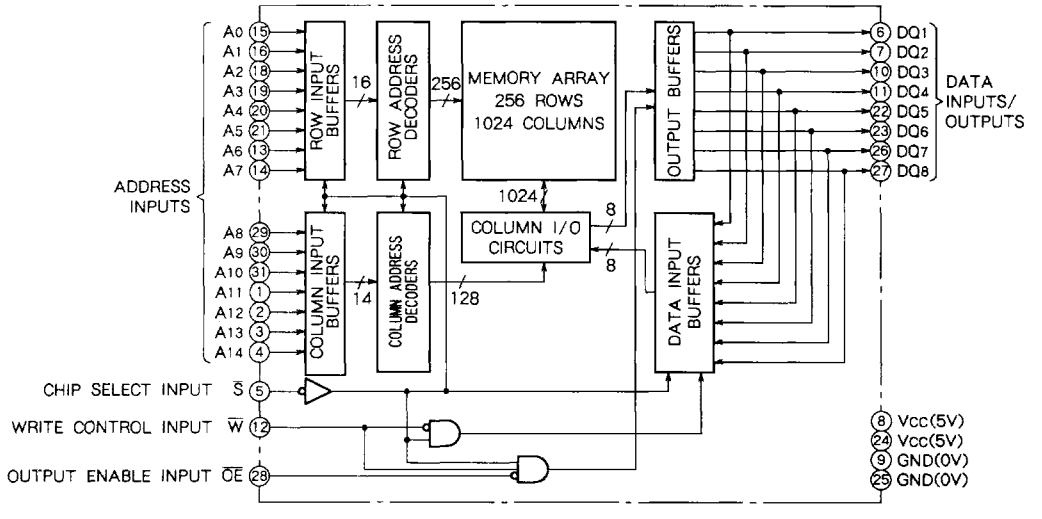
NC : NO CONNECTION

In a read operation, after setting $\overline{W}$ to high, $\overline{S}$ to low, and $\overline{OE}$ to low if the address signals are stable, the data is available at the DQ terminal.

When $\overline{S}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other devices.

Single $\overline{S}$ controls the power-down feature. When $\overline{S}$ goes high, power dissipation is reduced extremely. The access time from $\overline{S}$ is equivalent to the address access time.

BLOCK DIAGRAM



MITSUBISHI ELECTRIC

MODE SELECTION

$\overline{S}$	$\overline{W}$	$\overline{OE}$	Mode	Data input/output	Icc
H	X	X	Non selection	High-impedance	Stand by
L	L	X	Write	Din	Active
L	H	L	Read	Dout	Active
L	H	H		High-impedance	Active

H : VIH L : VIL X : VIH or VIL

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
Vcc	Supply voltage	With respect to GND	−3.5* ~7	V
VI	Input voltage		−3.5* ~7	V
Vo	Output voltage		−3.5* ~7	V
Pd	Maximum power dissipation		1	W
Topr	Operating temperature		0~70	℃
Tstg(bias)	Storage temperature(bias)		−10~85	℃
Tstg	Storage temperature		−65~150	℃

* Pulse width ≦ 10ns, In case of DC : −0.5V

DC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min	Limits Typ	Limits Max	Unit
VIH	High-level input voltage			2.2		Vcc+0.3	V
VIL	Low-level input voltage			−0.5*		0.8	V
VOH	High-level output voltage	IOH = −4mA		2.4			V
VOL	Low-level output voltage	IOL = 8mA				0.4	V
II	Input current	VI = 0~Vcc				2	μA
I IOZ I	Off-state output current	VI(S) = VIH, VO = 0~Vcc				10	μA
ICC1	Supply current from Vcc	VI(S) = VIL, Output open	AC(8ns cycle)			195	mA
			AC(10ns cycle)			185	
			AC(12ns cycle)			175	
			DC		90	115	
ICC2	Stand by current	VI(S) = VIH	AC(8ns cycle)			70	mA
			AC(10,12ns cycle)			60	
			Other VI≧VIH or ≦VIL			50	
ICC3	Stand by current	VI(S) = Vcc − 0.2V, Other VI ≦ 0.2V or VI ≧ Vcc − 0.2V				10	mA

Note 1. Current flow into an IC is positive, out is negative.
* −3.0V in case of AC (Pulse width ≦ 10ns)

CAPACITANCE

Symbol	Parameter	Test conditions	Limits Min	Limits Typ	Limits Max	Unit
CI	Input capacitance	VI = GND, VI = 25mVrms, f = 1MHz			5	pF
Co	Output capacitance	Vo = GND, Vo = 25mVrms, f = 1MHz			7	pF

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70℃, Vcc = 5V ± 10%, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

Input pulse levels ····· VIH = 3V, VIL = 0V
Input rise and fall time ····· 3ns
Input timing reference levels ····· VIH = 1.5V, VIL = 1.5V
Output timing reference levels ··· VOH = 1.5V, VOL = 1.5V
Output loads ····· Fig.1, Fig.2

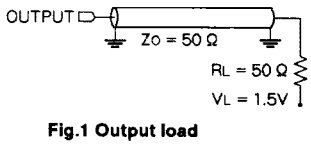


Fig.1 Output load

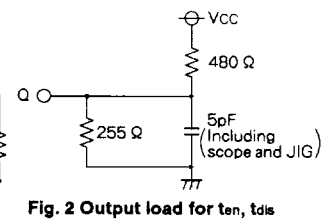


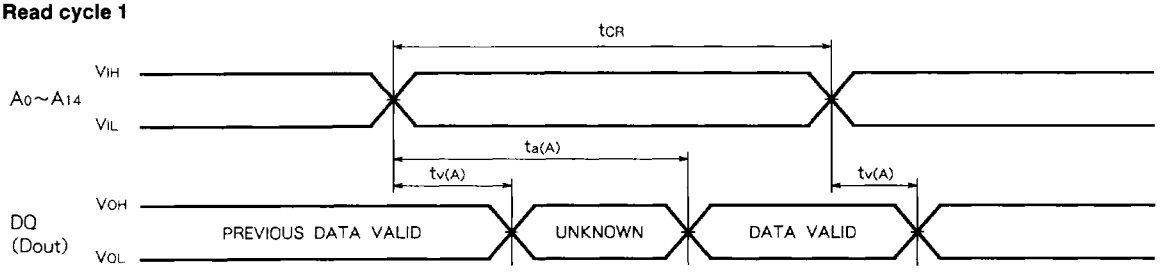
Fig. 2 Output load for ten, tdis

(2) READ CYCLE

Symbol	Parameter	Limits						Unit
		M5M52B88-8		M5M52B88-10		M5M52B88-12		
		Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	8		10		12		ns
$t_{a(A)}$	Address access time		8		10		12	ns
$t_{a(S)}$	Chip select access time		8		10		12	ns
$t_{a(OE)}$	Output enable access time		4		5		6	ns
$t_{v(A)}$	Data valid time after address change	3		4		4		ns
$t_{en(S)}$	Output enable time from($\overline{S}$)	3		4		4		ns
$t_{en(OE)}$	Output enable time from($\overline{OE}$)	3		3		3		ns
$t_{dis(S)}$	Output disable time from($\overline{S}$)	0	4	0	5	0	6	ns
$t_{dis(OE)}$	Output disable time from($\overline{OE}$)	0	4	0	5	0	6	ns
t_{PU}	Power-up time after chip selection	0		0		0		ns
t_{PD}	Power-down time after chip selection		8		10		12	ns

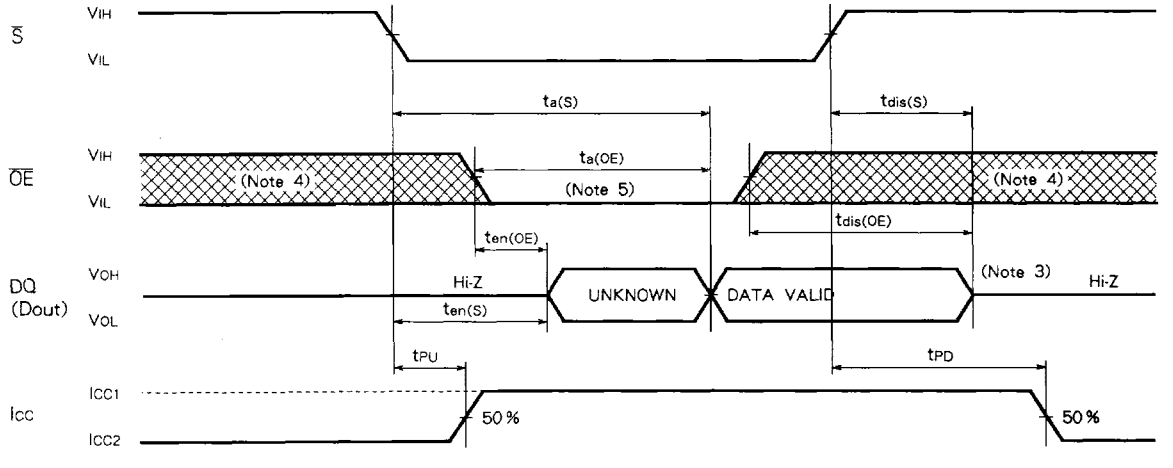
(3) TIMING DIAGRAMS FOR READ CYCLE

Read cycle 1



$\overline{W}$ = H $\overline{S}$ = L $\overline{OE}$ = L

Read cycle 2 (Note 2)



$\overline{W}$ = H

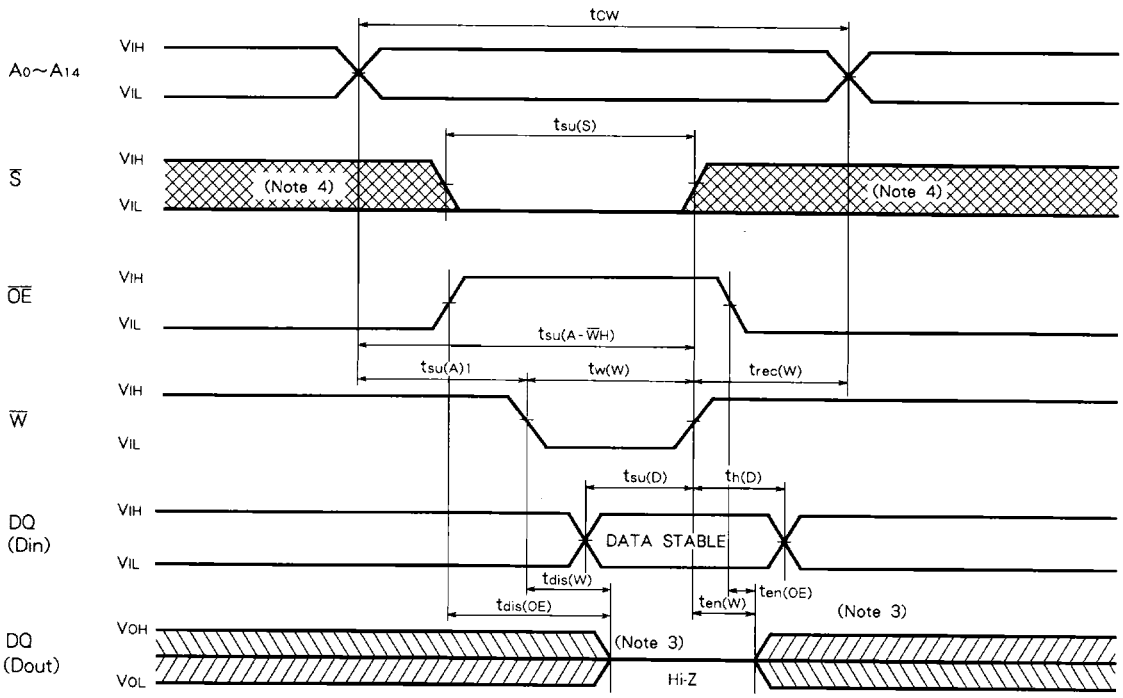
Note 2. Addresses valid prior to or coincident with $\overline{S}$ transition low.
3. Transition is measured ± 500mV from steady state voltage with specified loading in Figure2.
4. Hatching indicates the state is don't care.
5. Addresses and $\overline{S}$ valid prior $\overline{OE}$ transition low by [$t_{a(A)} - t_{a(OE)}$, $t_{a(S)} - t_{a(OE)}$].

(4) WRITE CYCLE

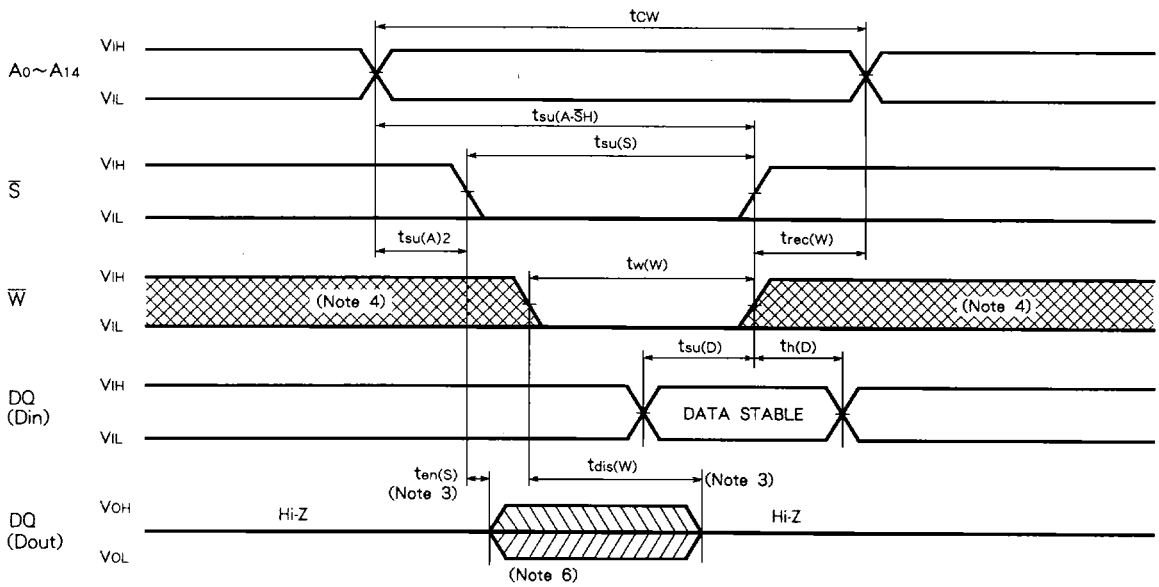
Symbol	Parameter	Limits						Unit
		M5M52B88-8		M5M52B88-10		M5M52B88-12		
		Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	8		10		12		ns
$t_{su(S)}$	Chip select setup time	7		9		10		ns
$t_{su(A)1}$	Address setup time($\overline{W}$)	0		0		0		ns
$t_{su(A)2}$	Address setup time($\overline{S}$)	0		0		0		ns
$t_{w(W)}$	Write pulse width	7		9		10		ns
$t_{rec(W)}$	Write recovery time	0		0		0		ns
$t_{su(D)}$	Data setup time	4		5		6		ns
$t_{h(D)}$	Data hold time	0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$	0	4	0	5	0	6	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$	0	4	0	5	0	6	ns
$t_{en(W)}$	Output enable time from $\overline{W}$	0		0		0		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$	0		0		0		ns
$t_{su(A-\overline{W}H)}$	Address to $\overline{W}$ high	7		9		10		ns
$t_{su(A-\overline{S}H)}$	Address to $\overline{S}$ high	7		9		10		ns

(5) TIMING DIAGRAMS FOR WRITE CYCLE

Write cycle 1 ($\overline{W}$ control mode)



Write cycle 2 ($\overline{S}$ control mode)



Note 6. When the falling edge of $\overline{W}$ is simultaneous or prior to the falling edge of $\overline{S}$, the output is maintained in the high impedance.